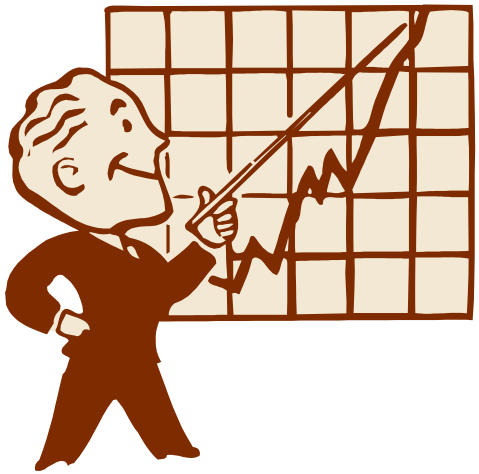
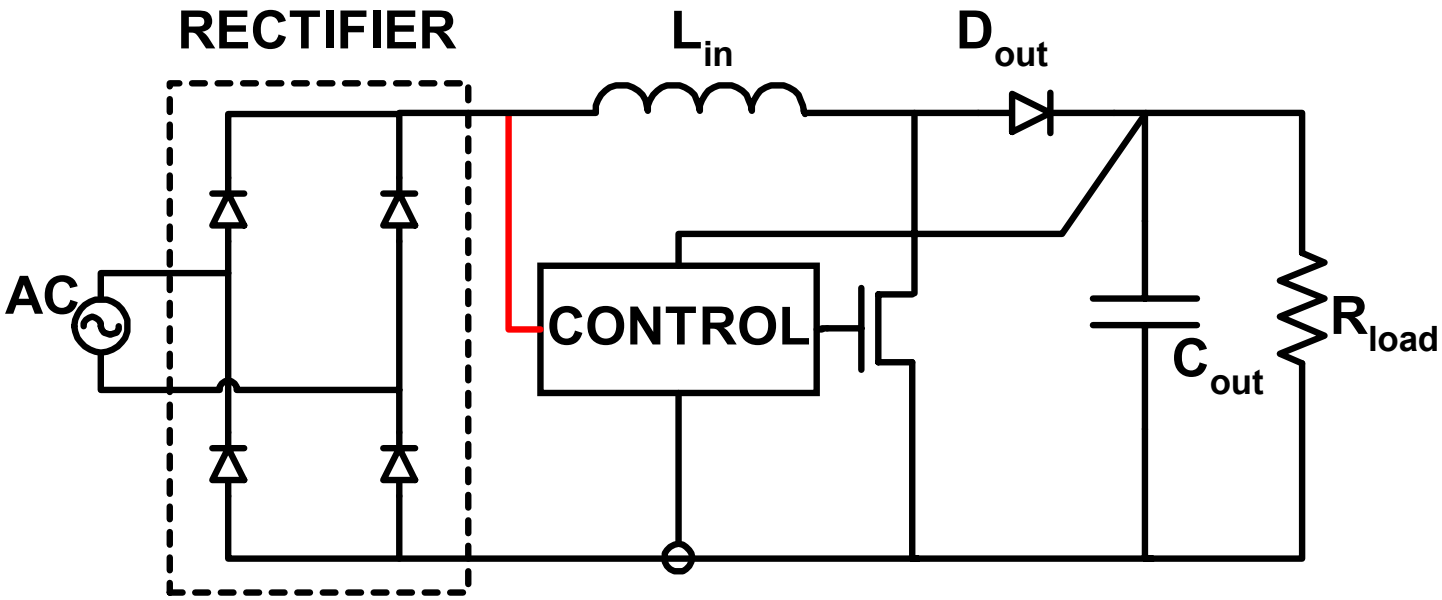
Active Power Factor Correction:

GPT's approach

Theory of Operation

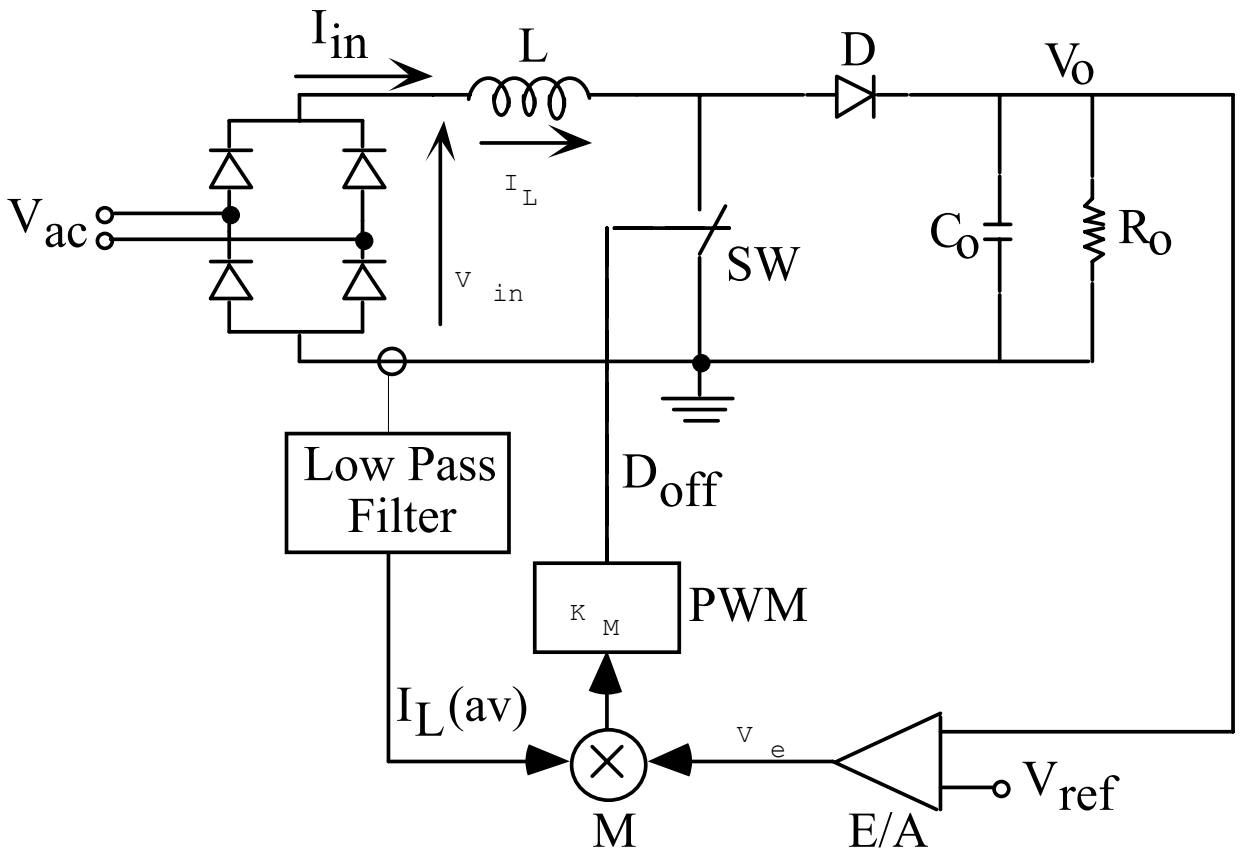


The GPT's Control Concept

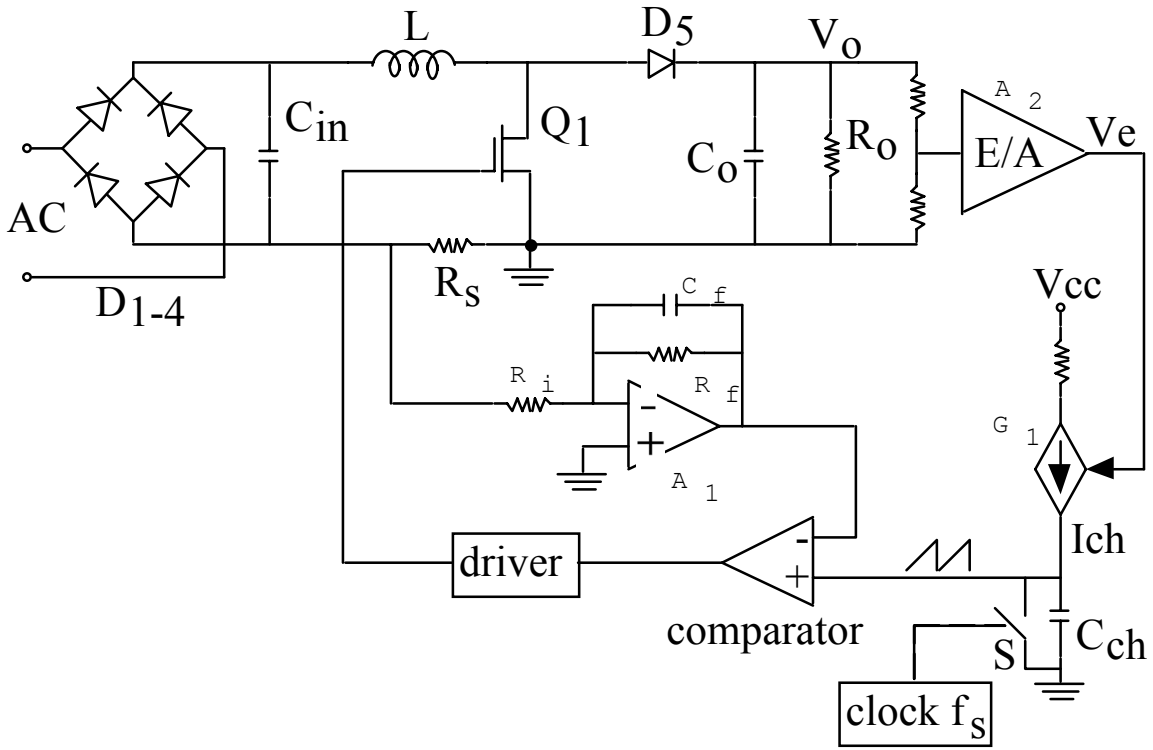


✓ With no "RED" connection, the active parts can be easily combined into one unit

The GPT's Control Concept



Method Implementation



- No analog multiplier is required

US006307361B1

(12) **United States Patent**
Yaakov et al.

(10) **Patent No.: US 6,307,361 B1**
(45) **Date of Patent: Oct. 23, 2001**

(54) **METHOD AND APPARATUS FOR REGULATING THE INPUT IMPEDANCE OF PWM CONVERTERS**

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(73) Assignee: **Green Power Technologies Ltd.**, Rehovot (IL)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/840,889**

(22) Filed: **Apr. 25, 2001**

(51) **Int. Cl.**[7] **G05F 1/46**; G05F 1/614
(52) **U.S. Cl.** **323/288**; 323/284
(58) **Field of Search** 323/222, 282, 323/284, 285, 288, 290, 351

(56) **References Cited**

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Primary Examiner—Jessica Han
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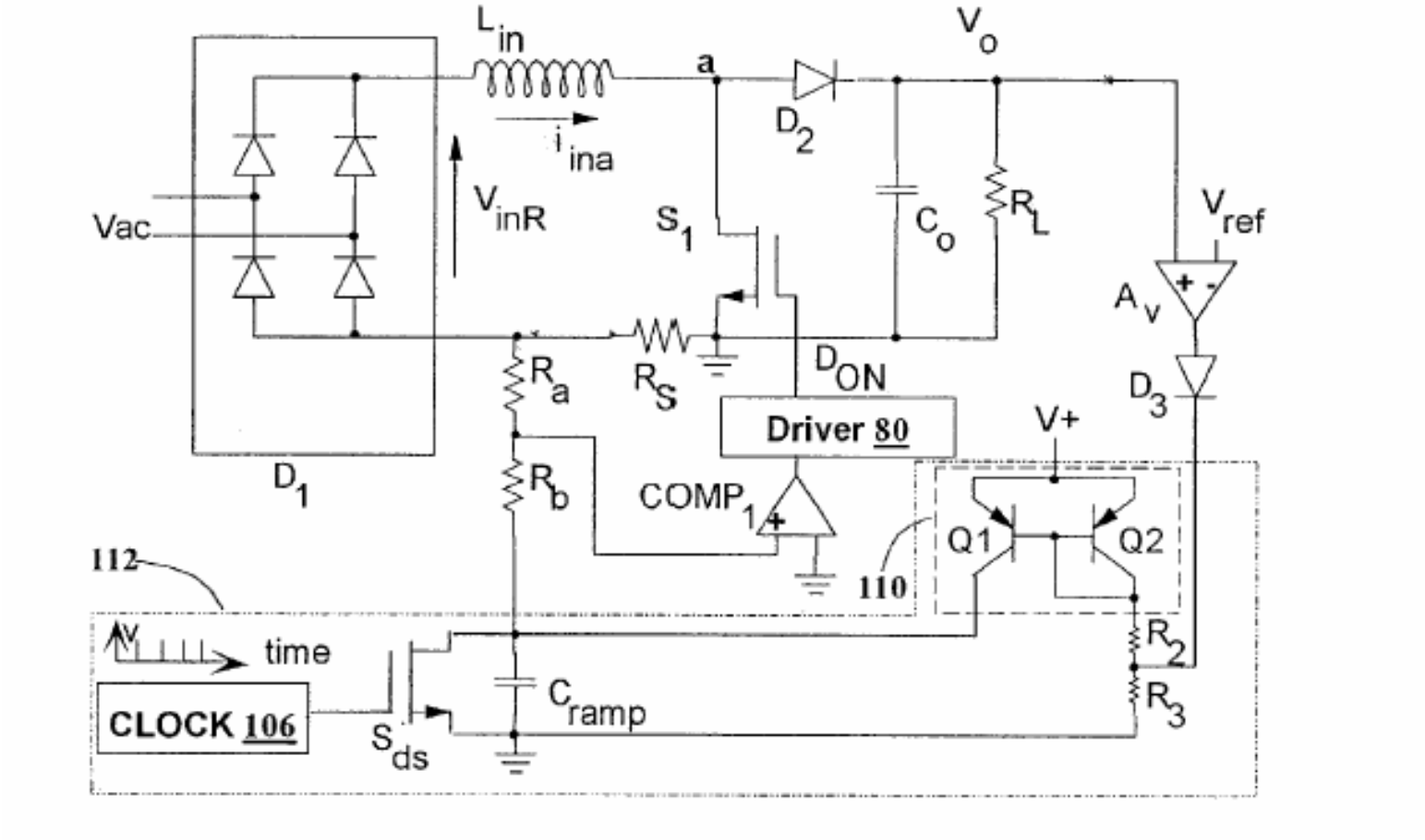
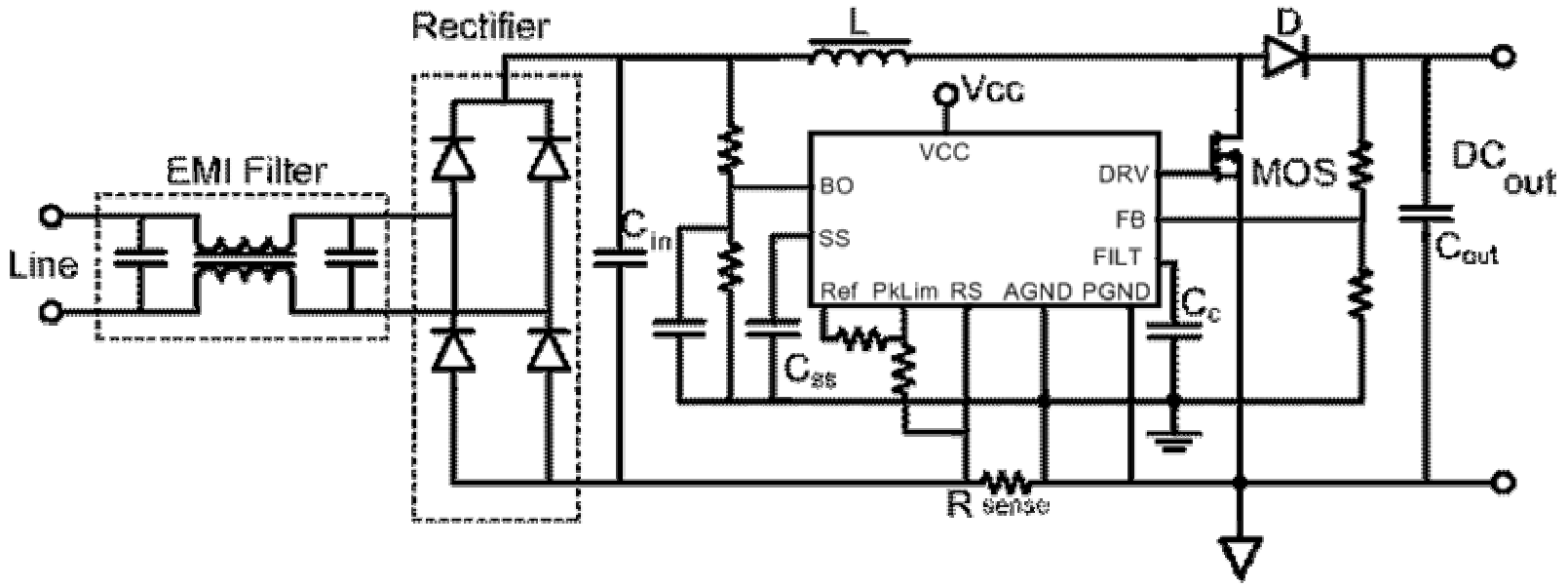
(57) **ABSTRACT**

A controller for a PWM converter. The low frequency input impedance is an important parameter of PWM converters. In active power factor correction schemes, this impedance needs to resistive in order to keep the power factor near unity. The controller of the present invention will force the input terminals of a PWM converter, and in particular that of a Boost converter, to look resistive, or with a reactive component as desired. The advantages of the controller according to the present invention are simplicity, low cost, robustness and the fact that it does not require an analog multiplier and does not require sensing the input voltage.

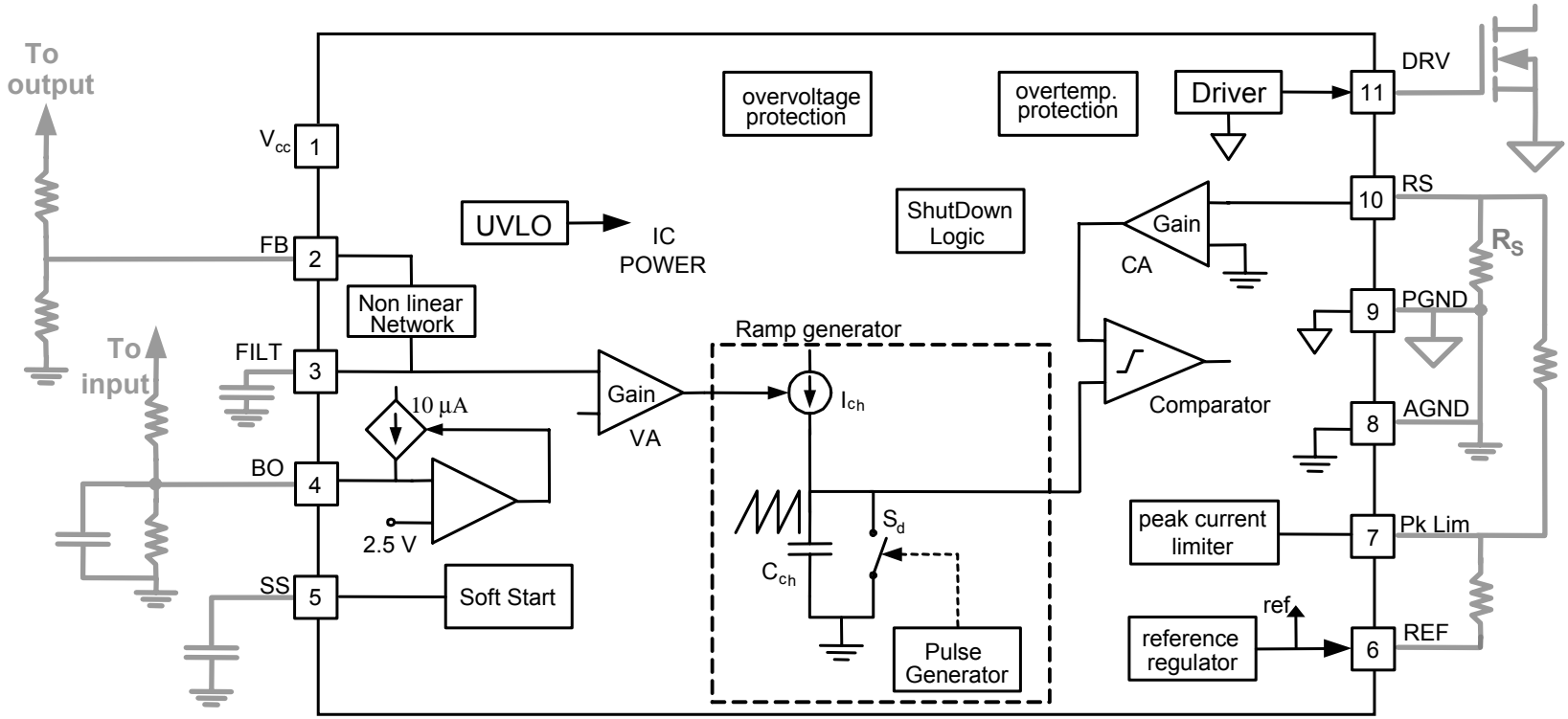
10 Claims, 3 Drawing Sheets


L in
a
V o
i ina
D 2
V inR
Vac
S 1
C o
R L
V ref
A v
R a
R S
D ON
D 3
Driver 80
V+
D 1
R b
COMP 1
Q1
Q2
112
110
time
R 2
R 3
CLOCK 106
S ds
C ramp

Controller Based PFC Stage



Block Diagram



Pinning

Vcc: Auxiliary power supply input.

FB: Feedback input.

FILT: Error amplifier's noninverting input. Compensation capacitor will be connected between this pin and signal ground pin.

Pinning

BO: Brownout input. Used to detect input line failure. Provided with hysteresis.

SS: Soft start input. Internal soft start circuitry provides 100mS delay at turn on. Turn on delay can be prolonged by connecting external capacitor between this pin and analog ground pin.

REF: Voltage reference output.

Pinning

PKLMT: Current peak limit input. The threshold for current peak limit comparator is 0V.

AGND: Serves as a signal ground and reference point for all the input circuitries.

PGND: Return terminal for high currents. Internally connected to the driver stage of the controller.

Pinning

RS: Current sense input. An external sense resistor will be connected between this pin and ground pin.

DRV: Output of the controller. Will drive an external MOSFET. The output stage of driver will not be damaged when connected to the input capacitance of the power MOSFET.

Block Description

PWM

- Duty Cycle: 0% ÷ 97%

Oscillator

- Operating frequency is in range of 60kHz÷70kHz
- Timing capacitor is internal

Ramp Generator

- Controlled by transconductance amplifier

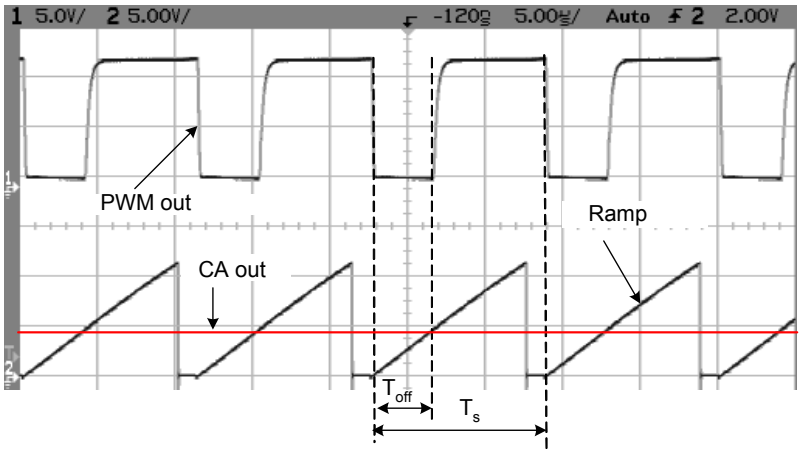
- Ramp capacitor is internal

- The range of ramp current source is at least 1:200

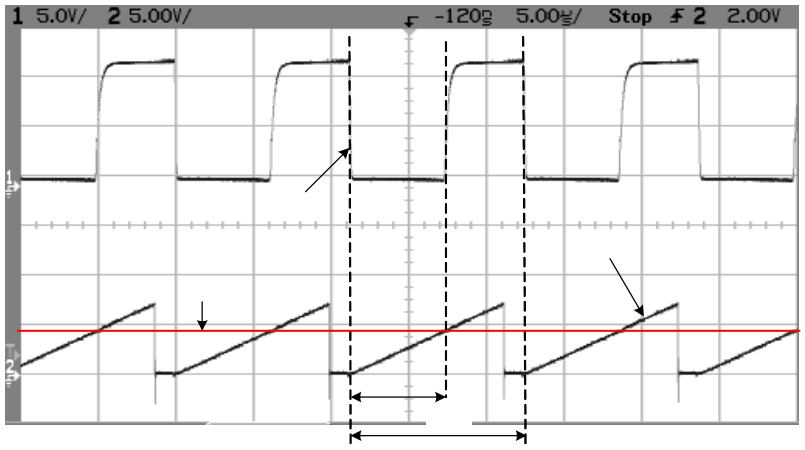
- The high state of the voltage amplifier will be higher then the maximum ramp voltage

- If the ramp reaches the maximum value before the end of the switching cycle it will be clamped to its maximum value until the ramp capacitor is discharged

Comparator



High ramp



Low ramp

- Comparator response needs to be carefully designed
- Duty cycle needs to be linear even at very low ramp situations (1:200 of maximum ramp value)

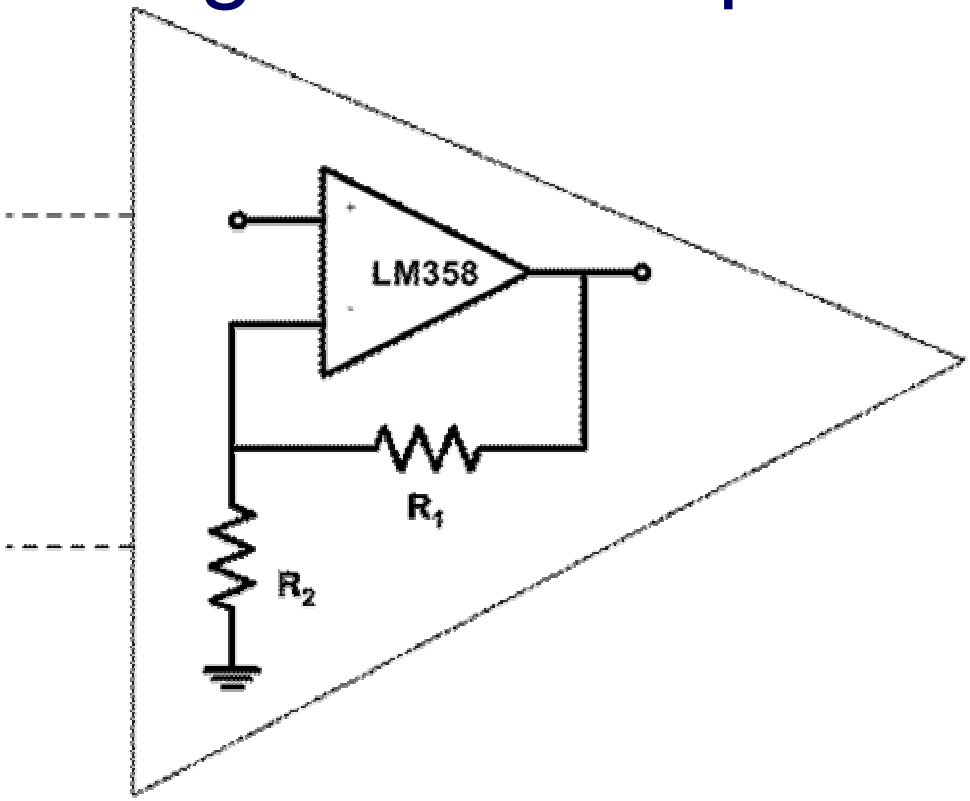
Soft Start

- Limits Duty Cycle at turn on
- Turn on time is about 100mS

Reference Regulator

- Accuracy of reference voltage is at least 1%

Voltage Error Amplifier



Present Implementation

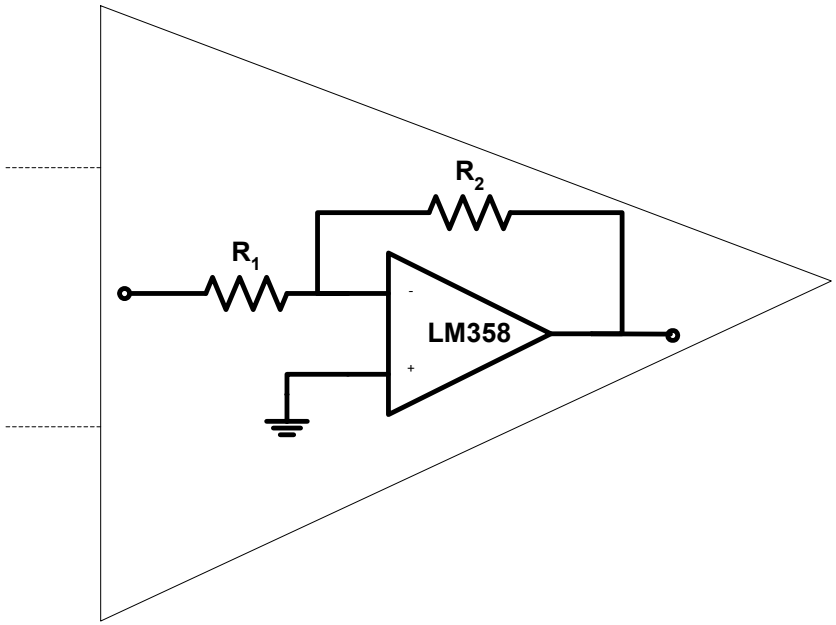
Voltage Error Amplifier

- Fixed gain amplifier

- Closed loop gain: 30dB (present implementation)

- Closed loop bandwidth: 30kHz (present implementation)

Current Amplifier



Present Implementation

Current Amplifier

- Minimum output voltage is zero
- Maximum output voltage is higher then maximum ramp voltage
- Able sensing negative voltages (assumed -1V max. operating)
- Total voltage error at the input (input offset voltage + bias current times resistor) to be less than 3mV
- Fixed gain amplifier
- Closed loop gain: 25dB (present implementation)
- Closed loop bandwidth: 6kHz (present implementation)

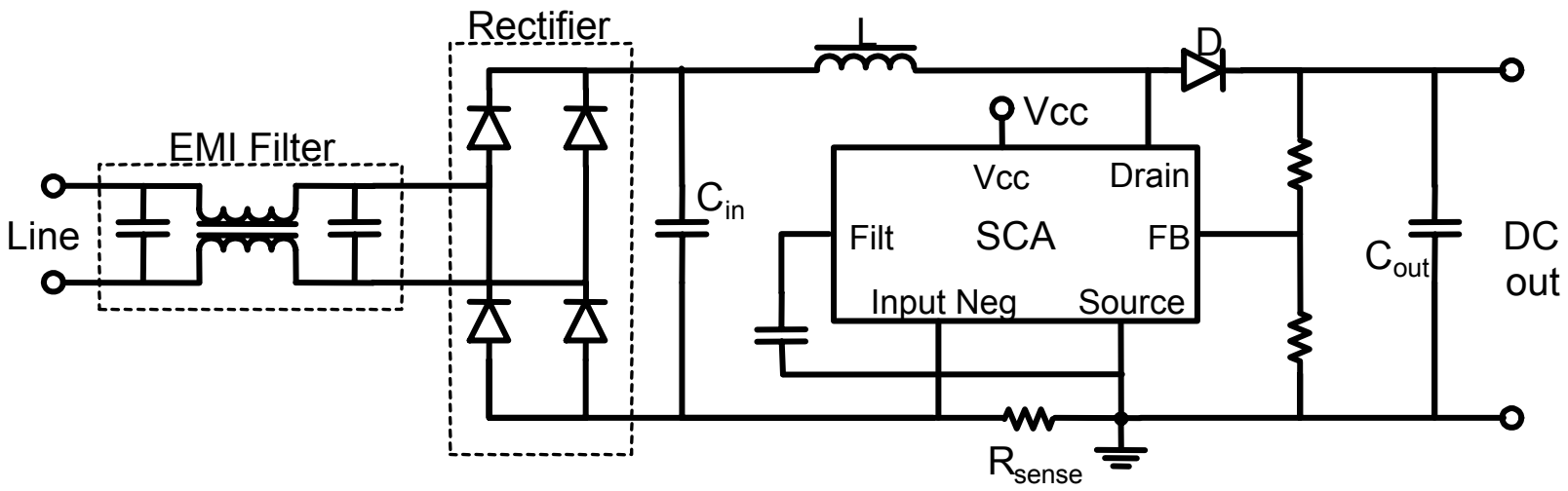
Supply current section

- Start up current doesn't exceed 200μA

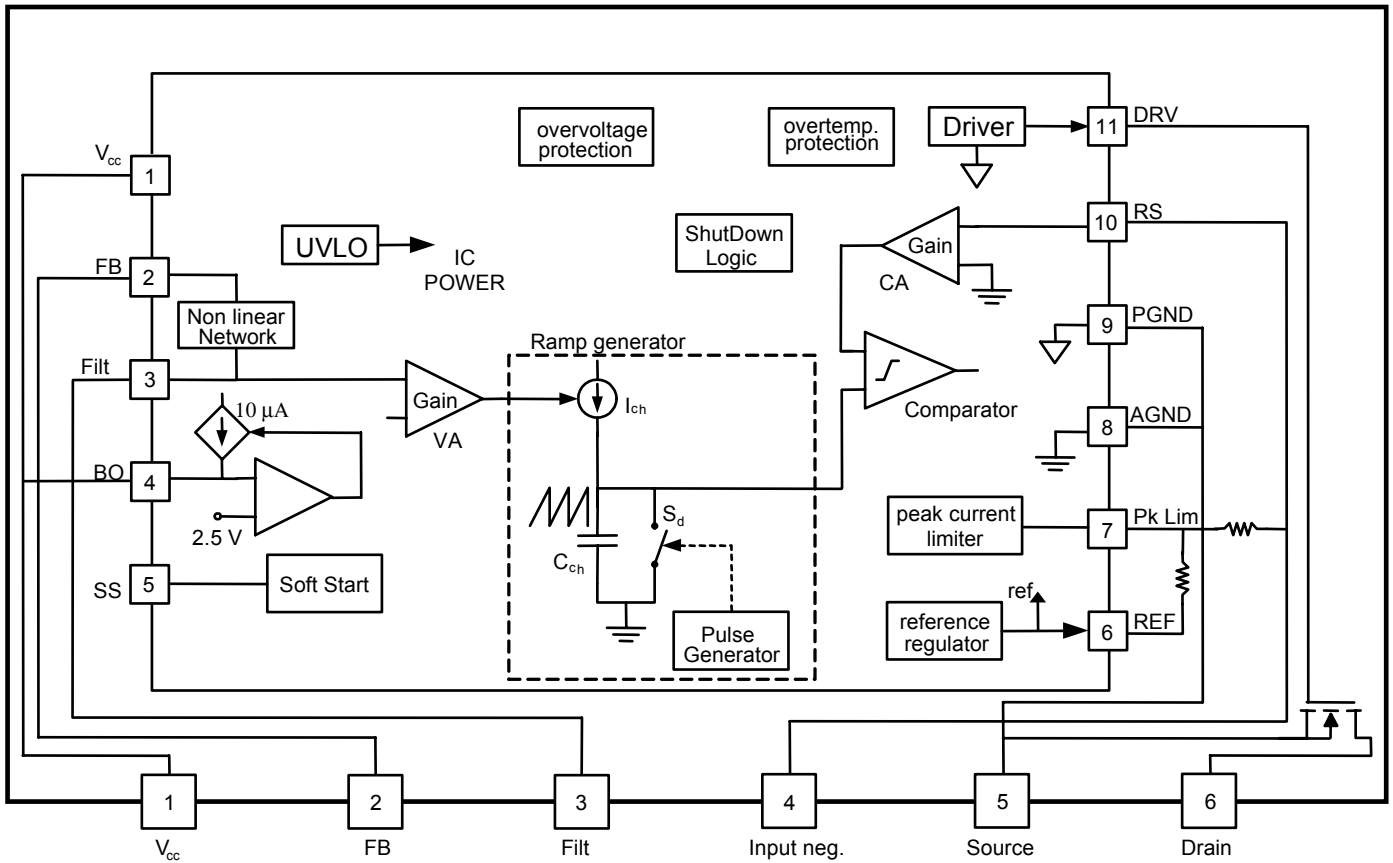
Driver Section

- Peak current is 1500mA
- Will not be damaged when connected directly to the input capacitance of power MOSFET

SCA based PFC stage



SCA Description



Auxiliary supply input	Feedback input	Comp. input	Negative power terminal input	Source of power switch	Drain of power switch

SCA Description

Key Features

- Based on controller + MOSFET

- Main switch:
  - Maximum voltage: 500V
  - Maximum current: 7A
  - Continuous current: 3.5A
  - Switching frequency: 100kHz

- Package: TO-220, TO-247 or similar

Thank you for your attention