Four Key Steps to Design a Continuous Conduction Mode PFC Stage Using the NCP1653

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APPLICATION NOTE

This paper proposes the key steps to rapidly design a Continuous Conduction Mode (CCM) PFC stage driven by the NCP1653. The process is illustrated by the following practical application:

- ***Maximum output power: 300 W***
- ***Input voltage range: from 90 Vrms to 265 Vrms***
- ***Regulation output voltage: 390 V***
- ***Switching frequency: 100 kHz***

INTRODUCTION

The NCP1653 is a controller for Continuous Conduction Mode (CCM) Power Factor Correction step−up pre−converters. It controls the power switch conduction time (PWM) in a fixed frequency mode and in dependence on the instantaneous coil current.

Housed in a DIP8 or SO8 package, the circuit minimizes the number of external components and drastically simplifies the PFC implementation. It also integrates high safety protection features that make the NCP1653 a driver for robust and compact PFC stages like an effective input power runaway clamping circuitry.

Generally, the NCP1653 is an ideal candidate in systems where cost−effectiveness, reliability and high power factor are the key parameters. It incorporates all the necessary features to build a compact and rugged PFC stage:

- **Compactness and Flexibility:** Easy to implement, the NCP1653 yields near−unity power factor in a simple and robust manner. Despite the low external components count it requires, the circuit sacrifices neither performance nor flexibility. Instead, by simply adjusting an external resistor, you can even choose to have the circuit operated in traditional or follower boost mode [(1)].
- **Low Consumption and Shutdown Capability:** The NCP1653 particularly, minimizes its consumptions during the startup phase and in shutdown mode. Hence, the PFC stage losses are extremely low when the circuit is off. This feature helps meet the more stringent standby low power specifications. Grounding the Feedback pin (pin1) forces the NCP1653 in shutdown mode.
- **Safety Protections:** The NCP1653 permanently monitors the input and output voltages, the coil current and the die temperature to protect the system from possible over−stresses. More specifically, the following protections make the PFC stage extremely robust and reliable:
  - **Maximum Current Limit:** The circuit immediately turns off the MOSFET if the coil current exceeds the maximum permissible level. The NCP1653 also prevents any turn on of the power switch as long as the coil current is not below this limit. This feature protects the PFC stage during the startup phase when large in−rush currents charge the output capacitor.
  - **Undervoltage Protection/Shutdown:** The circuit keeps in shutdown mode as long as the feedback current indicates that the output voltage is lower than 8% its regulation level. In this case, the NCP1653 consumption is very low (<50 μA). This feature protects the PFC stage from starting operation in case of too low AC line conditions or of a failure in the feedback network (e.g., bad connection).
  - **Overvoltage Protection:** Given the low bandwidth of the regulation block, PFC stages may exhibit dangerous output voltage overshoots because of abrupt load or input voltage variations (e.g. at startup). Overvoltage Protection (OVP) turns off the Power Switch as soon as V_{out} exceeds the OVP threshold (107% of the regulation level).

[(1)]The “Follower Boost” mode makes the pre−converter output voltage stabilize at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the difference between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage (refer to MC33260 and NCP1653 data sheet at www.onsemi.com).

- **Over−Power Limitation:** The NCP1653 senses the coil current and the input voltage and based on this information, the circuit is able to detect excessive power levels. In this case, it grounds the regulation block (nonfiltered) output as long as the calculated power keeps too high.
- **Thermal Shutdown:** An internal thermal circuitry forces the power switch off when the junction temperature exceeds 150°C typically. The circuit resumes operation once the temperature drops below about 120°C (30°C hysteresis).

PFC STAGE DIMENSIONING

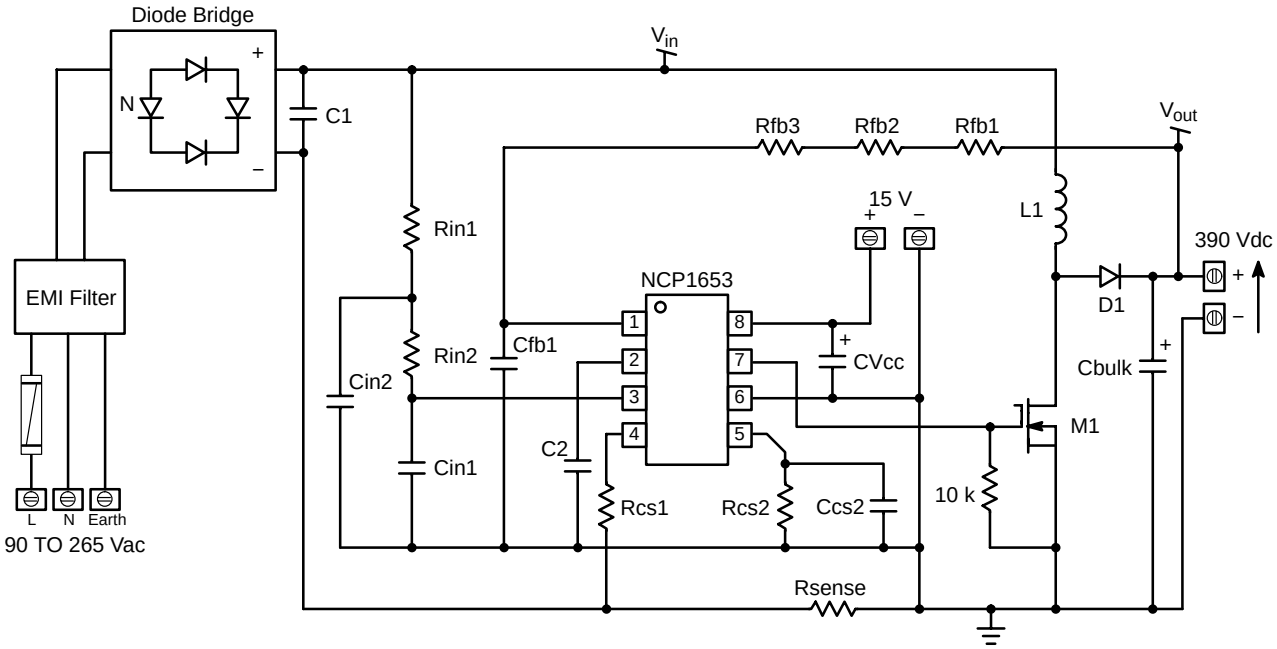

Figure 1. Generic Schematic

Step 1: Power Components Selection

Basically, the coil, the bulk capacitor and the power silicon devices are dimensioned “as usually”, that is, as done with any other CCM PFC. This section does not detail this process, but simply states some key points.

1. Coil Selection

One generally selects the coil to limit the current ripple below a certain pre−determined level, for instance ±15% when the input current is maximum.

The input current amplitude, (Iin), is maximum at low line and high power. Hence, $(Iin)max = \frac{\sqrt{2} * (Pout)max}{\eta * VacLL}$ (eq. 1), where (Pout)max is the maximum output power, η the efficiency and VacLL the AC line lowest level.

Consequently, if we assume a 92% efficiency, our 300 W application leads to the following maximum AC line peak current: $\sqrt{2} * 300/(0.92 * 90)$ that is: 5.1 A.

On the other hand, one could show that at the sinusoid top, the peak−to−peak ripple of the coil current, is given by the following equation: $\frac{\sqrt{2} * Vac}{L * f} * (1 - \frac{\sqrt{2} * Vac}{Vout})$. (eq. 2)

Typically, one targets the peak−to−peak ripple between 10 and 50% of the AC line current maximum amplitude ((Iin)max).

Therefore if we target a ±15 % ripple at low line, the coil inductance (L) is given by the following equation: $\frac{\sqrt{2} * VacLL}{2 * L * f} * (1 - \frac{\sqrt{2} * VacLL}{Vout}) = 15\% * \frac{\sqrt{2} * (Pout)max}{\eta * VacLL}$. (eq. 3)

Hence, the coil inductance is:

$$L = \frac{\eta * VacLL^2}{0.3 * f * (Pout)max} * (1 - \frac{\sqrt{2} * VacLL}{Vout}).$$ (eq. 4)

The combination of 390 V for the output voltage (V_{out}) and 100 kHz for the switching frequency, leads to a coil inductance in the range of 557 μH. In practice, we have chosen 600 μH that more specifically, leads to about a ±14 % ripple.

Finally, if one neglects the switching ripple of the coil current, its rms value equates the rms AC line current. In other words: $(Icoil)rms = \frac{Pout}{\eta * Vac}$. (eq. 5)

The maximum rms current of the coil is then: $((Icoil)rms)max = \frac{(Pout)max}{\eta * VacLL}$. (eq. 6)

The coil specification is then:
- L = 600 μH
- (Icoil)max = 5.8 A (maximum amplitude of the AC line current + ripple)
- (Icoil)rms = 3.7 A

2. Power Silicon Devices

Generally, the diode bridge, the power MOSFET and the output diode will be placed on the same heatsink.

As a rule of the thumb, one can estimate that the heatsink will have to dissipate around:
- 6% of the output power in wide mains applications (92% being generally the targeted minimum efficiency)
- 3% of the output power in European mains applications

Among the sources of losses that contribute to this heating, one can list:
- The diodes bridge conduction losses that can be estimated by the following equation:

$$Pbridge = \frac{4 * \sqrt{2}}{\pi} * \frac{Vf}{VacLL} * \frac{Pout}{\eta} \approx 1.8 * \frac{Vf}{VacLL} * \frac{Pout}{\eta} \quad \text{(eq. 7)}$$

where Vf is the forward voltage of the bridge diodes.
- The MOSFET conduction losses, that if one neglects the current ripple, are given by:

$$(pon)max = R_{DSON} * \left(\frac{< Pin > max}{VacLL}\right)^2 * \left(1 - \frac{8 * \sqrt{2} * VacLL}{3 * \pi * Vout}\right) \quad \text{(eq. 8)}$$

- The output diode conduction losses: (Iout * Vf), where Iout is the load current and Vf the diode forward voltage. The maximum output current being nearly 0.75 A (300 W/390 V), the diode conduction losses are in the range of 0.75 W (assuming Vf = 1.0 V).

In our case, we have:
- Pbridge = 6.6 W, assuming that Vf is 1.0 V.
- (pon)max = 9.5 * R_{DSon}. In our application, a low R_{DSon} MOSFET (0.19 Ω) is implemented to avoid excessive MOSFET losses. Assuming that R_{DSon} doubles at the high temperatures, the maximum conduction losses are about 4.0 W.
- Pdiode = 0.75 W

The diode and MOSFET switching losses are highly dependent on the diode choice, on the MOSFET drive speed and on the possible presence of some snubbering circuitry. Hence, their prediction is a tough and inaccurate exercise that will not be made in this paper.

Instead, they are just assumed to be part of the power budget initially specified for the heatsink (6% of Pout in our case). Experimental tests will ensure that the estimation is correct.

3. Output Bulk Capacitor

Unless another constraint is specified (the hold−up time for instance), the main criterion when choosing the bulk capacitance is the maximum voltage ripple (100 or 120 Hz ripple exhibited by the bulk voltage[(2)]).

The voltage ripple constraint requires that:

$$Cbulk > \frac{Pout}{(\delta Vpk - pk)_{max} * \varpi * Vout} \quad \text{(eq. 9)}$$

where $(\delta Vpk-pk)_{max}$ is the maximum permissible peak−to−peak voltage ripple and ω is the AC line angular frequency. In our application, let's allow a voltage ripple of ±3.5% ($(\delta Vpk-pk)_{max}$ = 7% Vout). This requirement leads to the following bulk capacitance:

$$Cbulk > \frac{300}{7\% * 100\,\pi * 390^2} \approx 89.7\ \mu F \quad \text{(eq. 10)}$$

100 μF is the closest higher normalized value.

Hold−up Time Requirement:

If some hold−time requirement was specified, this would lead to the following additional constraint: $Cbulk > \frac{2 * Pout * t_{HOLD}}{(Vout1^2 - Vout2^2)}$, where Vout1 is the nominal output voltage (390 V), Vout2 is the minimum acceptable level of Vout and t_{HOLD} is the hold−up time. t_{HOLD} = 10 ms and Vout2 = 300 V lead to: Cbulk > 96.6 μF.

With this specification, 100 μF / 450 V is still a valid choice. However, the calculation is based on the average Vout1 value instead of its minimum level resulting from the 100 or 120 Hz ripple. Hence, 150 μF / 450 V would be a more robust option.

Bulk Capacitor Heating:

It must also be checked that the ESR is low enough to prevent the rms current that flows through it, from overheating the bulk capacitor. This rms current depending on the input impedance of the downstream converter, is not computed here. One simple solution consists of experimentally measuring it in the worst case: low line, high power. In a first approach, you can rapidly estimate its magnitude by making a simulation (refer to www.onsemi.com to download our IsSpice or PSpice NCP1653 model).

[(2)]The input current and voltage being sinusoidal, PFC stages deliver a squared sinusoidal power that matches the load power demand in average only. When the power fed to the load is lower than the load demand, the output capacitor discharges while it charges when the supplied power exceeds the load consumption. As a consequence, the output voltage exhibits a ripple (e.g., 100 Hz ripple in Europe or 120 Hz in USA) that is inherent to the PFC function.

Step 2: Feedback Arrangement

As shown by Figure 1, the feedback arrangement consists of:

- A filtering capacitor to avoid that some switching noise may be injected into pin1. A 1 nF capacitor is traditionally implemented.
- A resistor connected between the output voltage rail and pin1 to provide the circuit with a feedback current proportional to Vout. In practice, one generally implements two or three resistors for safety considerations (see Figure 1, given that Vout is a high voltage, an accidental shortage of the feedback resistor would destroy the controller. That is why it is better to have several series resistors instead of only one).
- The capacitor C2 (applied to pin2) sets the regulation bandwidth together with the internal 300 kΩ resistor. Choose C2 in the range of 100 nF for an effective filtering of the 100 or 120 Hz ripple.

If (Rfb = Rfb1 + Rfb2 + Rfb3), the regulation output voltage is given by:

$$Vout = Vpin1 + (R_{FB} * Iref) \quad \text{(eq. 11)}$$

where:

- Vpin1 is the pin1 voltage (about 2 V)
- R_{FB} is the total feedback resistor placed between Vout and pin1
- Iref is the internal current reference (200 μA)

To regulate the output voltage to equate 390 V, one must then select the following R_{FB} resistance:

$$R_{FB} = \frac{390\ V - 2\ V}{200\ \mu A} = 1.94\ M\Omega \quad \text{(eq. 12)}$$

One can approximately obtain a 1.94 MΩ resistance by implementing: (Rfb1 = Rfb2 = 680 kΩ) and (Rfb3 = 560 kΩ). These normalized values precisely give: (Rfb = 1.92 MΩ) that is: 386 V as the regulation level, which is acceptable.

Finally:

Rfb1	Rfb2	Rfb3	Cfb1	C2
680 kΩ	680 kΩ	560 kΩ	1 nF	100 nF

Step 3: Input Voltage Sensing

The NCP1653 monitors the input voltage (Vin − rectified AC line sinusoid). Practically, pin3 is designed to sink a current that is proportional to the Vin average value. This current information is mainly used by the over−power limitation block. For a proper tuning of this protection, the input sensing network must force a constant 15 μA current into Pin 3, when the AC line is at its lowest level.

In other words, the input voltage sensing circuitry must be designed so that (Ipin3 = 15 μA) when (Vac = VacLL) and where VacLL is the AC line lowest level.

Hence, as portrayed by Figure 1, the Vin sensing arrangement consists of:

- An (optional) filtering capacitor Cin1 that can be placed between pin3 and ground to protect the pin from possible surrounding noise. It should be in the range of 1 nF.
- A set of two resistors Rin1 and Rin2 dimensioned to adjust the pin3 current.
- A capacitor Cin2 that forms a low pass filter together with Rin2, able to effectively filter the AC line ripple (Vin is a rectified sinusoid). A time constant in the range of 50 ms should be targeted to make the pin3 current substantially constant and proportional to the mean input voltage:

$$Ipin3 = \frac{< Vin > - Vpin3}{Rin1 + Rin2} \quad \text{(eq. 13)}$$

where <Vin> is the average input voltage and Vpin3 is the pin3 voltage (Vpin3 = 4 V).

Vin being a rectified sinusoid, $< Vin > = \frac{2 * \sqrt{2} * Vac}{\pi}$ and $Ipin3 = \frac{\frac{2*\sqrt{2}*Vac}{\pi} - Vpin3}{Rin1 + Rin2}$.

The sensing network must be designed so that: (Ipin3 = 15 μA) when (Vac = VacLL), hence:

$$Rin1 + Rin2 \cong \frac{(2 * \sqrt{2} * VacLL) - 4\ V}{15\ \mu A}$$

$$\approx (60021 * VacLL) - 266667 \quad \text{(eq. 14)}$$

In our case, VacLL = 90 V.

Hence: $Rin1 + Rin2 \approx 5.13\ M\Omega$.

Let's choose:

Rin1 = 4.7 MΩ

Rin2 = 470 kΩ

As aforementioned, the time constant (Rin2 * Cin2) should be in the range of 50 ms, then: $Cin2 = \frac{50\ ms}{470\ k\Omega} \approx 106\ nF$. Let's select: $Cin2 = \frac{100\ nF}{63\ V}$.

Note: Rin2 should be selected small compared to Rin1 so that a small portion of the input voltage applies across Cin1. In our case, the ratio (Rin1/Rin2 = 10) allows the use of a 50 or 63 V ceramic capacitor for Cin1.

Finally:

Rin1	Rin2	Cin1	Cin2
4.7 MΩ	470 kΩ	1 nF	100 nF

Step 4: Current Sense Network

The current sense circuitry consists of:

- A current sensing resistor Rsense.
- A resistor Rcs1 that sets the current limit threshold.
- A resistor Rcs2 that adjusts the PFC stage power capability.
- A capacitor Ccs2. Pin3 sources a current that is proportional to the coil current. Ccs2 must filter the coil current ripple so that Ipin3 is actually proportional to the input current.

⇒ Rsense

You are free to implement the current sense resistor (Rsense) of your choice. Practically, losses considerations dictate its value.

If one neglects the ripple current, maximum Rsense losses can be estimated by the following equation:

$$(pRsense)max = Rsense * \left(\frac{(Pout)max}{\eta * VacLL}\right)2 \quad \text{(eq. 15)}$$

As a rule of the thumb, one can choose Rsense so that its dissipation does not exceed 0.5% of (Pout)max. This criterion leads to:

$$Rsense \leq 0.005 * \frac{(\eta * VacLL)^2}{(Pout)max} \quad \text{(eq. 16)}$$

In our application, solving of the precedent equation gives: $Rsense \leq 114\ m\Omega$.

Hence, Rsense = 0.1 Ω that would spend about 1.4 W, is an acceptable choice.

⇒ Rcs1

Simply select Rcs1 in order to set the desired overcurrent limit:

$$Rcs1 = \frac{Rsense * (Icoil)max}{Iref} \quad \text{(eq. 17)}$$

where:

(Icoil)max is the maximum coil current

Iref is the internal current source (200 μA)

As step1 indicates that the maximum coil current is 5.8 A and as Rsense = 0.1 Ω is selected, Rcs1 is: $\frac{0.1\ \Omega * 5.8\ A}{200\ \mu A}$ that is 2.9 kΩ.

⇒ Rcs1 and Ccs2

Rcs2 adjusts the maximum power the PFC stage can supply given the chosen output voltage level. By choosing Rcs2 high enough, you can force the “Follower Boost” operation[3]. Use the following equation to select Rcs2:

$$Rcs2 = \frac{\eta * \pi * Rcs1 * Rin * Iref * Vref}{2 * \sqrt{2} * Rsense * (Pout)max * VoutLL} * VacLL \quad \text{(eq. 18)}$$

where:

- Rin is the input voltage sensing global resistance (Rin = Rin1 + Rin2)
- Iref is the internal current reference (200 μA)
- Vref is the internal voltage reference (2.5 V)
- VacLL is the lowest level of the AC line rms voltage
- (Pout)max is the maximum output power
- η is the efficiency @ VacLL and (Pout)max
- VoutLL is the output voltage corresponding to VacLL in full load conditions. In traditional mode, VoutLL is the targeted regulation level (390 V in general). In Follower Boost, you can choose a lower value.

Our application is a traditional one (constant output voltage). Hence, VoutLL equates 390 V and Rcs2 is:

$$\frac{0.92 * \pi * 2.85\ k\Omega * 5.17\ M\Omega * 200\ \mu A * 2.5V}{2 * \sqrt{2} * 0.1\ \Omega * 300\ W * 390\ V} * 90\ V$$

$$= 58\ k\Omega \quad \text{(eq. 19)}$$

Let’s take a normalized 56 kΩ resistor.

For a correct filtering of the pin3 voltage switching ripple, the time constant (Rcs2 * Ccs2) should be taken in the range of 50 μs. This time constant is large enough to filter the switching ripple and low enough not to distort the low frequency component (that is the 100 or 120 Hz rectified sinusoid).

Hence: $Ccs2 = \frac{50\ \mu s}{Rcs2}$.

In our application this leads to the following Ccs2 value: $Ccs2 = 893\ pF$.

Let’s take Ccs2 = 1 nF.

Finally:

Rsense	Rcs1	Rcs2	Ccs2
0.1 Ω	2.85 kΩ	56 kΩ	1 nF

[3]The “Follower Boost” mode makes the pre−converter output voltage stabilize at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the difference between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage (refer to MC33260 and NCP1653 data sheet at www.onsemi.com).

Summary

Steps	Components	Formula	300 W Application
Step 1: Coil Inductance, Bulk Capacitor and Power Silicon	Select the maximum switching peak−to−peak ripple of the coil current	Choose a value between 20 and 50%. $\rho = \frac{(\Delta Icoil)_{pk-pk}}{(Icoil)max}$	ρ = 28 %
	Coil Inductance (L)	$L = \frac{\eta * VacLL^2}{\rho * f * (Pout)max} * \left(1 - \frac{\sqrt{2} * VacLL}{Vout}\right)$	L = 600 μH
	Maximum coil current	$(Icoil)max = \frac{\sqrt{2} * \left(1 + \frac{\rho}{2}\right) * (Pout)max}{\eta * VacLL}$	(Icoil)max = 5.8 A
	Max rms coil current	$((Icoil)rms)max = \frac{(Pout)max}{\eta * VacLL}$	((Icoil)rms)max = 3.7 A
	Bulk Capacitor Value	$Cbulk > \frac{300}{7\% * 100\pi * 390^2} \approx 89.7\ \mu F$ (hold−up time and rms current considerations being not taken into account)	100 μF / 450 V
Step 2: Feedback Arrangement	Rfb1 + Rfb2 + Rfb3	$Rfb1 + Rfb2 + Rfb3 = \frac{Vout - 4\ V}{200\ \mu A}$	Rfb1 = 680 kΩ Rfb2 = 680 kΩ Rfb3 = 560 kΩ
	Cfb1	Cfb1 = 1 nF	Cfb1 = 1 nF
	C2	C2 = 100 nF	C2 = 100 nF
Step 3: Input Voltage Sensing	Rin1 and Rin2	$Rin = \frac{\left(\frac{2*\sqrt{2}*VacLL}{\pi}\right) - 4\ V}{15\ \mu A}$ (Rin = Rin1 + Rin2) Choose: Rin1 ≈ 10 * Rin2	Rin1 = 4.7 MΩ Rin2 = 470 kΩ
	Cin1	Cin1 = 1 nF	Cin1 = 1 nF
	Cin2	$Cin2 = \frac{50\ ms}{Rin2}$	Cin2 = 100 nF / 63 V
Step 4: Current Sense Network	Rsense	Choose Rsense so that its dissipation keeps reasonable (e.g., select Rsense so that pRsense is less than 0/5% * (Pout)max). $Rsense \le 0.5\% * \frac{(\eta * VacLL)^2}{(Pout)max}$	Rsense = 0.1 Ω / 3 W
	Rcs1	$Rcs1 = \frac{Rsense * (Icoil)max}{200\ \mu A}$	Rcs1 = 2.85 kΩ
	Rcs2	$Rcs2 = k * \frac{\eta * Rcs1 * (Rin1 + Rin2) * VacLL}{Rsense * (Pout)max * VoutLL}$ where : $k = \frac{250\ \pi}{\sqrt{2}}\ (\mu W)$	Rcs2 = 56 kΩ
	Ccs2	$Ccs2 = \frac{50\ \mu s}{Rcs2}$	Ccs2 = 1 nF

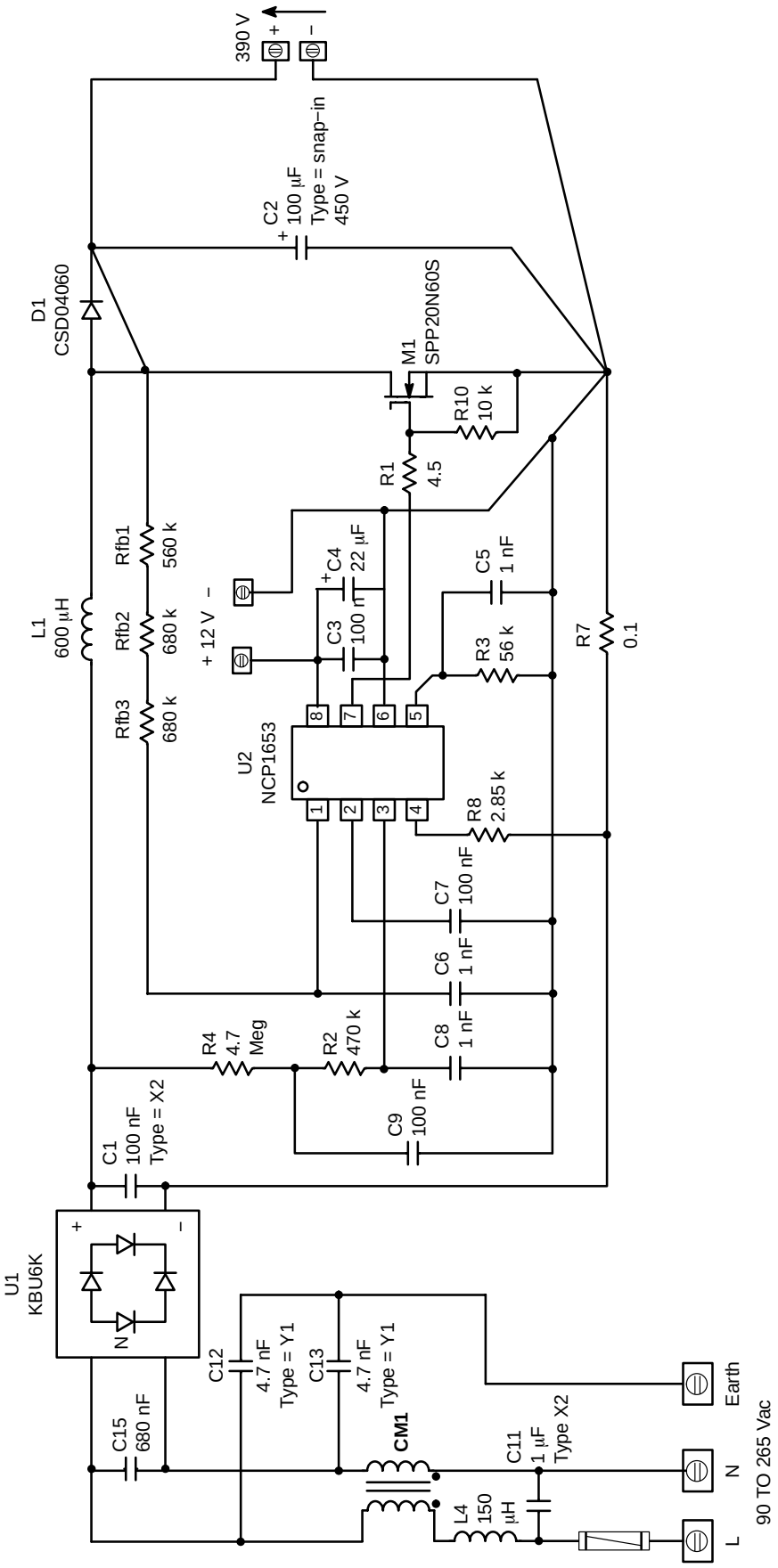

Figure 2. Application Schematic

CONCLUSION

As shown in this paper, the NCP1653 represents a major leap towards compactness and ease of implementation.

As desired, the circuitry of Figure 2 yields high power factor ratios and good efficiency. For more information on this application, please refer to Application Note AND8185/D at www.onsemi.com that gives more details on the practical implementation (BOM, PCB plots…) and on the circuit performance (THD, efficiency…).

An Excel Spreadsheet available at http://www.onsemi.com/pubCollateral/NCP1653%20WORKSHEET..XLS automatically computes the calculations present in this application note.

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