Fast Adaptive DC-DC Conversion Using Dual-Loop One-Cycle Control in Standard Digital CMOS Process

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Abstract – *An adaptive switching converter is presented. It adopts a dual-loop one-cycle control for tight line and load regulation, while retaining fast response and good stability. DC level shifting technique eliminates the use of negative supply voltage and enables both continuous and discontinuous conduction operation. Error correction loops greatly tightens output voltage regulation. Dynamic loss control further improves the efficiency for a wide power range. The converter was fabricated with a standard 0.5μm digital CMOS process. The output voltage can vary from 0.9V to 2.5V, with a tracking speed of less than 14μs/V for a step change of 1.6V. Maximum efficiency of 93.7% is achieved and high efficiency above 75% is retained over an output power of 10mW to 450mW.*

I. Introduction

Dynamic voltage scheduling (DVS), as one of the most effective techniques for power saving, has been widely adopted in many portable applications. A key component in achieving DVS technique is the design of the power supply. Different from traditional fixed-voltage power supplies, on-chip multiple or adaptive power supplies are essential to providing voltages with different levels for scheduling. In some applications, a power supply with multiple outputs [1], [2] are needed to simultaneously power up data-paths that require different speed and power. In other cases, an adaptive power supply is used to change the output voltage according to different loads at different operating modes. This paper explores the design issues of adaptive power supplies.

An adaptive power supply is preferably implemented by a switching converter due to its high efficiency and flexible voltage conversion. Compared to fixed-output counterparts, adaptive converter design is much more challenging. (1) It requires fast transient response to minimize latency and losses when switching between different voltage levels. Tracking speed of less than 100μs is preferred, which is much faster than most state-of-the-art designs [3]-[8]. (2) System stability is more difficult to be maintained under large signal dynamics. In the frequency domain, the dynamics of a switching converter depends on the locations of poles and zeros of the closed-loop gain, which are functions of the output voltage and power. Because large load and voltage level changes occur frequently in an adaptive converter, the poles and zeros vary accordingly, making the design of the compensation network extremely difficult. In the worst case, the system may be unstable. (3) Efficiency, speed and transistor sizing of the converter are difficult to be optimized over a wide voltage and power range. Motivated by the above concerns, a new nonlinear control DC-DC converter is proposed.

II. Converter Architecture

A. One-Cycle Control with Adaptive Output

One-cycle control was first proposed for fixed-output designs [9]. It is based on extracting the voltage information at the input node of the inductor V_x. Any perturbation due to the supply V_g can be corrected within one cycle. Because the converter has no dependence on past cycles, similar to the dead–beat control, it has good stability. Since the output voltage is not fed back, it is an open loop system, and the control equation can be satisfied cycle by cycle without waiting for the output to change [9]. Hence, the change in output is only affected by the dynamics of the power stage and the reference voltage:

$$v_o(t) = L^{-1}\left(\frac{V_{ref}(s)}{1+(L/R)s+LCs^2}\right)$$

where L^{-1} indicates the inverse Laplace transform. The linear relation between V_o and V_{ref} greatly simplifies the control mechanism.

However, all known one-cycle control converters are implemented with discrete components, and their controllers need both V_{dd} and $-V_{ss}$ for biasing. A negative reference voltage is also required. These requirements make the controller difficult to be integrated on a digital CMOS chip and the cost will be high. In addition, the control is open-loop and has poor load regulation.

B. DC Level Shifting Technique

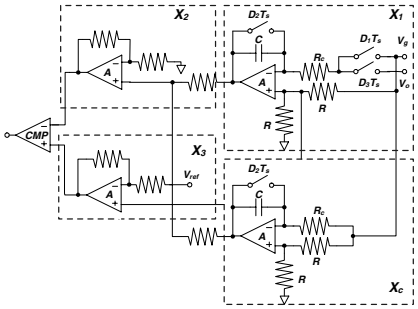

Fig.1 Integrator with DC level shifting for both CCM and DCM

To avoid using negative supply and reference voltages, a DC level shifting circuit is proposed (Fig.1), in which the integrators are referenced to $V_g/2$ instead of ground, and all node voltages are then positive. Thus, standard digital CMOS process can be employed for fabrication. To allow the converter to operate smoothly in both CCM and DCM, an error elimination loop X_c is also embedded to eliminate the integration error in DCM caused by the integrator X_1 [9].

C. Error Correction Loops (ECLs)

The original one-cycle control is an open-loop control and thus has poor load regulation. Error correction loops (ECLs) employing hysteretic control are thus designed. Both the upper and lower error voltage bounds Δ_+ and Δ_- are set in advance. For $V_{ref}-\Delta_- < V_o < V_{ref}+\Delta_+$, the ECLs will be defeated. But if $V_o > V_{ref}+\Delta_+$, the upper bound ECL is selected, issuing an error voltage to reduce the duty ratio of the controller and thus the output voltage, until V_o returns to within the bounds. When $V_o < V_{ref}-\Delta_-$, the lower bound ECL functions in a similar fashion.

D. Dynamic Loss Control (DLC)

Power devices introduce both conduction and switching losses.

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Efficiency of the converter can be enhanced if the sum of the losses is minimized. Dynamic loss control is thus implemented (Fig.2). Since power transistors are built from groups of smaller ones connected in parallel, some of them will be turned off as the output power decreases. By adjusting the equivalent size of the power transistor, high efficiency can thus be maintained dynamically over a much wider output voltage and power range.

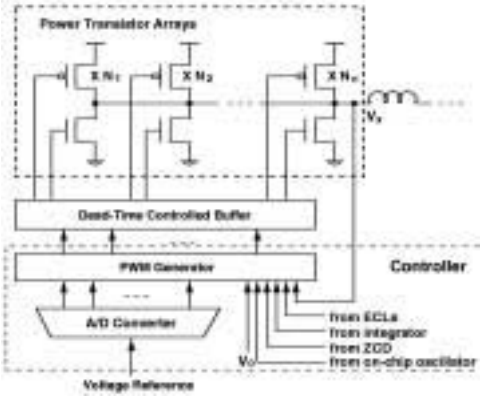

Fig. 2 Block diagram of dynamic loss control.

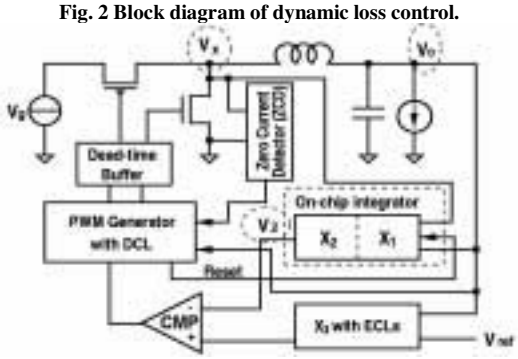

Fig.3 Block diagram of overall system.

E. System Implementation

Fig.3 shows the overall system. Synchronous rectification is adopted for high efficiency. Dead-time buffers avoid large shoot-through currents, and zero current detector (ZCD) helps to prevent inductor current from going negative at the boundary of CCM and DCM.

III. Experimental Results

The converter was fabricated in standard 0.5μm digital CMOS process (Fig.4) and measurement results are shown in Fig.5 to Fig.9. Chip area is 2.31mm^2. Maximum efficiency is 93.7%. With a 100mA load, the ripple voltage is only 10mV. Tracking times for a step-up and step-down change of 1.6V are 19.5μs and 22μs respectively. For a periodic change in the input voltage of 1V, the output variation is controlled to within 100mV, which shows a line regulation comparable to AC-DC converters (Fig.8). Load regulation is less than 50mV/90mA due to the presence of ECLs (Fig.9). Table I compares this work with prior arts, which shows that our converter has the fastest dynamic response and widest output voltage and power range. It is also very area-efficient. The efficiency is excellent since it is larger than 75% over a power range of 450mW.

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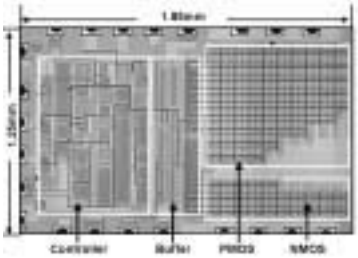

Fig.4 Chip micrograph.

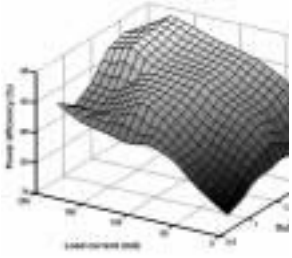

Fig.5 Measured efficiency.

Fig.6 Output voltage and inductor Current

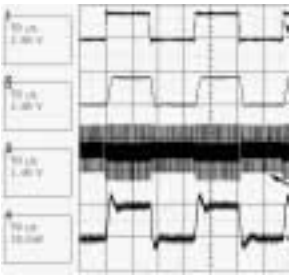

Fig.7 Tracking performance when V_{ref} steps up and down.

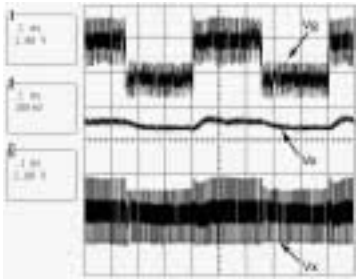

Fig. 8 Line regulation.

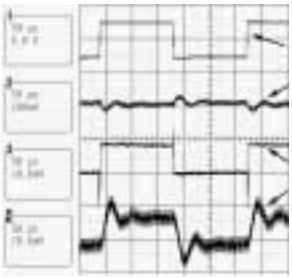

Fig. 9 Load regulation.

Table I Comparison with Prior Arts.

Des.	tracking speed	output range (V)	Volt	η_{max} (%)	P_{max} (mW)	proc (μm)	chip area (mm^2)
[3]	6ms/V	1.5–3.5	5	93	200	0.8	13.66
[4]	1ms/V	1.1–4.4	5	95	1200	0.8	N/A
[5]	180μs/V	1.4–2.5	3	95	300	0.3	4
[6]	80μs/V	1.1–2.3	2.5	95	350	0.25	1.43
[7]	146μs/V	0–0.5	1.2	92	23	0.35, SOI	6
This Work	14μs/V	0.9–2.5	3.3	93.7	450	0.5	2.31