TDA 4863 - Technical Description

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Power Management & Supply

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TDA 4863 - Technical Description

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1 Short Description

The TDA 4863 integrated circuit is the successor IC of TDA 4862. The main improvements are the reduction of the startup current, a reliable gate voltage level at worst case conditions and an improved low-load behavior. Like its predecessor it is able to control a variety of converter topologies which are suited for power factor correction operation. Amongst those, the boost converter is the most widespread one and is also described in this application note. The IC controls the power switch, so that sinusoidal current is taken from the single-phase line supply and a stabilized DC voltage is available at the output. The circuit therefore acts as active harmonic filter and limits the corresponding harmonic currents resulting from the capacitor pulse charge currents of conventional rectification. The power factor which describes the ratio between active and apparent power is almost 1. The IC also compensates possible changes of the line voltage and provides several protection features.

2 Technical Description TDA 4863

2.1 Control Method

The control method of the harmonic filter is based on the physical relationship between current and voltage at the boost converter choke, i.e. $u_L = L\ di_L/dt$, as it is shown in **Figure 1**. This leads to a triangular current waveform which is

$$i_L(t) = L \cdot |V_{in}| \cdot t/T_{on}; \qquad 0 \le t < T_{on} \text{ (T switched on, D switched off)} \quad [1]$$

$$i_L(t) = i_L(T_{on}) - L \cdot (V_{out} - |V_{in}|) \cdot t/T_{off}; T_{on} \le t < T_{on} + T_{off} \text{ (T switched off, D switched on)}$$

while neglecting the voltage $i_D(t).R_{DS(on)}$ of the MOSFET and V_F of the boost diode, respectively.

The transistor T does not switch on again until the current through the boost converter diode D turns zero. This avoids reverse recovery losses in the diode and the triangles of the inductor current i_L are always set immediately one after the other which is well known as discontinuous conduction mode (DCM). Using this control method, the pulse periods (i.e. $T_p = T_{on} + T_{off}$) and the operating pulse frequency f_p of the active harmonic filter change with the input voltage and the load.

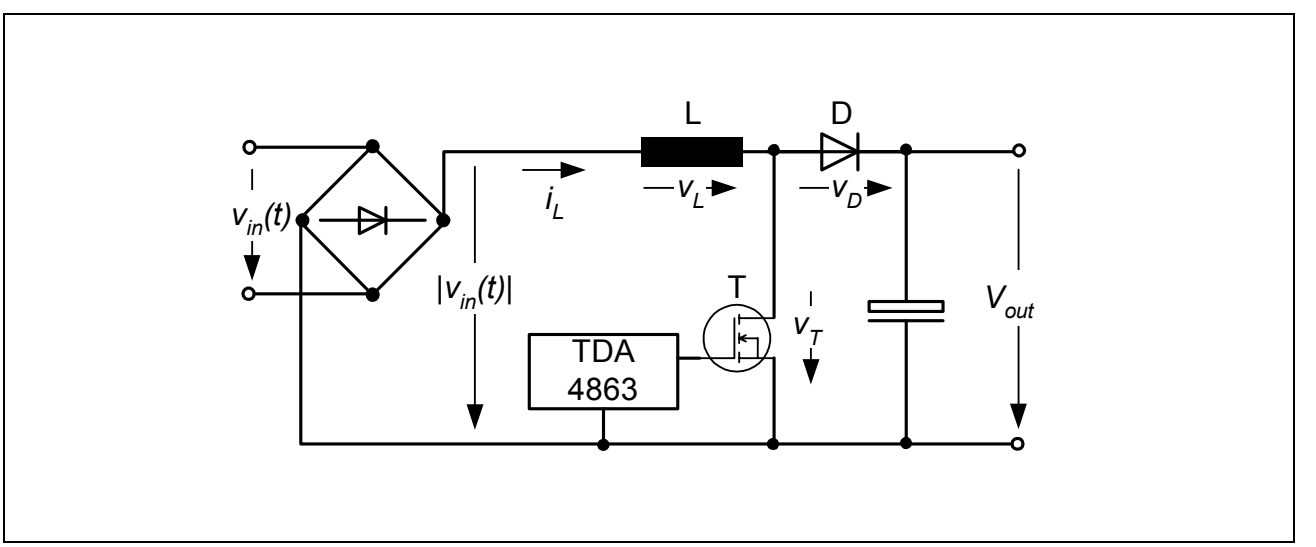

Figure 1 Principle of Boost Converter Used for PFC

The mean input current calculated over a pulse period is exactly half the peak value of the high frequency choke current. According to **Figure 2**, the TDA 4863 modulates them so that they are proportional to an envelope of the sinusoidal line input voltage v_{in} and a sinusoidal line current i_{in} will be drawn after smoothing by means of an RFI suppression filter.

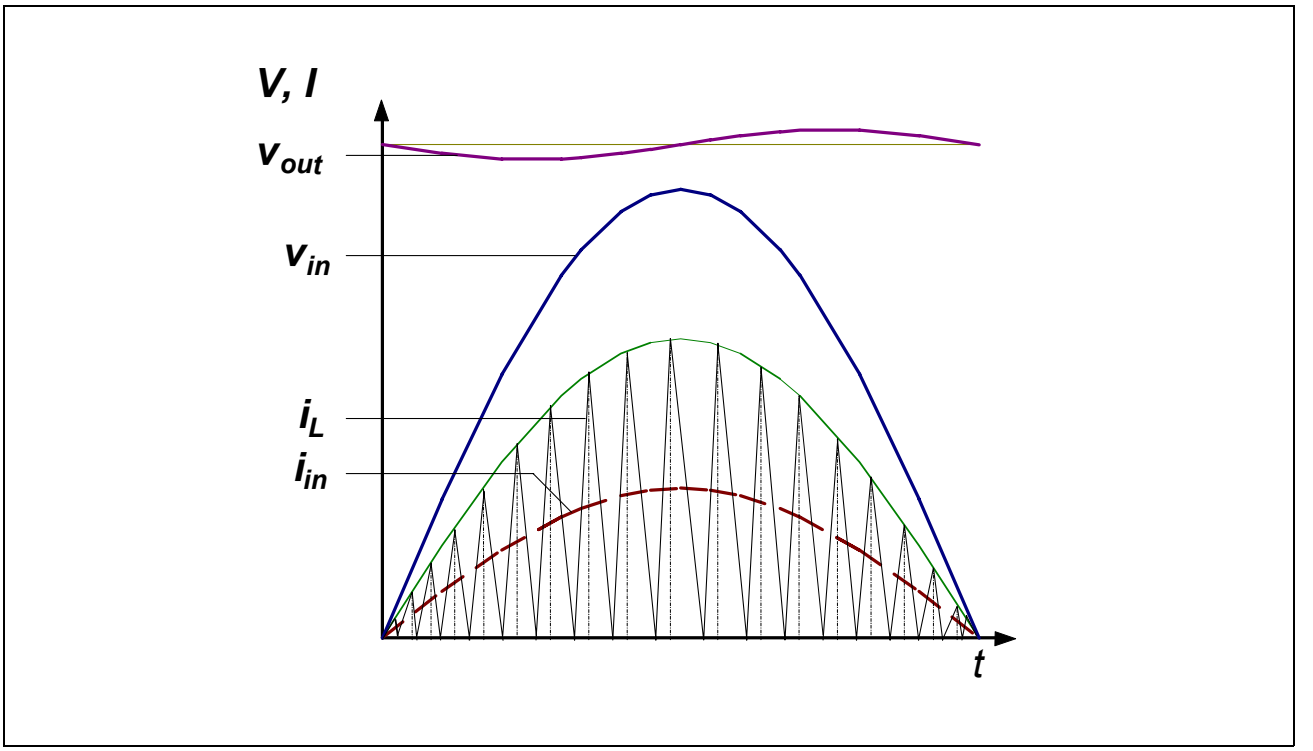

Figure 2 Input Current Shape and Inductor Current in a PFC Boost Converter

2.2 Characteristics

2.2.1 Self-Start

The IC is supplied via resistors either from the rectified mains or from the output voltage during start-up. In this state (V_{CC} < 10 V typ.) the IC consumes a current of less than 100 µA (max.). An turn-on threshold of 12.5 V typically is responsible to set the IC into an operable state. An undervoltage lockout with a turn-off threshold of 10 V typically prevent both the IC and the boost converter to get into a dangerous state of operation. The thresholds are also shown in **Figure 3**. After enabling the gate driver, a startup timer generates a set of pulses for the turn-off flip-flop. This is also done, if the gate driver output remains in low state levels for longer than 150 µs. In order to guarantee safe supply of the IC, the supply voltage pin 8 is internally limited to 20 V to ground. Thus, the IC has all functions necessary for low-loss self-start.

2.2.2 Driver Output

The driver output has been designed to control power MOSFET transistors with a current handling capability of ±500 mA (max.). In order to avoid reverse currents the totem pole driver output is equipped with clamping diodes connected to ground and supply voltage. Additionally, the gate drive is clamped to a maximum value of about 11.5 V typically, which is not shown in **Figure 3**.

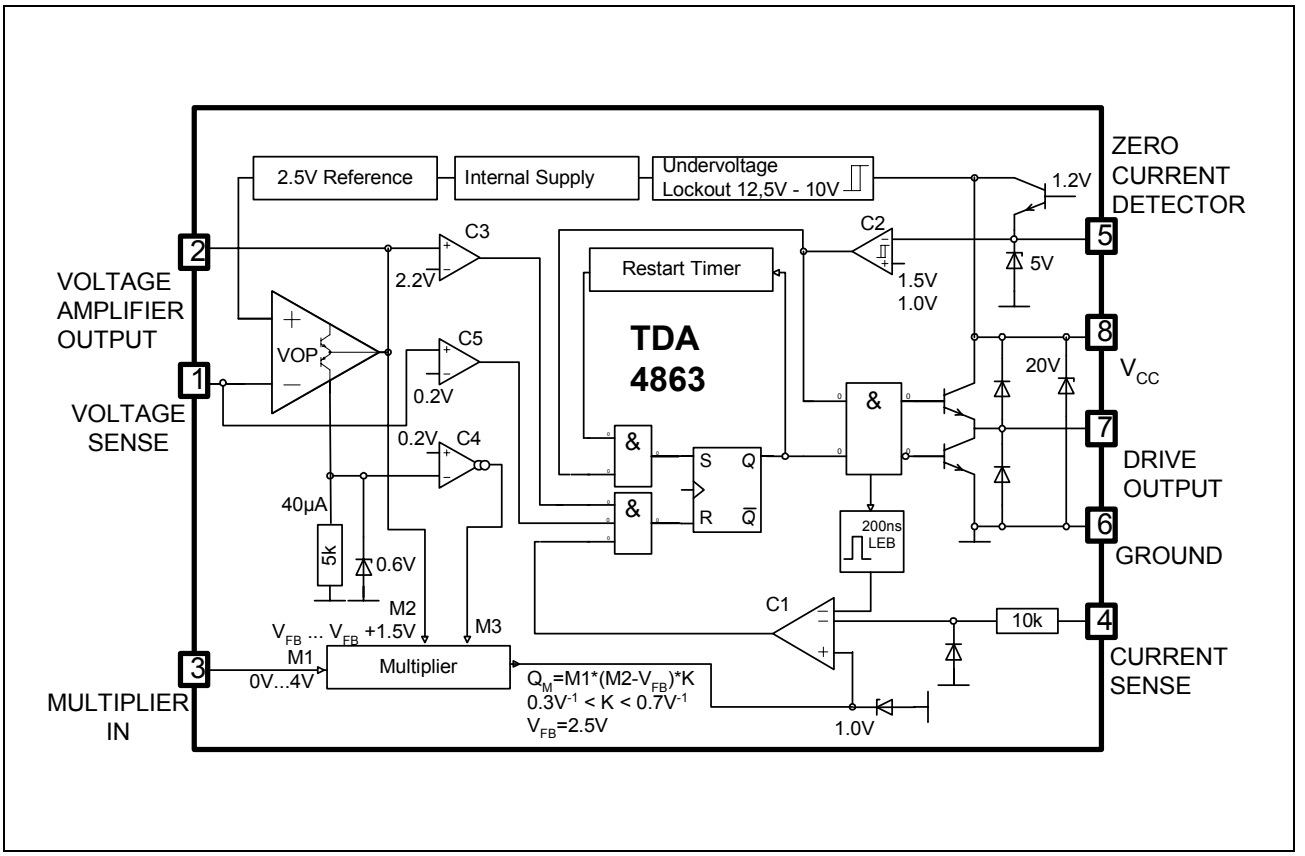

Figure 3 Scheme of TDA 4863

The driver output actively controls LOW levels during standby state using a residual voltage of 1 V at a gate current I_{GT} = 20 mA dissipation current.

2.2.3 Control Amplifier

The control amplifier compares the divided output voltage at its inverting input with a highly accurate reference voltage of 2.5 V at its non-inverting input. The reference has a maximum deviation of less than ±2% over the total temperature range (-40°C < T_J < 150°C). A feedback network is inserted between the amplifier output (pin 2) and its inverting input (pin 1) for the purpose of frequency response compensation. Using only one capacitor as an integral controller causes oscillating transient response, because the boost converter acts as a controlled current source and the storage capacitor at its output delays the phase by almost 90° in no-load and in low-load operation. A compensation network design containing a PI- or a PIT1-controller will lead to much better results. This is also described in the section **"Design Steps" on Page 17**.

The output voltage V_{VAOUT} of the control amplifier ranges from 1.1 V to 5.4 V and can be loaded with a current of 6 mA (source) and 30 mA (sink), respectively and is monitored by comparator C_3 according to **Figure 3**. If the output voltage drops 0.3 V below the reference level of 2.5 V (i.e. reference voltage), the driver output will be blocked directly

via the turn-off flip-flop. This measure guarantees the stability of the output voltage in case of complete no-load operation, without interferences from offset voltages at the multiplier output or at the comparator input.

On the other hand if the voltage sense signal drops below 0.2 V, the IC disables the gate drive. That may occur e.g. when the feedback signal is broken. As soon as the supply voltage crosses the UVLO level, the IC is in off-state and begins another start-up cycle. This is not performed, if the IC is supplied from the subsequent converter, because the supply voltage stays stable and the UVLO level is never reached. Then the IC is continuously off.

The output voltage of the boost converter contains a superimposed AC voltage having twice the mains frequency. Its amplitude depends on the output capacitor and the load and is also fed back via the control amplifier. That causes undesired modulations and increases the total harmonic distortion of the line current drawn. Therefore a bandwidth of the control amplifier is chosen which is considerably lower than twice the mains-frequency. However, the controller then reacts slowlier to sudden load changes which may result in temporary overvoltages or even output breakdowns.

2.2.4 Setting and Limitation of Output Voltage

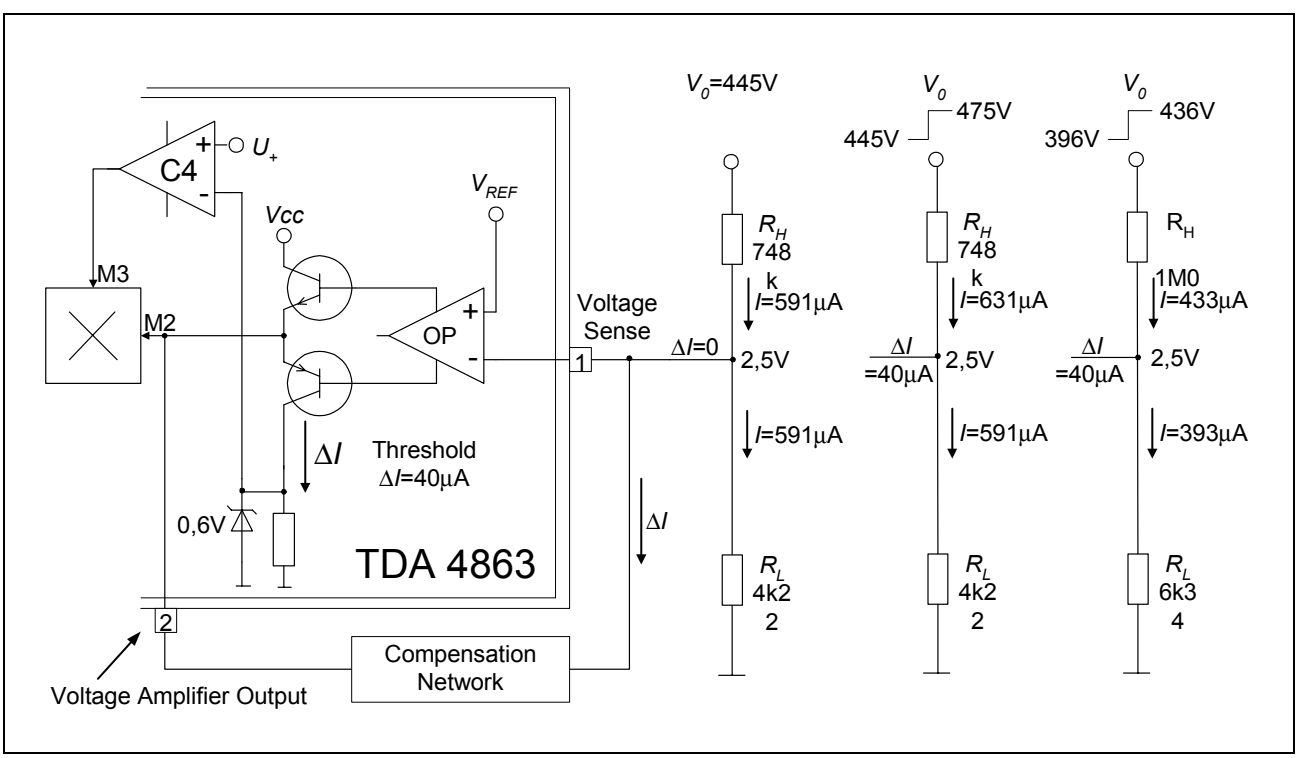

Figure 4 Overvoltage Limitation Dependent on the Output Voltage Divider

The output voltage is set by a voltage divider from V_{out} to GND. The divider should be high ohmic in order to prevent losses. The tap of the divider is set to 2.5 V (i.e. reference voltage, see section **"Design Steps" on Page 17**). But voltage transients or load

rejections may cause output voltage overshoots in boost converter which makes an overvoltage protection necessary, e.g. for the output capacitor. The higher output voltage also forces a higher current through the output voltage divider which causes an increase of the tap potential. The voltage amplifier now tries to compensate this by measuring the current ΔI flowing into the compensation network according to **Figure 5**. ΔI is therefore dependent on the inner resistance of the divider. So is the overvoltage protection limit V_{OVP} because as soon as ΔI exceeds 40 µA the comparator C_4 in **Figure 5** is effective via multiplier input M3. Then the multiplier output is almost linearly reduced until it reaches about 0.1 V at 43 µA. This is shown in diagram 7 of the preliminary datasheet **[1]**. Since the multiplier output simultaneously is the reference voltage of the current comparator its decrease also affects a decrease of the line current drawn. This technique continuously compensates the input current back and avoids uncontrolled oscillations of the line current drawn, as it usually appears with digital measures.

That means, the output voltage divider has to meet the following conditions:

$$V_{out} = V_{ref} \cdot (R_H + R_L)/R_L \text{ and} \quad [2]$$

$$V_{OVP} = V_{ref} + R_4 \cdot (\Delta I + V_{ref}/R_L) \quad [3]$$

Therefore the resistor values are

$$R_L = \frac{V_{ref}}{\Delta I} \cdot \left(\frac{V_{OVP} - V_{out}}{V_{out} + V_{ref}}\right) \quad [4]$$

$$R_H = \left(\frac{V_{OVP} - V_{ref}}{\Delta I + V_{ref}/R_L}\right) \quad [5]$$

with the reference voltage V_{ref} = 2.5 V

The overvoltage control is also guaranteed in those states of operation when the output voltage of the control amplifier reaches its upper limit threshold, because the dissipation current is measured as well. As soon as the output voltage of the control amplifier tends towards the minimum level, the comparator turns off at a level of 2.2 V to guarantee safe no-load operation.

2.2.5 Multiplier

The multiplier has three inputs M1, M2 and M3. The input M1 provides the information of the waveform of the input voltage. Its range is from 0 V to 4 V being referenced to ground. In order to reach a high THD value it is necessary that the transfer function M_{out} / M1 is highly linear like it is shown in diagram 9 of the datasheet **[1]**. The best performance is available, when the tap potential of the AC voltage divider is close to 4.0 V at highest peak input voltage.

The signal M2 is the output of the voltage amplifier with a range of 2.5 V to 4 V which is referenced to 2.5 V. It is the compensated feedback signal of the output voltage. Principally, the control loop gain will increase with increasing input voltages at given output power which possibly results in control loop instability. But it also causes a high amplification of the 100 Hz-ripple of the DC-bus voltage or other disturbances and is therefore responsible for poor THD values. Unlike input M1, it needs not necessarily to be highly linear. As it is already shown with other PFC control IC better results in terms of THD are possible with a non linear transfer function like square or exponential functions ([2], [3]). A piecewise linear transfer function is implemented in the TDA 4863 according diagram 10 of the datasheet in order to decrease the loop gain in such critical states of operation.

The two corresponding constant factors K_{low} and K_{high} are 0.3 V^{-1} and 0.7 V^{-1}, respectively, which are internal factors of the multiplier. Their dimension is V^{-1} in order to comply with the following equations. In this way the current comparator level can be calculated as

$V_{QM} = K_{low} (V_{pin2} - V_{REF}) V_{pin3}$ for $V_{VVAOUT} < 3.0$ V

$V_{QM} = K_{high} (V_{pin2} - V_{REF}) V_{pin3}$ for $V_{VVAOUT} > 3.5$ V

The output voltage of the multiplier is limited to 1.0 V. This measure causes a defined turn-off threshold for current limitation and also leads to a higher gate voltage u_{GS} of the power MOSFET at worst case conditions.

2.2.6 Current Comparator

The current comparator detects the momentary shunt resistor voltage via its inverting input. The shunt resistor is in the source path of the MOSFET and should have an intrinsic inductance as low as possible. As soon as the shunt voltage reaches the turn-off threshold defined by the multiplier, the turn-off flip-flop is reset and the driver switches off. The turn-off flip-flop prevents multiple pulses during the switching procedure of the power MOSFET.

Voltage spikes occur at the shunt resistor during the turn-on of the MOSFET as a result of the intrinsic inductance of the shunt and the influence of the driver currents. They may lead to an irregular turn-off of the MOSFET. An integrated leading edge blanking suppresses such effects by making the current comparator signal ineffective for 200 ns (typ.).

2.2.7 Detector

A second winding (detector winding) on the choke provides an image of the drain voltage in the ratio N_{det}/N_{boost} according to **Figure 6**. During interval T_1 the MOSFET is on resulting in a negative voltage at the detector winding. When the MOSFET turns off, the flip-flop is reset by the current comparator. Simultaneously the polarity of the detector winding will change to positive corresponding to the drain voltage. When the detector

voltage exceeds 1.5 V with positive edge the flip-flop is locked. After the diode took the current its voltage is positive (interval T_2) as long as current is flowing through the boost diode. When the current reaches zero, the detector voltage falls below 1 V being the level of enabling the driver stage for the MOSFET.

The calculation of its number of turns is done in section **"IC Supply" on Page 12**. The winding is applied to pin 5 via a high-ohmic resistance (10 kΩ to 47 kΩ). Clamping structures are available in the IC which limit the voltage at the input to +5 V and +0.5 V, respectively, at ±5 mA.

There are cases in which there is no significant detector signal to set the turn-off flip-flop. This may occur when the supply voltage is switched on, in case of line overvoltage exceeding the output voltage and in no-load and low-load operation, when the voltage controller specifies intermittant operation. In that case a startup generator is activated which supplies a set of pulses to the turn off flip-flop if the driver output stays on LOW-level longer than 160 µs typically.

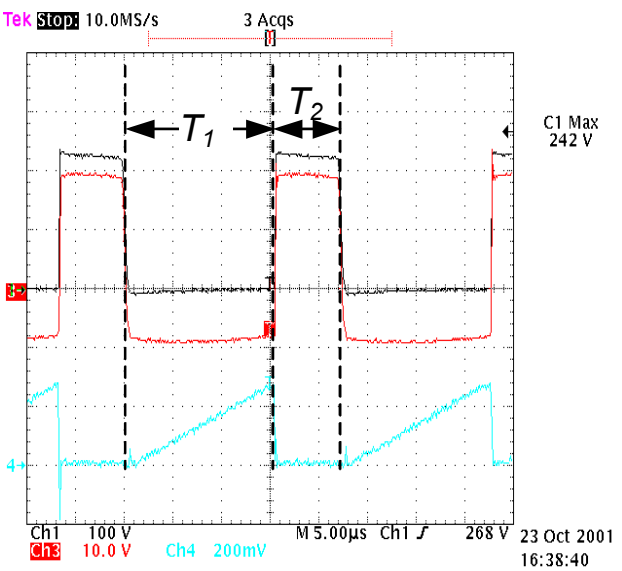

Figure 5 Drain voltage (black, 100 V/div), detector voltage (red, 10 V/div) and shunt voltage (200 mV/div) using a supply circuit similar to Figure 10

3 Applications of the TDA 4863

3.1 IC Supply

An obvious way to supply the IC is to use the detector winding. We have to care, that the supply circuit doesn't influence the detector signal. First, in a simple voltage mode supply, we use a diode, a storage capacitor C_{10} and a current limiting resistor R_{12} as it is given in a) of **Figure 6**. We achieve good results in ballast applications with the following design of the transformation ratio:

$$\frac{N_{ZCD}}{N_P} = \frac{V_{ZCD}}{V_{out} - V_{innom}} \qquad V_{ZCD} = 22\ V...24\ V; \qquad R_{12} = 220\ \Omega...270\ \Omega \qquad [6]$$

Second, in a charge pump supply we use two diodes, two capacitors C_{10}, C_{13} and one decoupling resistor R_{12} or a decoupling inductor L_5 (lower losses) and a current limiting resistor R_{12A} as it is shown in b) and c) of **Figure 6**, to avoid burn down at resonance frequency. This method of supply is to prefer in SMPS applications with wide input voltage range. All the following applications use circuitry b) of **Figure 6**.

The supply current increases with the operating frequency at low load and is not dependent on the input voltage. We achieve good results with the following design of the transformation ratio:

$$\frac{N_{ZCD}}{N_P} = \frac{V_{ZCD}}{V_{out}} \qquad V_{ZCD} \approx 80\ V, \quad C_{13} = 3\ nF...4\ nF; \quad R_{12} = 390\ \Omega...270\ \Omega \qquad [7]$$

Or C_{13} = 1 nF...1.5 nF, L_5 = 50 µH...100 µH, R_{12A} designed with C_{13} and L_5 as a low-pass filter of Bessel characteristic.

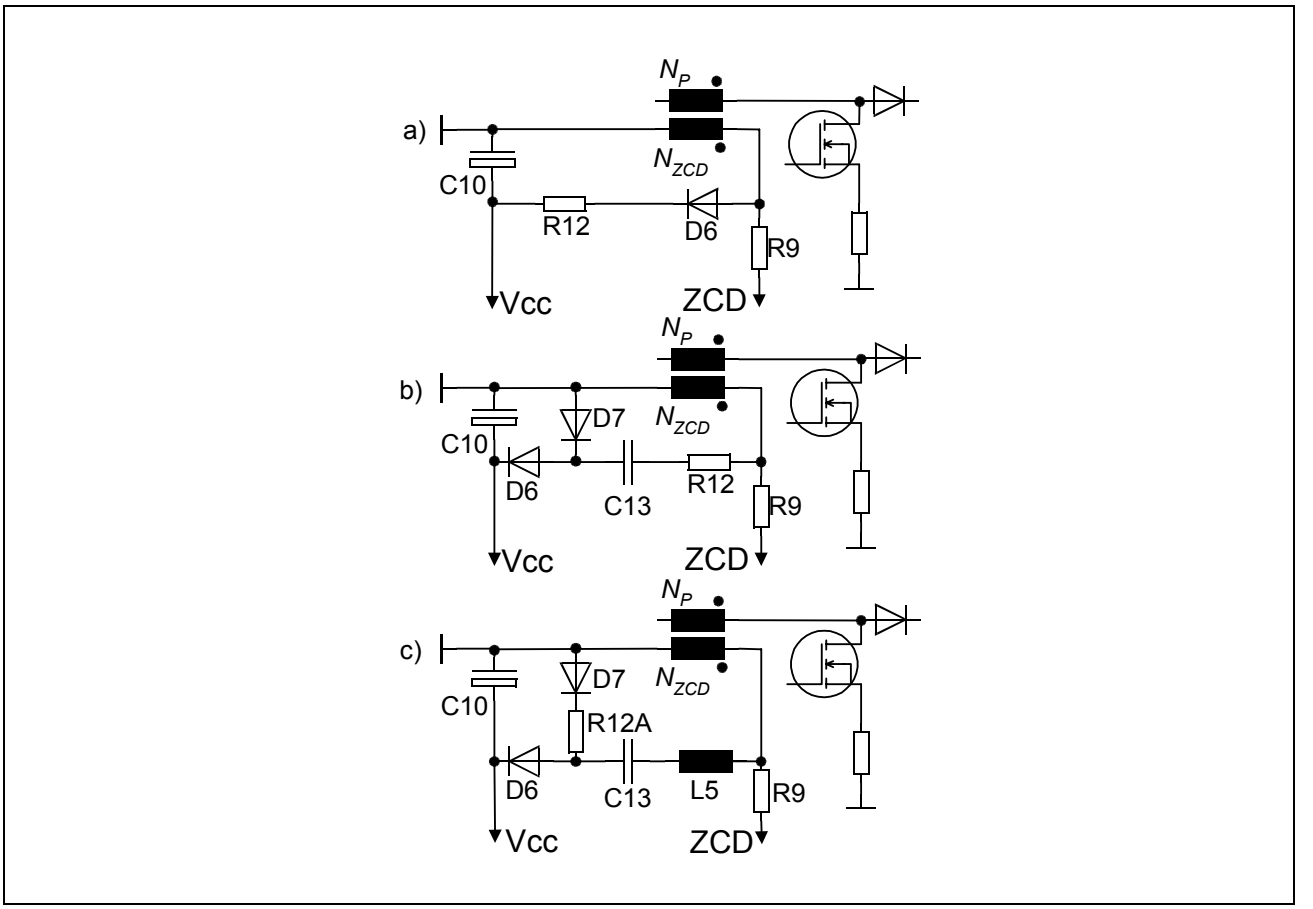

Figure 6 IC Supply Circuit Realized with Rectifier (a) and Charge Pump (b and c)

3.2 Opamp Compensation Design

The design of the compensation network of PFC controller is a very sensitive topic, because it highly influences the performance of the circuit in terms of the total harmonic distorsion (THD) of the input current. It is particularly responsible for the control loop behavior in case of changes of operational parameters, such as load or input voltage, as well as for the AC-ripple rejection of the output voltage. Especially the demand for a good suppression of the superimposed AC-share of the output voltage is contrary to the demand of a good behavior at load changes or changes of the input voltage, because they take effect in different areas of frequencies. For example, load steps will always affect higher frequencies than the 100 Hz (or 120 Hz in North America) output voltage ripple does.

3.2.1 PI-Controller

In case that a constant output power is taken from the boost converter, the boost converter can be modelled as an integrator according to [2]

$$F_S(s) = \frac{V_{out}}{I_{PkmaxHF}} = \frac{K_I}{sC_{out}}; \quad K_I = \frac{\sqrt{2}V_{in}}{4V_{out}} \qquad [8]$$

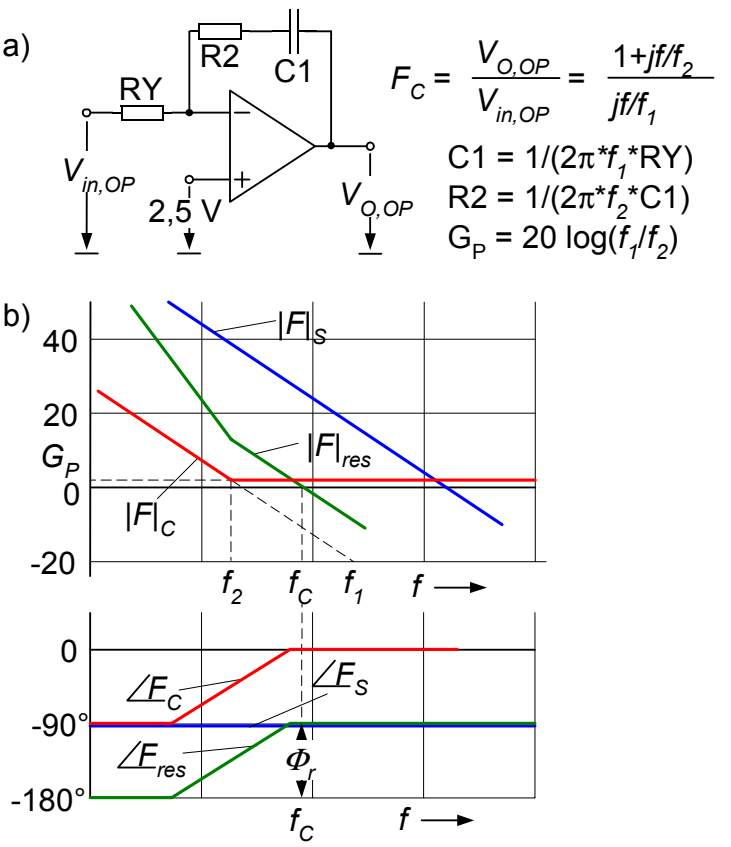

Figure 7 a) PI-Controller Topology
b) Frequency Response of PI-Controller and Load

It has therefore a phase of constantly 90°. If the compensation would now be integrating as well, the resulting phase response of the control-loop will have 180°, which will lead to a phase margin $\Phi_r = 0$ and to a highly instable system. Hence, a PI-controller topology is recommended at least. Such a controller is shown in a) of **Figure 8**

The correspondence between the components R_Y, C_1 and R_2 is given by the equations in **Figure 7**.

Part b) of **Figure 7** shows the resulting frequency response of the transfer function of the controller of a) and a load with constant power. In the area of the crossover frequency f_C

there is a decrease of 20 dB/decade which indicates a good dynamic behavior of the system [4]. There is also a zero in the Nominator of the controller transfer function giving a phase shift of +90°. In Figure 7 this leads to a phase margin of Φ_r = 90° and therefore a good stability of the system.

A good set of the frequencies f_1 and f_2 will be f_1 = 0.1 Hz and f_2 = 5 Hz which will result in a capacitor C_1 = 2.2 µF and a resistor R_2 = 16 kΩ.

It is usually recommended, that the bandwidth of the compensation is about 20 Hz. This will lead to a relatively constant output of the compensator over a mains period. A better performance can be achieved by introducing a pole at 100 Hz (or 120 Hz, respectively).

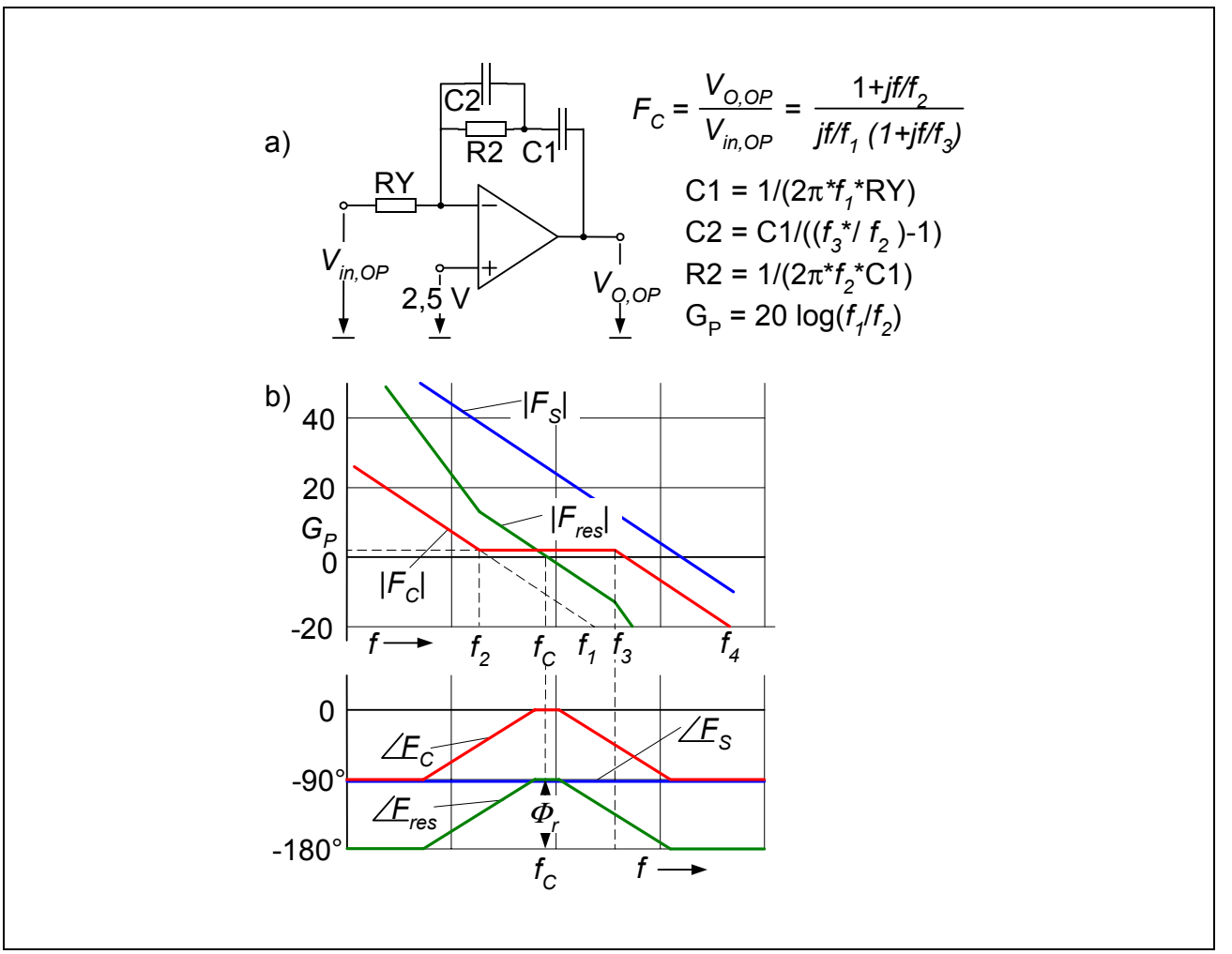

Figure 8 **a) PI-Controller topology**
b) Frequency Response of PIT1-Controller and Constant Load

3.2.2 PIT1 Controller

In some applications a higher immunity against higher frequency disturbances is required. This can be achieved using an additional delay share in the controller transfer function as it is shown in **Figure 8** causing a pole in the controller transfer function. The only difference is the additional capacitor C_2 in parallel to the resistor R_2 as it is shown in a) of **Figure 8**.

The resulting gain response $|F_{res}|$ now decreases with 40 dB/decade after frequency f_3, so that higher frequencies will be damped stronglier. Simultaneously the trace rises with 40 dB/decade on direction of lower frequencies which will amplify low frequency shares of the opamp input voltage. Both will lead to a better steady state operation and the influence of disturbances will be reduced. It must be noted here, that the phase margin must not necessarily be 90° as it is shown in b) of **Figure 8**. With another selection of f_3 there might also be smaller phase margins.

A recommended rating for a 110 W PFC preconverter for wide range applications is C_1 = 2.2 µF, C_2 = 1 µF and R_2 = 33 kΩ.

3.3 Universal Preconverter and 2-lamp Dimming Ballast Design

These applications demonstrate the excellent performance of the TDA 4863 controlling a power factor preconverter. The design steps indicate the method of the calculation of the components values. A design for lamp ballast (nominal input voltage V_{innom} = 277 V, output power P_{out} = 70 W) as well as a design for switched mode power supplies (input voltage V_{in} = 90 V ... 265 V, output power P_{out} = 120 W) are give here as examples. Circuit diagrams and measurements results at different operating conditions establish a good basis for evaluation.

Usually a single stage RFI-filter does not accomplish the RFI-standards. Therefore multiple stage RFI-filters are designed into these applications as an example how to suppress resonant oscillations of these filters.

Discontinuous conduction mode always results in high efficiency, because it avoids reverse recovery losses of the boost converter diode. A high power factor, low harmonics, a wide input voltage range and a feedback controlled output voltage are the most important features of a power factor preconverter. The TDA 4863 contains all control and monitoring functions to meet these demands.

3.4 Design Steps

3.4.1 Input and Output Section

Application			2-Lamp-Ballast	SMPS-Preconverter
Nominal input voltage	V_{innom}		277 V AC	110 V - 230 V
Minimum input voltage	V_{inmin}	= V_{innom} - 20%	250 V AC	90 V AC
Maximum input voltage	V_{inmax}	= V_{innom} + 20%	305 V AC	265 V AC
Minimum peak input voltage	$V_{inPkmin}$	= $\sqrt{2}\ V_{innin}$	353 V	127 V
Maximum peak input voltage	$V_{inPkmax}$	= $\sqrt{2}\ V_{innax}$	431 V	375 V
Estimated minimum efficiency	η		0.9	0.9
Output power	P_{out}	= $\eta\ P_{in}$	70 W	120 W
Maximum peak input current	$I_{inPkmax}$	= $2P_{out}/(V_{inpmin}\ \eta)$	0.44 A	2.1 A
Maximum high frequency peak current	$I_{PkmaxHF}$	= $2I_{inPkmax}$	0.88 A	4.2 A
Maximum current sense threshold	$V_{ISensemax}$	= 1.0 V		
Shunt resistor	R_{11}	= $V_{ISensemax}/I_{PkmaxHF}$	1.14 Ω	0.24 Ω
Nominal output voltage	V_{out}	Recommended minimum: V_{out}+30 V	450 V DC	400 V DC
Reference voltage	V_{ref}	= 2.5 V		
Controller current at pin V_{AOUT}	I_{VAOUT}	= 40 µA		
Overvoltage threshold	V_{OV}	≈ 1.1 V_{out}	480 V DC	440 V DC
Output voltage divider	R_4	= $R_5 = \frac{V_{ref}}{\Delta I} \cdot (\frac{V_{OVP} - V_{out}}{V_{out} + V_{ref}})$	748 kΩ	998 kΩ
	R_5	= $R_4 = (\frac{V_{OVP} - V_{ref}}{\Delta I + V_{ref} / R_5})$	4.12 kΩ	6.34 kΩ

3.4.2 Multiplier Section

Application			1-Lamp-Ballast	SMPS-Preconverter
Multiplier inputs M1 and M2 dynamic voltage range		V_{m1R} = 4.0 V; V_{m2R} = 1.5 V		
Multiplier output limitation	V_{Qmmax}	= $V_{ISensemax}$ = 1.0 V		
Multiplier gain V_{m1}(V_{Qm} = 1.3 V; V_{m2R} = 2 V) Select V_{m1} = V_{m1lim} = 1.2 V	K	= 0.65 @ V_{inpmin} =	 127 V	
Select upper resistor of input voltage divider	R_6		1.0 MΩ	940 kΩ
Lower resistor of input voltage divider	R_7	= R_6 . V_{m1lim}/(V_{inpmin}-V_{m1lim})	9.1 kΩ	9.1 kΩ
Low pass filter capacitor	C_4	= 1/(2π.R_7.f), 1 kHz < f < 3 kHz	10 nF	10 nF
Test: Input range V_{m1}(V_{in}=V_{inpmax}) < V_{m1R} = 3.8 V? otherwise select V_{m1}(V_{in}=V_{inpmin}) < V_{m1lim} = 1.2 V	$V_{m1inmax}$	= V_{inpmax} *R_7/(R_6 + R_7)	3.9 V	3.59 V
	$V_{m1inmin}$	= V_{inpmin} *R_7/(R_6 + R_7)	3.2 V	1.22 V

3.4.3 Boost Inductor Section

In this section two different approaches for the calculation of the transformer primary inductance L_P are presented. The first one is recommended for a small input voltage range application or for applications with nearly constant output power, e.g. lamp ballasts. The other one is suitable for the demands of wide range applications like they occur in SMPS. All the values of the sections before are still valid.

2-Lamp-Ballast	SMPS-Preconverter
On-time of power switch: $T_{on} = L_P \cdot I_{pmaxHF}/V_{in,\ lpmaxHF} = 2\ I_{in}$ Off-time of power switch: $T_{off} = L_P \cdot I_{pmaxHF}/(V_{out} - V_{in})$ Pulse frequency: $f = \frac{1}{T_{on}+T_{off}} = \frac{V_{in}\cdot(V_{out}-V_{in})}{V_{out}\cdot L_P \cdot I_{p\max HF}}$	
Design Criterion:	
Calculate L_P according to desired range of pulse frequency (e.g. 80 kHz < f_p < 110 kHz) at nominal input voltage V_{innom} and rated output power P_{out} $L_P = \frac{V_{innom}\cdot(V_{out}-V_{innom})}{V_{out}\cdot f_p \cdot I_{p\max HF}} = \frac{V_{innom}\cdot(V_{out}-V_{innom})\cdot\eta\cdot V_{innom}}{V_{out}\cdot f_p \cdot 2P_{out}} =$ $= \frac{277\,V\cdot(480\,V-277\,V)\cdot 0{,}9\cdot 277\,V}{450\,V\cdot 90\,kHz\cdot 2\cdot 70\,W} = 1077\ \mu H$ **Also possible** Calculate L_P by selecting the on-time T_{on} in the range of 3 µs < T_{on} < 6 µs $L_P = \frac{T_{on}\cdot V_{innom}}{I_{p\max HF}} = \frac{T_{on}\cdot V_{innom}^2\cdot\eta}{2\cdot P_{out}} = \frac{3\,\mu s\cdot(277V^2)\cdot 0{,}9}{2\cdot 70\,W} = 1480\ \mu H$ Both inductances are appropriate, but the calculation is done with 1077 µH. Core selection: EF20	Calculate L_P in order to obtain pulse frequencies higher than 25 kHz at maximum peak input voltage and twice of nominal output power and at minimum peak input voltage and twice of nominal output power $L_P < \frac{V_{inp\max}^2\cdot(V_{out}-V_{inp\max})\cdot\eta}{V_{out}\cdot f_p\cdot 2\cdot 2P_{out}} = \frac{(375V)^2\cdot(410\,V-375\,V)\cdot 0{,}9}{410\,V\cdot 25\,kHz\cdot 2\cdot 2\cdot 120\,W} = 665\ \mu H$ and $L_P < \frac{V_{inp\min}^2\cdot(V_{out}-V_{inp\min})\cdot\eta}{V_{out}\cdot f_p\cdot 2\cdot 2P_{out}} = \frac{(127V)^2\cdot(410\,V-127\,V)\cdot 0{,}9}{410\,V\cdot 25\,kHz\cdot 2\cdot 2\cdot 120\,W} = 828\ \mu H$ We therefore select L_P < 665 µH Core selection: E36

Number of turns:

A_L-value for EF20-core:

$$A_L = \frac{B_{max}^2 \cdot A_e^2}{i_{p\,max\,HF}^2 \cdot L_P} = \frac{(250mT)^2 \cdot (32mm^2)^2}{(0{,}88A)^2 \cdot 1077\mu H} = 77nH$$

Air gap:

$$s = \left(\frac{A_L}{K_1 nH}\right)^{\frac{1}{K_2}} = \left(\frac{77nH}{60{,}6nH}\right)^{\frac{1}{-0{,}737}} = 0{,}74mm$$

Select air gap according [1]: s = 0.75 mm => resulting A_L-value:

$$A_L = K_1 \cdot s^{K_2} = 76nH$$

=>

$$N_{PFC} = \sqrt{\frac{L_P}{A_L}} = \sqrt{\frac{1077\mu H}{76nH}} = 118.$$

A_L-value for E36-core:

$$A_L = \frac{B_{max}^2 \cdot A_e^2}{i_{p\,max\,HF}^2 \cdot L_P} = \frac{(250mT)^2 \cdot (120mm^2)^2}{(4{,}2A)^2 \cdot 665\mu H} = 77nH$$

Air gap:

$$s = \left(\frac{A_L}{K_1 nH}\right)^{\frac{1}{K_2}} = \left(\frac{77nH}{182nH}\right)^{\frac{1}{-0{,}749}} = 3{,}15mm$$

Select air gap according [1]: s = 2 mm =>

$$A_L = K_1 \cdot s^{K_2} = 108nH$$

=>

$$N_{PFC} = \sqrt{\frac{L_P}{A_L}} = \sqrt{\frac{665\mu H}{108nH}} = 78.$$

Zero current detector and auxiliary power supply

A winding ratio $N_{PFC} : N_{aux}$ of about 5:1 is recommended for proper operation. Therfore: N_{aux} = 118/5 = 23

Dito
N_{aux} = 78/5 = 16

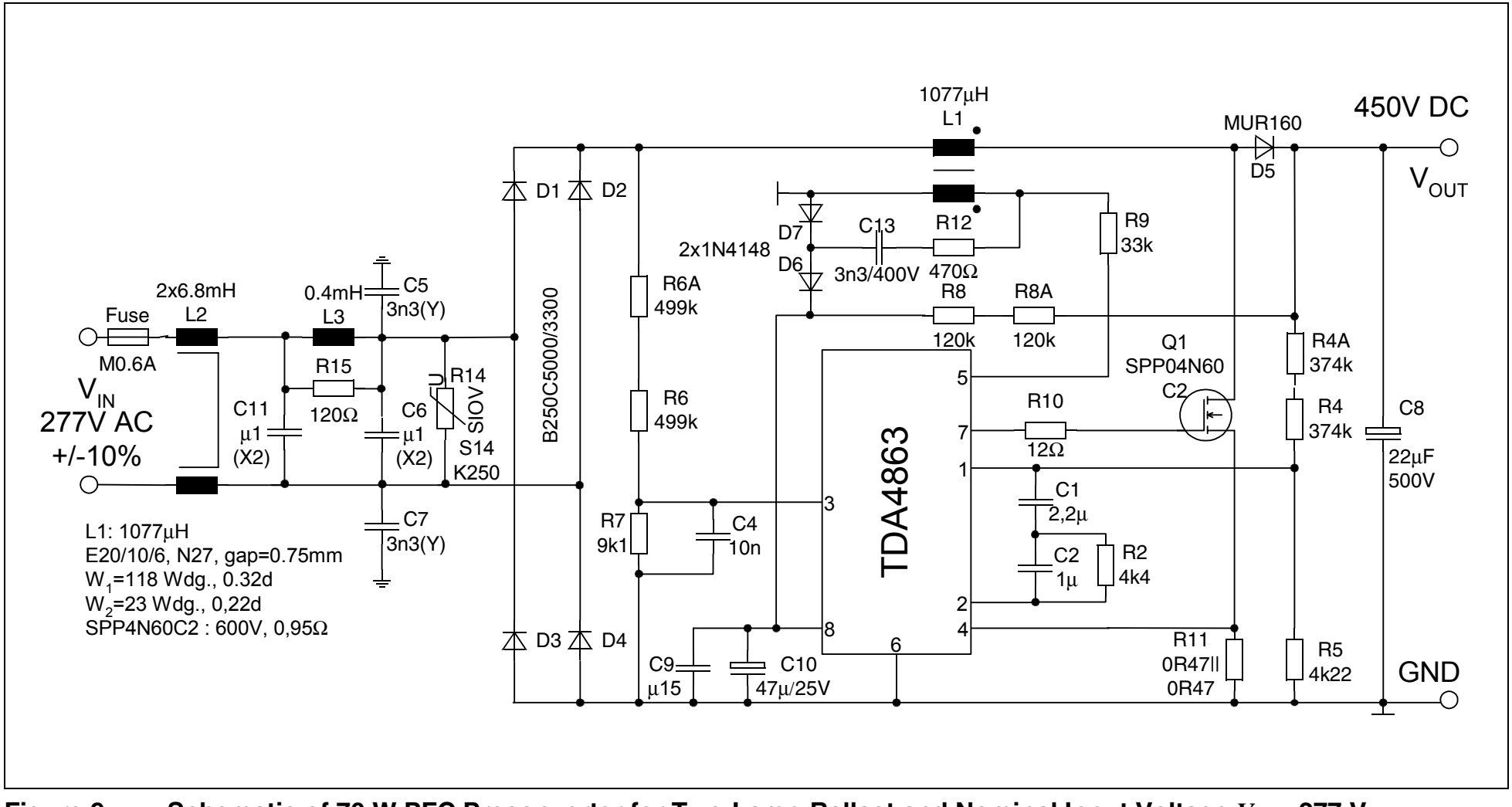

Figure 9 Schematic of 70 W PFC Preconverter for Two-Lamp-Ballast and Nominal Input Voltage V_{in} = 277 V

Measurement Results of TDA 4863 for 2-lamp-ballast (70 W) at 10%, 25%, 50% and 100% of Rated Load

TDA 4863 Operation 70 W (V_{innom} = 277; C_{out} = 22 µF)

V_{in} [V AC]	I_{in} [mA rms]	P_{in} [W]	PF	THD [%]	V_{BUS} [V DC]	I_{out1} [mA]	P_{out} [W]	Effi`cy [%]
250.4	42.65	9.74	0.913	11.1	453.0	15.4	6.98	0.72
250.4	83.70	20.40	0.974	11.7	453.0	38.5	17.44	0.85
250.6	123.70	38.15	0.990	9.4	453.0	77.0	34.88	0.91
249.8	296.20	73.70	0.996	6.3	453.0	154.1	69.81	0.95
276.2	40.20	9.61	0.866	20.8	453.0	15.4	6.98	0.73
277.5	75.90	20.30	0.963	12.5	453.0	38.5	17.44	0.86
277.7	138.60	38.00	0.987	9.9	453.0	77.0	34.88	0.92
276.9	267.00	73.50	0.994	8.0	453.0	154.0	69.76	0.95
305.3	41.00	9.20	0.726	48.0	453.0	15.4	6.98	0.76
305.2	69.50	20.16	0.949	12.0	453.0	38.5	17.44	0.87
304.8	126.60	37.90	0.981	11.0	453.0	77.1	34.93	0.92
304	263.30	73.40	0.993	8.1	453.0	154.1	69.81	0.95

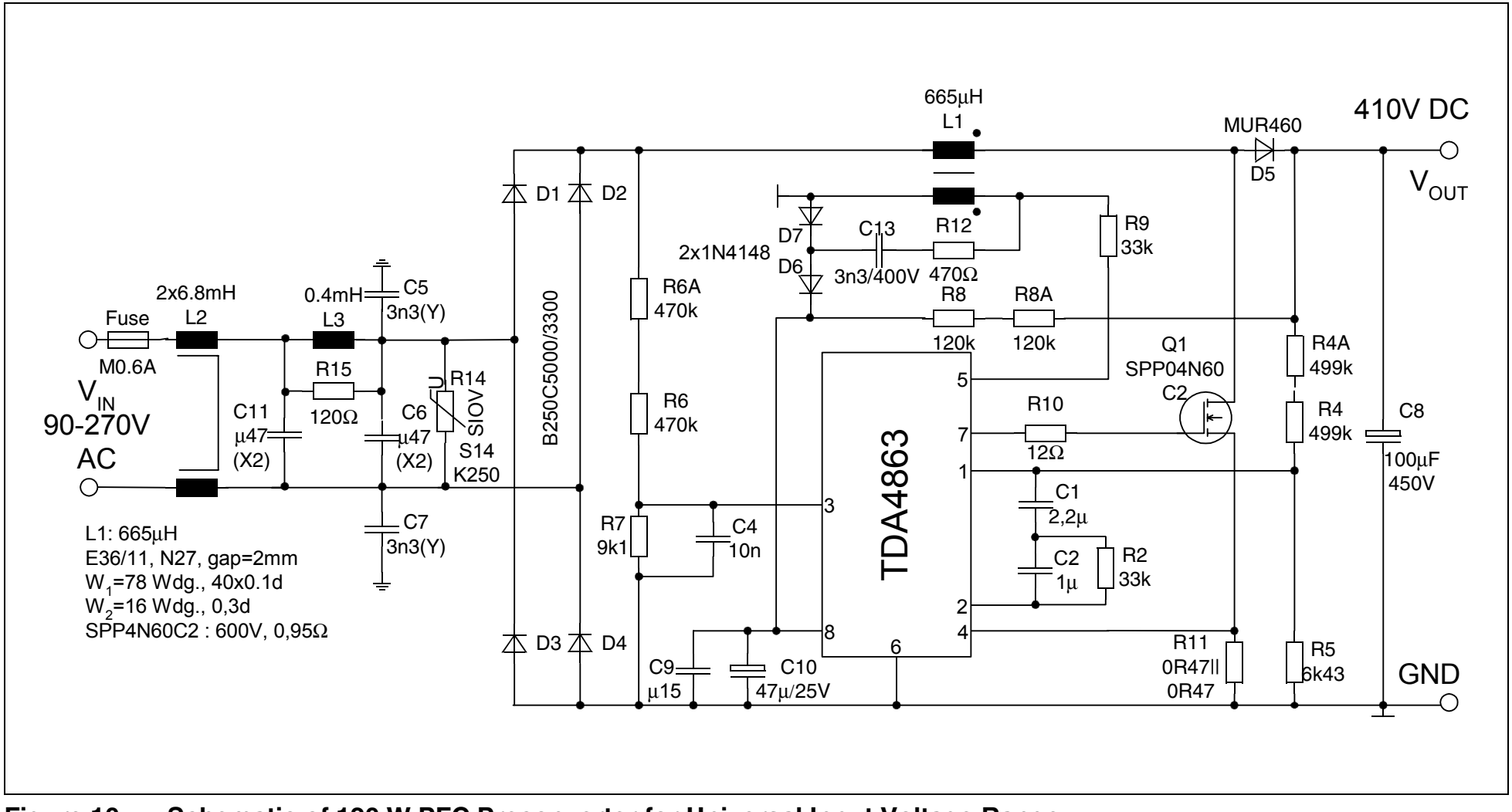

Figure 10 Schematic of 120 W PFC Preconverter for Universal Input Voltage Range

Measurement results of TDA 4863 with Universal Input Voltage Range at 10%, 25%, 50% and 100% of Rated Load

TDA 4863 Operation 120 W Universal Input Voltage Range (C_{out} = 100 µF)

V_{in} [V AC]	I_{in} [mA rms]	P_{in} [W]	PF	THD [%]	V_{BUS} [V DC]	I_{out1} [mA]	P_{out} [W]	Effi`cy [%]
90	166.10	14.80	0.987	5.9	401.0	30.0	12.03	0.81
90.2	380.10	33.30	0.997	4.2	401.0	75.0	30.08	0.90
91.5	711.00	65.00	0.998	6.0	401.0	150.0	60.15	0.93
90.6	1482.00	132.80	0.995	8.2	401.0	299.0	119.90	0.90
119.3	130.70	15.00	0.962	8.5	401.0	30.0	12.03	0.80
120.5	278.80	33.30	0.993	4.4	401.0	75.0	30.08	0.90
121	532.70	64.38	0.998	2.2	401.0	150.0	60.15	0.93
120	1069.00	128.20	0.999	4.0	401.0	299.0	119.90	0.94
180.4	100.10	15.10	0.836	12.8	401.0	30.0	12.03	0.80
181.1	191.80	33.40	0.959	7.9	401.0	74.7	29.95	0.90
182.1	355.20	64.00	0.989	4.4	401.0	150.5	60.35	0.94
181.2	693.80	125.40	0.997	3.2	401.0	300.0	120.30	0.96
231.3	102.90	14.80	0.622	37.0	401.0	30.0	12.03	0.81
230.9	156.66	33.10	0.899	9.5	401.0	74.7	29.95	0.90
230.8	284.40	63.73	0.970	6.7	401.0	150.0	60.15	0.94
230	546.00	124.80	0.993	3.4	401.0	300.5	120.50	0.97
265	102.80	14.70	0.54	26.0	401.0	30.0	12.03	0.82
265	151.30	32.80	0.817	23.8	401.0	75.0	30.08	0.92
264.7	252.60	63.40	0.948	8.8	401.0	150.0	60.15	0.95
263.9	475.70	123.90	0.987	4.6	401.0	300.0	120.30	0.97

4 Summary of Used Nomenclature

Physics:

General identifiers:

A.....cross area
b, B.....magnetic inductance
d, D .....duty cycle
f.....frequency
i, I.....current
N .....number of turns
p, P.....power
t, T.....time, time-intervals
v, V.....voltage
W.....energy
η.....efficiency

K_1, K_2 ..ferrite core constants

Special identifiers:

A_L ..... inductance factor
$V_{(BR)CES}$ .. collector-emitter breakdown voltage of IGBT
V_F..... forward voltage of diodes
V_{rrm} ..... maximum reverse voltage of diodes

big letters: constant values and time intervals
small letters: time variant values

Components:

C .....capacitance
D .....diode
IC .....integrated circuit
L.....inductance
R.....resistor
TR .....transformer

Indices:

AC.....alternating current value
DC.....direct current value
BE .....basis-emitter value
CS.....current sense value
OPTO..optocoupler value
P .....primary side value
Pk.....peak value
R..... reflected from secondary to primary side
S .....secondary side value
Sh .....shunt value
UVLO ..undervoltage lockout value
Z.....zener value

fmin..... value at minimum pulse frequency
i .....running variable
in .....input value
max .....maximum value
min .....minimum value
off .....turn-off value
on .....turn-on value
out .....output value
p .....pulsed
rip .....ripple value

1, 2, 3 .....on-going designator

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Dr. Ulrich Schumacher

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