A Novel Control Concept for Highest Precision Accelerator Power Supplies

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Abstract

Accelerator applications need extremely precise power supplies (PS) for their various magnets. For the control an exact modelling of the PS and the load is essential. A sophisticated analog to digital conversion scheme is the key part for the necessary precision. A fully digital controller enabled identical control hard- and software for 580 units, allowing high flexibility of the control structures. Adaptions for different types of PS are made by software parameter adjustments only.

I. Introduction

In the **S**wiss synchrotron **L**ight **S**ource (SLS) electrons are accelerated to very high energy. A large number of **P**ower **S**upplies (PS) is needed to feed the magnets for the beam control. The demands on the magnetic field, and consequently on the currents, are extremely high: a short term stability down to 10 ppm (parts per million) is necessary for a selection of them: [2], [3], [4]. In addition, some of them require a control bandwidth exceeding 1kHz.

The reference values for all the PS are generated by a digital control system. In today's accelerator these values are fed to the analog control circuit of the power supplies via a precise DAC. For supervisory purposes the measured current is also fed back to the control system via a precise ADC. In most cases the control bandwidth is low.
With a digital controller for the PS the twofold very precise conversion can be reduced to a single AD-conversion. Drift problems are reduced to the drift of the voltage reference for the ADCs. Additionally, a significantly expanded functionality and flexibility of the control results. A powerful intelligent DSP-controller and a fast high-precision, high stability ADC card were developed in close cooperation with two industrial companies. All the PS of the new synchrotron light source are equipped with this card set. (Two special PS with higher power ratings use even sets of multiple controllers.)

This paper will first describe the structure and the model of the implemented PS. The model and the method for the parameter estimation of the load (magnets) will be explained. This is followed by the basic structure of the developed DSP-controller and the ADC card. Further, the chosen control concept will be presented. Key parts and solutions for critical tasks are outlined.
The presented system is the first fully digital control of all the PS of an entire accelerator [2]. The very positive experience with these power supplies since 1999 has proven the chosen concept.

II. Hardware structure and modelling of the PS

The demands on the PS are very high. For a fast and precise control of these units exact models of the entire PS with load, i.e, the magnets, are needed.

The accelerator needs over 200 PS with one voltage and one current direction. They are built as straight forward buck converters. These are one quadrant PS as shown in Fig. 1. left. 300-plus PS need positive and negative load voltage as well as positive and negative currents, they are operated in four quadrants. The basic structure is shown in Fig. 1. right. For some magnets positive and negative voltage but only one current direction is needed. This functionality can be provided with a two quadrant PS. Its structure is identical to the four quadrant set up, but two switching elements are replaced by diodes only (D_2 and D_3 instead of T_2 and T_3). The used power semiconductors are MOS-FETs with switching frequencies of 50kHz or 100kHz, as well as IGBTs, switched with 25kHz, depending on the ratings of the PS. All controllable semiconductors are driven via optical links and high quality gate driver.

The dc-voltage source U_{d0} in Fig. 1. represents a unregulated or poorly regulated source as it is for example a mains transformer with a 6 pulse rectifier. This standard block needs no further discussion.

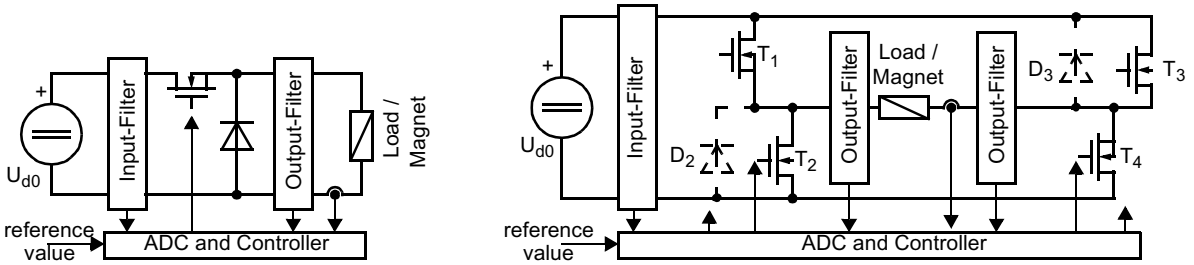

Fig. 1. Left: single quadrant buck structure; right: H-Bridge with T1..T4 operating as full bridge for 4 quadrants; with diodes D2 and D3 as two quadrant converter (‚reduced H-bridge')

II.1 Input and output filter

In order to limit EMI (electromagnetic interferences) all PS need filtering of the input (mains side) and output (load side) properties. Since the instruments around the accelerator are extremely sensitive, the suppression has to cover a wide frequency range. The frequencies that have to be suppressed can be grouped into the low frequent harmonics of the PWM-frequency and high frequent EMIs, caused by switching transients. Only the filter for the ‚low'-frequent PWM-harmonics influences the controller design. Therefore, only those will be considered in the following. Input and output filters consist of higher order LC-Filter as shown in Fig. 2. The fundamental structure for all PS is identical.

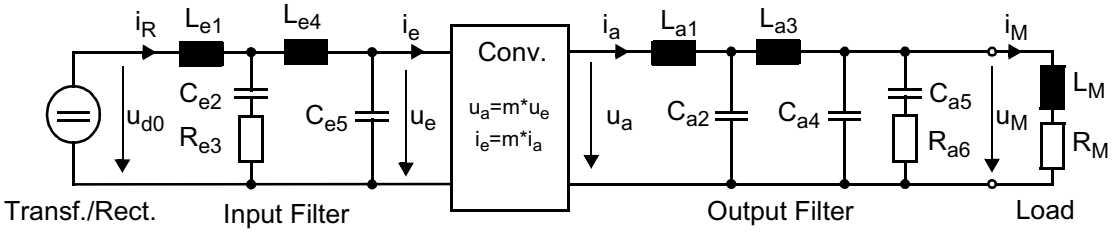

Fig. 2. PS-structure with input filter, time continuous converter model and output filter

The input filter fulfils two tasks: The first being the reduction of the 300Hz ripple (6 times 50Hz) caused by the 6 pulse rectifier. The second to keep the PMW harmonics from the mains. The 4. order filter is damped with the resistor R_{e3}. As the resulting capacity of C_{e2} plus C_{e5} has to be designed to filter 300Hz, the filtering of a PWM frequency of some 10kHz is very good.

A converter, that is controlled for a constant output current, represents a negative impedance for the dc-link. In high current low voltage PS this can lead to instabilities for certain combinations of the filter inductors and capacitors, as described for example in [1]. The problem can be overridden by reducing the filter output impedance, i.e. increasing the capacitance.

All output filters are of the 5. order. The damping is made in the last stage, in order to minimize the losses in the resistor R_{a6} caused by the PWM. The corner frequencies of the filters are chosen to guarantee the PWM fundamental to be less than 100mV over the magnets. Typically these frequencies are by a factor of ten below the switching frequency of the semiconductors.
For the controller design the two identical output filters of the four quadrant converter in Fig. 1. can be summarised into the form of Fig. 2.

II.2 Converter model

For control considerations and simulations it is preferable to have a time continuous model of the converters. As the input voltage depends on the load current, the entire system becomes nonlinear. With the *modulation function m(t)* a simple set of equations results (1), as it is described in [7].

$$u_a = m u_e; \quad i_e = m i_a \quad (-1 \le m \le 1) \tag{1}$$

These equations describe the behaviour of the converter correct. For a linear controller design they have to be linearised according to (2). The index $_0$ indicates the operating point.

$$\Delta u_a = m_0 \Delta u_e + \Delta m u_{e,0}; \quad \Delta i_e = m_0 \Delta i_a + \Delta m i_{a,0}; \quad (-1 \le m \le 1)) \tag{2}$$

II.3 Modelling of the load

For an optimal control, good models of the electrical behaviour of the magnets are needed. The resistive and inductive part of their impedance show a strong frequency dependence. In addition, cabling capacitance can cause resonances.

The design of the magnets varies, depending on their application. The iron cores of magnets for constant field are built of thick sheet metal. Some of them even have solid iron cores. Magnets for dynamic tasks are built with thin sheets. Hysteresis losses and eddy currents in the iron core increase with rising frequency and with the thickness of the sheet metal. Both effects can be modelled with a frequency dependant ohmic part of the coil. Furthermore, skin- and proximity-effects in the copper windings occur. While this also leads to increasing losses with rising frequency, the inductance falls. Altogether, the resistance of the magnet impedance rises while the inductance falls.

II.3.1 Cabling impedance and grouping of the magnets

The cabling inductance is added to the inductance of the magnets and does not cause any problems as it is comparatively small. However, the capacitance leads to a parallel RLC-resonance in a frequency range of less than 10kHz.

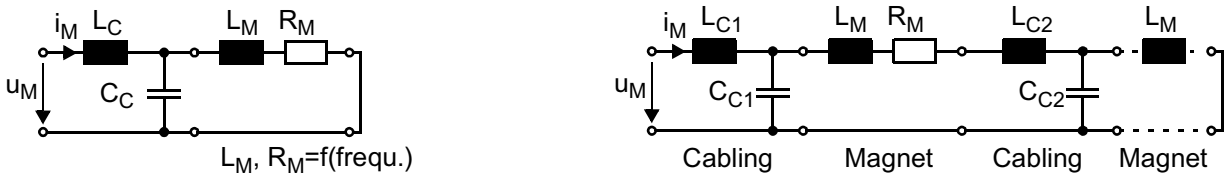

Fig. 3. Magnets with cabling; left: single magnet; right: magnet family

Some magnets are grouped into families, serially connected with cabling between every magnet. Such a set up shows a number of parallel and series resonances. The electrical representation of a single magnet and a magnet family, both with cabling, are shown in Fig. 3.

II.3.2 Measured impedances

Measurements were performed with a vector signal analyser in the range from dc to 20kHz. A family of 12 sextupole magnets is depicted as an example in Fig. 5. left. This group shows the lowest resonance frequencies. For all the measured magnets the sequence of parallel and series resonances is the same: they all start with a parallel resonance followed by a series resonance and so forth.

II.3.3 Equivalent circuit for the magnets

A simple representation of the load is highly desirable for the controller design. The model has to be included into the PS output filter. The correctness of the representation has to be guaranteed for a limited frequency range only, i.e. up to approximately 10kHz. This allows a limited order of the magnet-model. With the goal of an identical structure for all magnets, i.e. single magnets and families, the electrical circuit of the fourth order in Fig. 4. proved to be a good solution. It allows the modelling of the frequency dependent ohmic and reactive parts, as well as one parallel and one series resonance. All the elements of the model are frequency-independent.

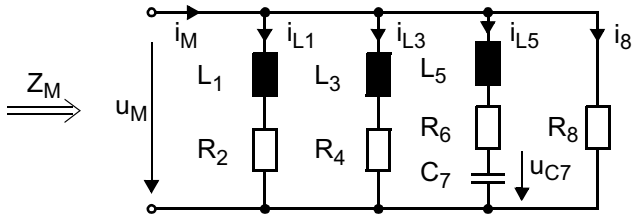

Fig. 4. Electrical circuit for the modelling of the magnet behaviour

II.3.4 Fitting of the elements

The numerical fitting of the elements is done with help of a least square algorithm in the frequency range from ω_{min} to ω_{max}. The optimisation tries to minimise the squared error. Negative elements as a result of a fit have to be avoided, as they lead to unstable networks. The fitting is done for the real and the imaginary part of the impedance. The squared error between the components of the measured impedance $\underline{Z}_m$ and the impedance of the model $\underline{Z}_M$ is defined with (3) and (4).

$$err_{Re} = g_{Re} \sum_{\omega_{min}}^{\omega_{max}} \left(Re(\underline{Z}_m) - Re(\underline{Z}_M)\right)^2 \tag{3}$$

$$err_{Im} = g_{Im} \sum_{\omega_{min}}^{\omega_{max}} \left(Im(\underline{Z}_m) - Im(\underline{Z}_M)\right)^2 \tag{4}$$

The best fit for the impedance of the magnets is yielded with the weighting functions in (5). These functions give a good balance between the absolute value of the impedance as well as the ratio between real and complex part. If a stronger emphasis for low frequencies is needed, an additional weight with $1/\omega$ can be added.

$$g_{Re} = 1/(\left|\underline{Z}_m\right| Re(\underline{Z}_m)); \qquad g_{Im} = 1/(\left|\underline{Z}_m\right| Im(\underline{Z}_m)) \tag{5}$$

The quality of a fit for the chain of sextupole magnets with its multiple resonances is shown in Fig. 5. right. The fit is optimized as to model the first and second resonance correct, i.e. in the angular frequency range from 10 to 20ks^{-1}.

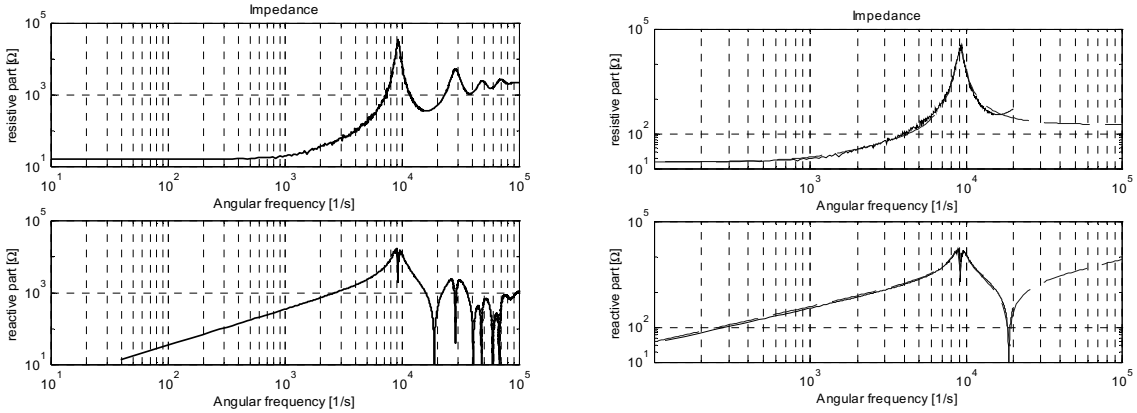

Fig. 5. Family of 12 magnets; top: resistive part, bottom absolute value of the reactive part, left: measured impedance; right: solid: measurements; dashed: model results

II.3.5 Start values for the optimization

The given optimization problem has not only one but a number of local optima. Therefore, the start values for an optimization run are important for the result. No overall rule for all the initial values of the elements could be derived. But, for a selection the following values, derived from the measurements, where usually successful:

a) L_1, R_2 represent the impedance at low frequency
b) R_8 models the high frequency resistive part
c) C_7 corresponds to the approximate cabling capacitance

The other elements are chosen in between the above mentioned values. Depending on the measured impedance it was sometimes necessary to empirically vary these values to find a global optimum.

III. Control hardware

The basic structure of a power supply with controller, ADC and interface to the control system is shown in Fig. 6., while Fig. 7. shows the block diagrams of the developed DSP- and ADC-card.

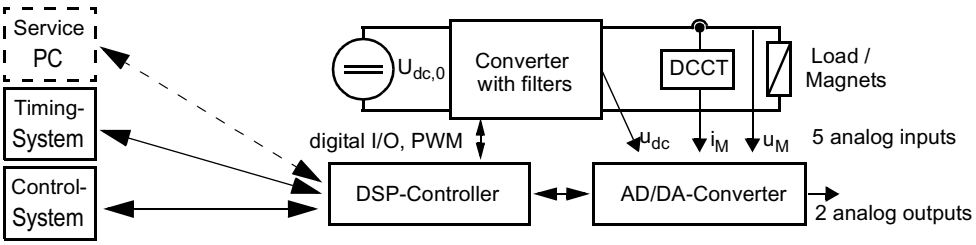

Fig. 6. PS control structure overview

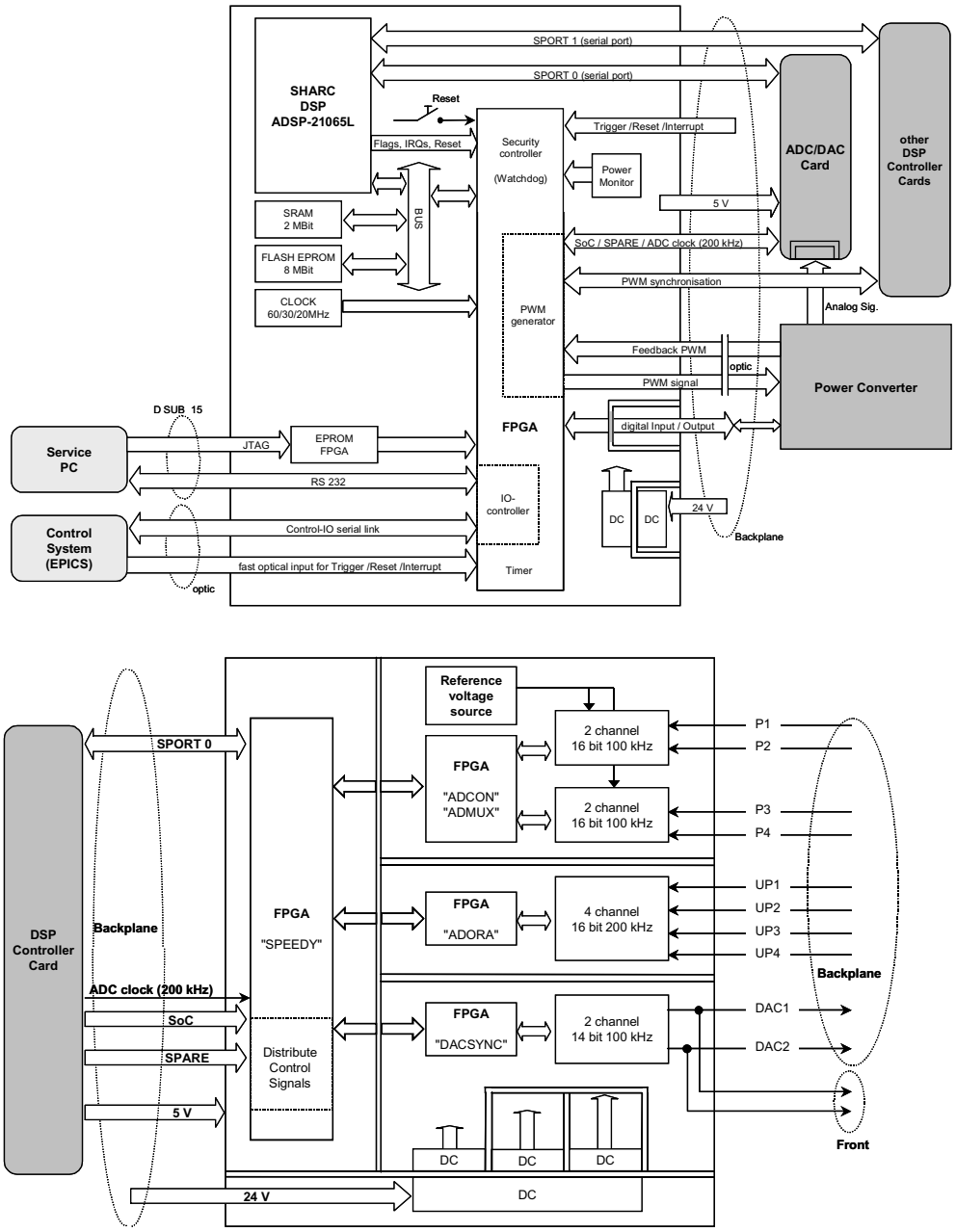

Fig. 7. Top: Functional block diagram of the DSP-card,
bottom: Functional block diagram of ADC/DAC card

III.1 DSP-card

The core of the DSP-card is an Analog Devices SHARC digital signal processor with floating point capabilities. The on card clock frequency is 30MHz, inside the DSP 60MHz. The flexibility is enhanced with a large field programmable gate array (FPGA) which performs all the communications. For the precise converter control a fully digital pulse width modulator was developed [3] and also implemented in the FPGA. 16 digital inputs and 8 outputs are fed via opto couplers, while the fast PWM signals and the communication with the control system uses fibre optics with 5Mbaud. Multiple cards can be connected together via the fast serial link (20Mbaud) of the DSP (SPORT) in order to get multiprocessor capability. The fast communication with the ADC-card is performed via the second fast serial link.

III.2 ADC- / DAC- card

The ADC's are the key parts for the necessary precision of the entire controller. Especially for the current measurement (the output property of the power supply) a final resolution of less than 10 ppm is required, asking for 17 bits plus sign. This measurement is made with two 16 bit two-channel ADCs with self calibrating capability. All four channels are used in parallel for the current measurement. At full speed they deliver values at a rate of 200kHz. Additional oversampling technique and filtering properties of the whole circuit give the desired quality of the current measurement. The precision voltage reference used for these ADCs is additionally temperature stabilised.
Another 4-channel ADC is used for differential voltage measurements of the power supply's dc-link and the load. These measurements have reduced requirements compared to the output property. However, they still have a resolution of 16 bit at 50kHz per channel!

Two 14bit 50kHz DAC- channels are used to monitor any internal property of the controller by an oscilloscope for maintenance and trouble shooting.

IV. Control concept

The goal was to find a simple but robust control structure that fulfils the high demands. This resulted in a nonlinear PI-structure of the well known form of Fig. 8. For the suppression of the dc-link ripple a nonlinear feed forward is implemented. In addition, a limiter for the *du/dt* was necessary to protect the output filters of the PS. *d/dt*-limiters and filters for the reference value, as well as for the measured properties, are needed. Last but not least, an anti wind up feed back is implemented.

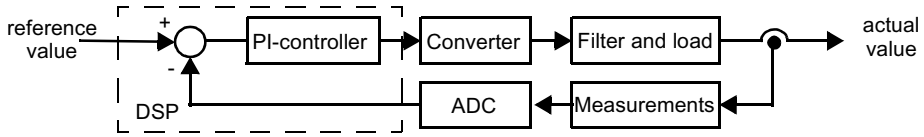

Fig. 8. Basic structure of the closed loop control for the PS

IV.1 PI-controller

The coefficients of the PI-controller are determined in a proven way: Of the entire PS a linear model is derived. From this model the open loop frequency response is simulated. According to the rules of Bode the P- and I-coefficients are determined for various points of operation.

IV.2 DC-link voltage feed forward

DC-link voltage variations influence the converter output voltage. Again, this will cause variations of the load current which will be corrected by the controller - but, delayed. Especially voltage fluctuations of a medium speed are critical: fast pulses are filtered by the output filter while slow fluctuations are well corrected by the control loop. With an appropriate voltage feed forward the influence of dc-link voltage pulsations on the converter output can be reduced. Based upon the transfer function of the converter in (1)it is obvious that for a constant output voltage the product mu_e has to be kept constant. A variation of u_e has to be compensated with an appropriate change of m. Starting with the linearised equation (6)for the output voltage the feed forward coefficient for Δu_e in (7)can be derived.

$$\Delta u_a = m_0 \Delta u_e + \Delta m u_{e,0} = 0 \tag{6}$$

$$\Delta m = (-m_0 / u_{e,0}) \Delta u_e \tag{7}$$

The operation can be performed with the blocks shown in Fig. 9.. The differentiation is performed with

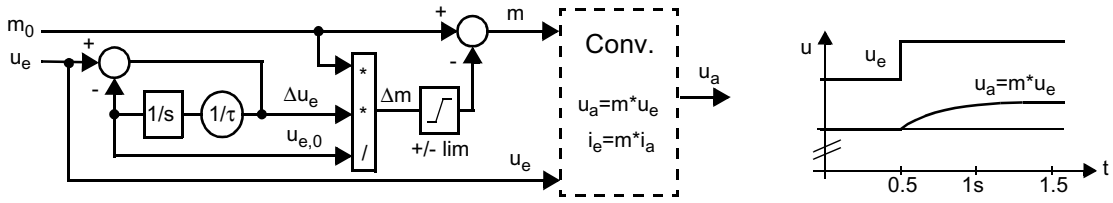

Fig. 9. Left: Block diagram of the voltage feed forward with the derivative block for $\Delta u_{e,}$ right: $u_a=f(u_e)$ with voltage feed forward $(m_0 \approx 0.9)$

help of a low pass filter. The time constant of the integration has to be chosen so, that the not compensated slow variation of the output voltage can be compensated by the current controller. A to dominant influence of this feed forward function can be limited by limiting Δm. This is in any case necessary at start up.

IV.3 Low pass filter and di/dt-limiter

For the measured values simple low pass filters are implemented on the DSP as shown in Fig. 10. left. The well known transfer function in (8)results.

$$Y/X = 1/(s\tau + 1) \tag{8}$$

The voltage ratings of the PS are designed for a maximum di/dt in the load. Therefore, a limiter for the reference value is needed. This limiter is combined with a low pass filter as depicted in Fig. 10. right.

Fig. 10. Left: simple low-pass filter, right: combination with maximum d/dt-limiter

The upper and lower value of the limiter block determine directly the maximum *dy/dt*. An additional limiter at the input can be implemented to limit the range of the output *y*.

IV.4 dm/dt-limiter

The damping resistor R_{a6} of the output filter in Fig. 2. can be destroyed with over current. A simple worst case consideration leads to two limits: If all the filter elements are omitted the current through the resistor is limited to $i_{Ra6} \approx C_{a5} du_M/dt$ for low frequencies. If the magnet voltage oscillates with the maxim *du/dt* a rectangular current flow through the resistor results. For a given power dissipation P_V the maximum *du/dt* is given with (9).

$$P_V = R_{a6} I_{Ra6}{}^2;\ I_{Ra6} = C_{a5}\frac{du_M}{dt};\quad \Rightarrow \frac{du_M}{dt} = \sqrt{\frac{P_V}{R_{a6}}}\frac{1}{C_{a5}} = \frac{dm}{dt}u_e \tag{9}$$

For high frequencies the capacitor C_{a5} can be neglected and the magnet voltage is identical to the voltage over the damping resistor. Therefore, this contribution to the dissipated power can be limited by a limitation of the output voltage of the converter. For a square wave voltage (10)results.

$$P_V = U_M{}^2 / R_{a6}; \quad \Rightarrow \hat{u}_M = \sqrt{P_V R_{a6}} = \hat{m} u_e; \quad \Rightarrow \hat{m} = \hat{u}_M / u_e \tag{10}$$

In our case the allowed losses are divided evenly between the two phenomena. The filter will reduced the calculated values further. The implementation of both limiting functions, is shown in Fig. 11.

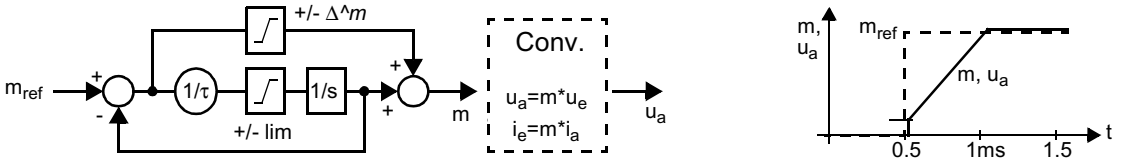

Fig. 11. left: dm/dt-limiter combined with a small signal bypass limiting the possible losses in the damping resistors of the output filter, right: transfer function of the block.

IV.5 Amplitude dependant proportional amplification

Simple buck converter, as well as two quadrant converter, suffer from an increased amplification at small modulation indices [3]. This can be compensated with a reduced amplification of the PI-controller in the range of small currents. The amplification has to be adjusted, according the individual behaviour of each PS.

IV.6 Anti wind-up

The limitation of the PI-controller output is made with a anti wind up structure. In case of a larger than possible output signal the integrator of the controller is taken back. As the controller is realised as a time discrete system, the amplification in the anti wind up loop is limited. To high values will lead to instablities. This limited amplification asks for limited error values in the control loop, as it is shown in the block diagram.
The resulting time discrete controller structure with all the discussed features is shown in Fig. 12.

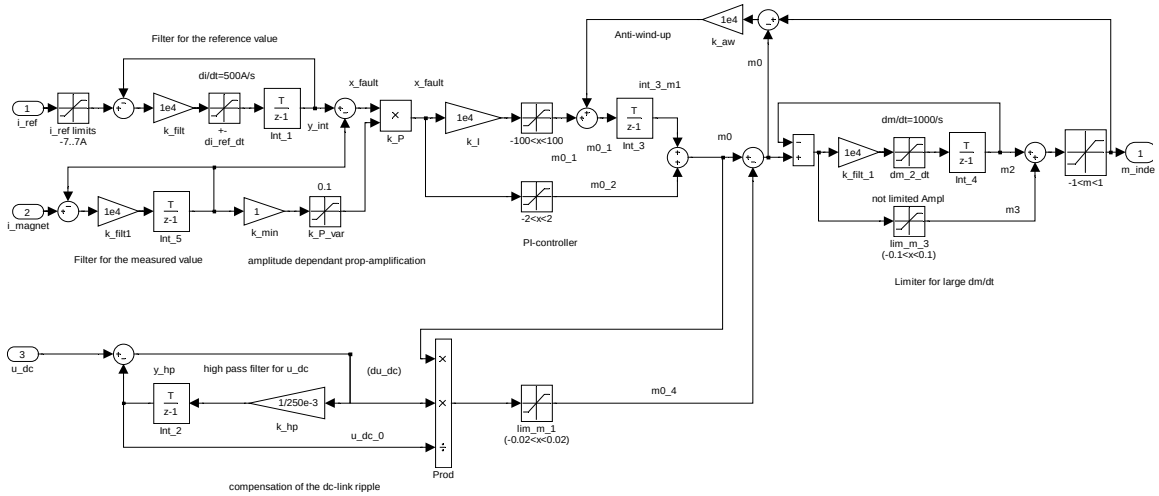

Fig. 12. Complete Simulink block diagram of the controller

IV.7 Diagnostic and supervision functions

A processor based control system allows any number of additional tasks to be performed. In the discussed PS the following are implemented amongst other things: Turn on sequence for the mains voltage with a continuous control of the dc-link voltage. Several temperatures, as well as the load status are

checked. Ground isolation of the load is supervised. Calibration of the ADCs. Most important, the load impedance is continuously supervised. This is also a very useful check of a correct function of the ADCs.

IV.8 Results

Two measurements demonstrate the achieved results: Fig. 13. left shows 2ppm current-steps in a slow but very precise PS. To permit steps with such a small order of magnitude without any visible drift was one of the reason for the chosen solution. On the other hand good dynamic behaviour is asked for, as shown in Fig. 13. right.

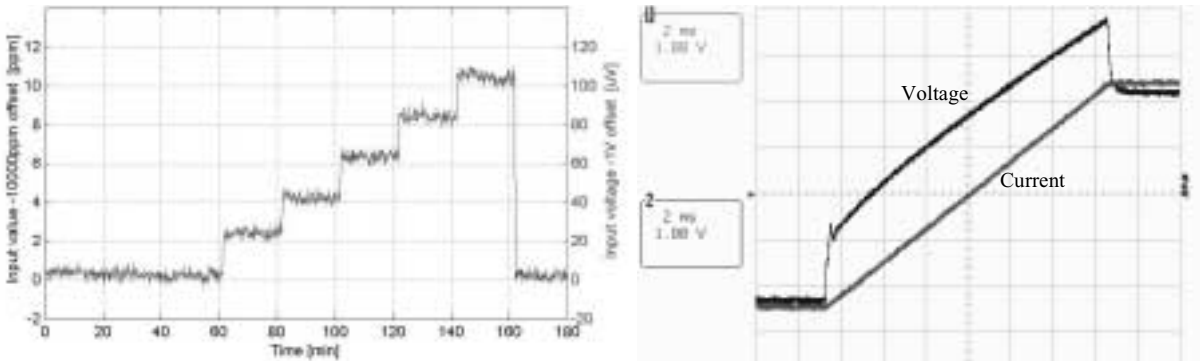

Fig. 13. Left: Step response for 2ppm steps;
right: -5A to +5A current step with maximum di/dt. (2ms/div.)

V. Conclusions

For the first time it was possible to equip all the magnet power supplies for an accelerator with a fully digital control. This required a precise and adequate modelling of filters and converter of the power supply. Very important is the model of the implemented magnets with their properties of: frequency dependent resistance, inductance and multiple resonances. With the implemented hard and software structure the extreme requirements on precision and elevated dynamic were entirely satisfied. The implementation is based on a sophisticated analog-digital conversion, a fully digital PWM and a sophisticated control algorithm. At present, more than 580 units are operational and even exceeding the specifications.

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