Novel Zero-Voltage and Zero-Current-Switching(ZVZCS) Three Level DC/DC Converter Using A Simple Auxiliary Circuit

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Abstract - **This paper proposes a Zero Voltage and Zero Current Switching (ZVZCS) Three-Level (TL) DC/DC converter, which overcomes the drawbacks presented by the Zero Voltage Switching (ZVS) Three-Level converter, such as high circulating energy, severe parasitic ring on the rectifier diodes, and limited ZVS load range for the lagging switches. A simple auxiliary circuit which consists of one small capacitor and two small diodes is added in the secondary to provides ZVZCS conditions to primary switches as well as to clamp secondary rectifier voltage. The additional clamp circuit for the secondary rectifier is not necessary. The auxiliary circuit includes neither lossy components nor additional active switches which makes the proposed converter efficient and cost effective. The principle of operation, features and design considerations are illustrated and verified by experimental circuit.**

Keywords - **auxiliary circuit, three-level, ZVZCS**

I. INTRODUCTION

To Improve the input power factor in the utility side, a three-phase ac/dc boost converter has been used. However, in order to reduce the harmonic distortion in this converter, its input to output voltage characteristic has to be increased, therefore, it also increase the voltage stress in the dc/dc step down second stage converter. Three-level (TL) dc/dc converter [1] has been attracted more and more attentions in high voltage and high power conversion applications because its power switches suffer only the half of the input voltage, as shown in Fig. 1:

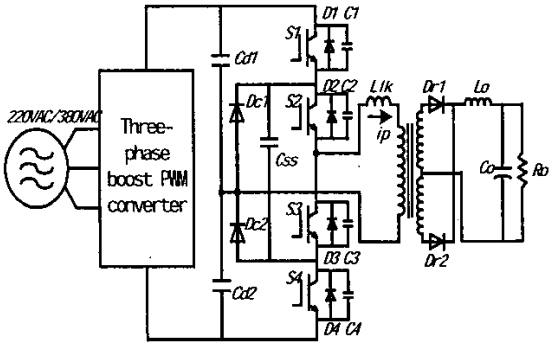

Fig.1 Three-level ZVS dc/dc converter

However, the conventional three level ZVS phase-shifted dc/dc converter has a disadvantage that the primary circulating current that is the reflected output current *nIo* flows through the transformer and switching devices during the freewheeling interval, which will cause higher switching loss in high power applications using IGBTs because of tail current . Therefore, to operate IGBTs at higher switching frequencies, it is required to reduce the turn-off switching loss.

Zero Voltage and Zero Current Switching (ZVZCS) techniques for the three level converter have shown that they can eliminate this major limitation presented in the ZVS techniques. The ZVS of leading-leg switches is achieved by the same manner as that of the ZVS three level PWM converter while the ZCS of lagging-leg switches is achieved by resetting the primary current during the freewheeling period. So far, a couple of ZVZCS-TL-PWM converters have been presented but their primary currents during freewheeling period are reset by different manners: In the converter [2], the primary current is reset by adding an active clamp in the secondary side which provides ZVZCS condition to the primary switches as well as active clamp of secondary rectifier. Additional switch, however, makes switching loss due to hard switching and increases cost and control complexity. In the converter [3], the primary current is reset by using a saturable reactor, but the saturable reactor loss limits the maximum power level.

This paper proposes a novel ZVZCS-TL-PWM converter, as shown in Fig. 2. The ZVS mechanism of leading-leg switches is also the same as that of the converters in [1]~[4]. A simple auxiliary circuit [5] provides not only ZVZCS condition to the primary switches but clamping of the secondary rectifier. Therefore, most of the problems of the previous ZVZCS converters are solved and furthermore additional passive or active clamp circuit is not necessary.

II. ZVZCS THREE - LEVEL DC/DC CONVERTER

The proposed converter has eight operation stages during a half switching cycle. The circuit uses the well known phase shift control with turn on and turn off of nearly 50% duty cycle. The phase shift between *S1* and *S2* or *S3* and *S4* determines the operation duty cycle of

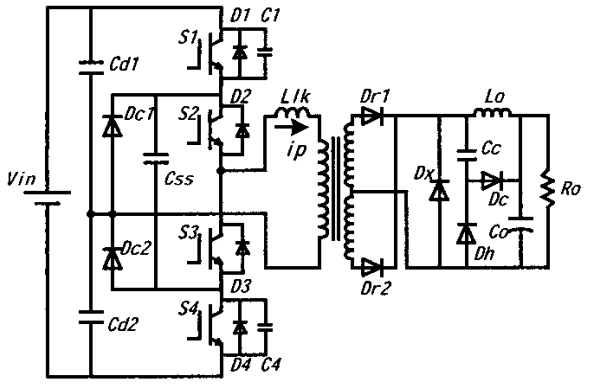

Fig.2 The proposed ZVZCS TL dc/dc converte

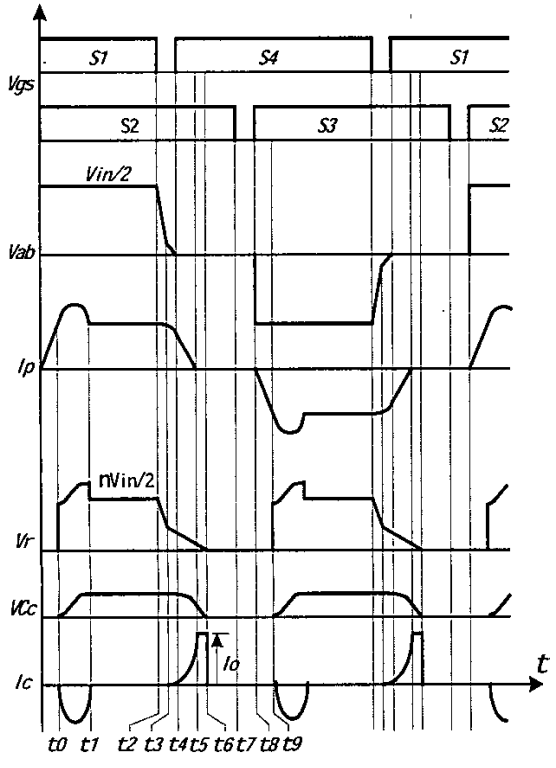

Fig.3 Operation waveforms

the converter. The operating waveforms and equivalent circuits are shown in Fig. 3 and Fig. 4, respectively. To illustrate steady state operation, it is assumed that all components and devices are ideal and the output filter inductor is a constant current source.

Mode 1[*t0-t1*]: During this stage, *S1* and *S2* are conducting and the input power is delivered to the output. The clamping capacitor voltage V_{Cc} is charge up through *Dc* and *Co* by the resonant with leakage inductance as shown in Figure 4. The *VCc* reaches twice of ($nV_{in}/2-V_o$) after a half resonance period (*Llk* and *Cc*) at the end of this mode, where *n* is the transformer turns ratio. The rectifier voltage starts from *Vo* and reaches $V_{Cc}+V_o$ as shown in Fig. 3. The detailed equivalent circuit is shown in Figure 4.(To simplify the explanation of operation, The junction capacitance of the secondary rectifier diode is ignored.) The primary current and the clamping capacitor voltage can be obtained as follows:

$$I_P(t) = nI_o(1-\cos(\omega_\alpha t)) - \frac{\frac{V_{in}}{2}-\frac{V_o}{n}}{Z_\alpha}\sin(\omega_\alpha t) + nI_o \quad (1)$$

$$V_{Cc} = \frac{nV_{in}}{2}(1-\cos(\omega_\alpha t)) - n^2 Z_\alpha I_o \sin(\omega_\alpha t) \quad (2)$$

where, $Z_\alpha = \sqrt{\frac{L_{lk}}{n^2 Cc}}$, $\omega_\alpha = \frac{1}{n\sqrt{L_{lk}Cc}}$

Mode 2[*t1-t2*]: *Dc* is turned off and the rectifier voltage is returned to the nominal value, $nV_{in}/2$. The *Dh* is never turned on during this mode unless the duty cycle is smaller than 0.5. The input power in still delivered to the output during this mode.

Mode 3[*t2-t3*]: *S1* is turned off and then the current through the primary charges *C1* and discharges *C4*. The primary voltage is linearly decreased and the secondary rectifier voltage is also decreased with the same rate.

$$V_{ab}(t) = \frac{V_{in}}{2} - \frac{nI_o}{C_1+C_4}t \quad (3)$$

$$V_{rect} = nV_{ab}(t) \quad (4)$$

Mode 4[*t3-t4*]: When the rectifier voltage reaches the holding capacitor voltage V_{Ch}, the diode *Dh* is turned on and the *Cc* holds the rectifier voltage, which means the rectifier voltage decreases much slower than the primary voltage. The primary voltage keeps decreasing with almost same rate as before since the stored energy in the leakage inductance still charges *C1* and discharges *C4*. (*Cc* is much larger than *C1* or *C4*.) The difference between the primary voltage and the reflected secondary voltage is applied to the leakage inductance and the primary current starts decreasing. The voltage and current of circuit are as follows:

$$V_{ab}(t) = \frac{nI_O}{\omega_\beta}\left(\frac{1}{\omega_\beta^2} - \frac{1}{C_{eq}}\right)\sin(\omega_\beta t) - \frac{I_O}{n\omega_\beta^2}t + 2V_{Lo} \quad (5)$$

$$I_P = nI_o\left(1-\frac{C_{eq}}{\omega_\beta^2}\right)\cos(\omega_\beta t) + \frac{C_{eq}nI_O}{\omega_\beta^2} \quad (6)$$

$$V_{Cc}(t) = -\frac{I_O C_{eq}}{Cc\omega_\beta^2}\sin(\omega_\beta t) + \frac{I_O C_{eq}}{Cc\omega_\beta^2}t + 2V_{Lo} \quad (7)$$

where, $\omega_\beta = \sqrt{\frac{n^2 Cc + C_{eq}}{n^2 L_{lk} Cc C_{eq}}}$, $C_{eq} = C_1 + C_3$

Mode 5[*t4-t5*]: The *C4* is completely discharged and then *S4* is conducting with ZVS. The reflected secondary voltage is applied to the leakage inductance and the primary current decreases quickly. The *Cc* supplies more current to the load. The primary current reaches zero at the end of this mode.

Mode 6[*t5-t6*]: In this mode, the primary current is completely reset and no current flows through the

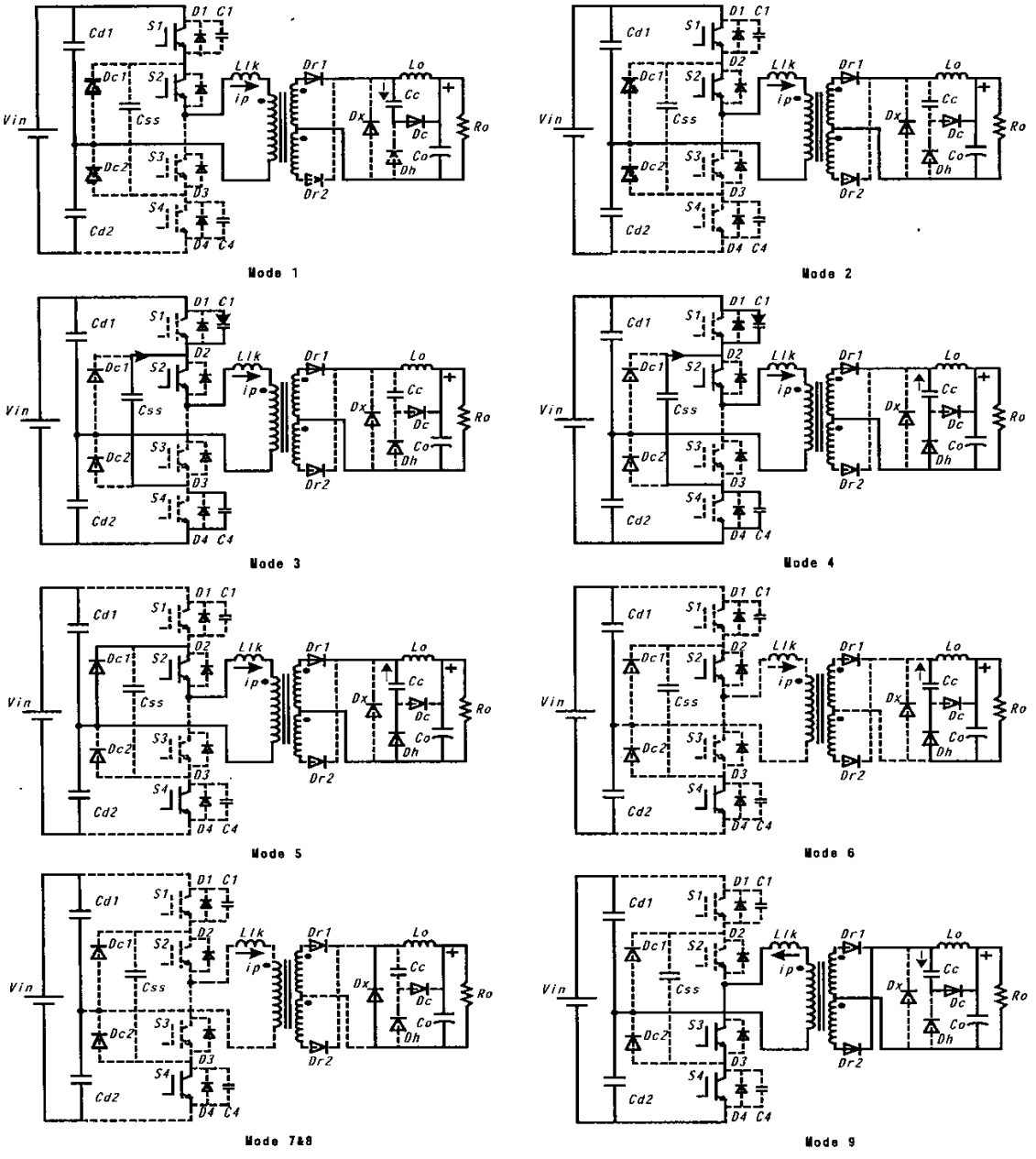

Fig.4 Equivalent circuits for each operating mode

primary. Then the *Cc* supplies whole load current and thus the secondary rectifier voltage is decreased quickly. The holding capacitor voltage is obtained as follows:

$$V_{Cc} = -\frac{I_o}{Cc}t + V_{t5} \tag{8}$$

Mode 7*[t6-t7]*: When the *Cc* discharges completely, the diodes *Dx* starts to conduct and the load current freewheels through *Dx*.

Mode 8*[t7-t8]*: At the end of freewheeling period, *S2* is turned off with complete ZCS since there is no current through the device. This mode is a dead time between *S2* and *S3*.

Mode 9*[t8-t9]*: *S3* is turned on. The primary current is linearly increased as follows:

$$I_p(t) = \frac{V_{in}}{2L_{lk}}t \tag{9}$$

The rectifier voltage is still zero. This is the end of an operating half-cycle.

III. DESIGN CONSIDERATION

A. *Design of the Auxiliary Circuit*

Due to the resonance between the leakage inductance and the auxiliary circuit, the peak rectifier voltage is not constant and it depends on the duty cycle as follows:

$$V_{rect-pk} = nV_{in}(1-\frac{D}{2}) \tag{10}$$

From (10) we can see that the peak rectifier voltage is inversely proportional to the duty cycle and the duty cycle should be high to get low rectifier voltage stress. And during the charging mode, the peak current through Cc is as follows:

$$I_{Cc(\max)} = \frac{V_{rect-pk} - \frac{nV_{in}}{2}}{\sqrt{L_{lk}/Cc}} \tag{11}$$

then the maximum value of primary current is:

$$I_{p(\max)} = nI_{o(\max)} + nI_{Cc(\max)} \tag{12}$$

From (10), (11) and (12), the value of Cc can be derived as follows:

$$Cc = \left[\frac{2(I_{p(\max)} - nI_{o(\max)})}{n^2 V_{in}(1-D)}\right]^2 \cdot L_{lk} \tag{13}$$

We can suppose that: $I_{p(\max)} = 1.15nI_{o(\max)}$, and then the value of Cc is determined.

B. *ZCS Range of Lagging-Leg*

The ZCS of lagging-leg is achieved by resetting the primary current and the primary current is reset by the auxiliary capacitor voltage. At light load, the auxiliary capacitor voltage may not be discharged completely. In this case, the peak voltage is reduced because the load current is decreased. Then, the primary current reset time may be increased. The primary current, however, is also decreased as the load current is decreased and the ZCS of lagging-leg can be achieved by lower auxiliary capacitor voltage. So, the ZCS range of lagging-leg is wide enough.

IV. EXPERIMENTAL RESULT

A 2.5 kW, 40kHz prototype of the ZVZCS-TL-PWM converter has been built and tested to verify the principle of operation.

The specifications of the experimental circuit are as follows:

DC input voltage: 500VDC ±10%
Output voltage: 48VDC
Output current: 53A
Switching frequency: 40KHz

The power stage shown in Fig. 2 consists of the following components:

S1-S4: IGBT(1MBH60D-100)
D1-D4: the IGBT's body diodes of *S1-S4*
C1,C4:1nF/1600V-polypropylene
Dr1-Dr2: DSEI 2*12-02A
Dc1-Dc2: DSEI 30-10A
Llk: 6uH
Css: 4*0.47 f/630V-polypropylene
Cc: 1uF
Lo: 20uH
Co: 3300uF

The turns-ratio of the transformer is designed to achieve high output voltage at low voltage conditions. Then the transformer is selected to be a center tap transformer with turns-ratio equal to 4 and 12/3/3 turns in the primary and secondary, respectively.

Experimental waveforms of the proposed converter at 10% and full load are shown in Fig. 5, 6, 7, 8 and 9.

Fig. 5 and 6 shows the drain to source voltage (lower trace), V_{DS}, across the power switch *S1* and its gate signal voltage (upper trace) at 10% load and full load. Which illustrate that the leading switch can realizes ZVS with wide load range. Also, it can be seen that the value of V_{DS} is about 250 Volts, just half of the input voltage.

Fig. 7 and 8 shows the ZCS waveforms of lagging-leg switches at 10% load and full load. The switch *S2* is turned off with complete ZCS since the current through it is zero before turning off. There is no IGBT tail current due to ZCS.

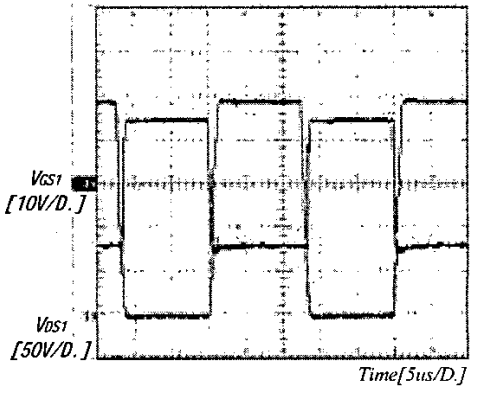

Fig.5 Drain to source and gate voltage waveforms of *S1* at 10% load

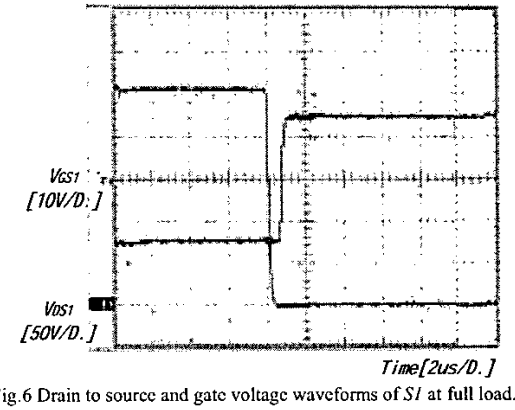

Fig.6 Drain to source and gate voltage waveforms of *S1* at full load.

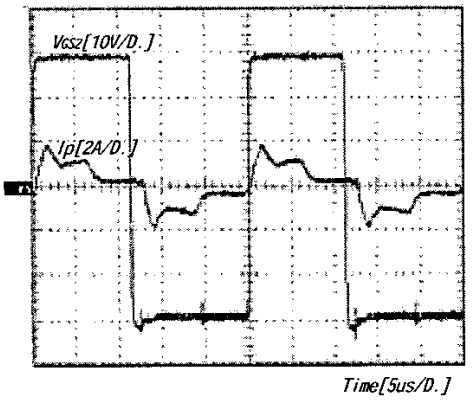

Fig.7 ZCS waveforms of lagging-leg switch *S2* at 10% load.

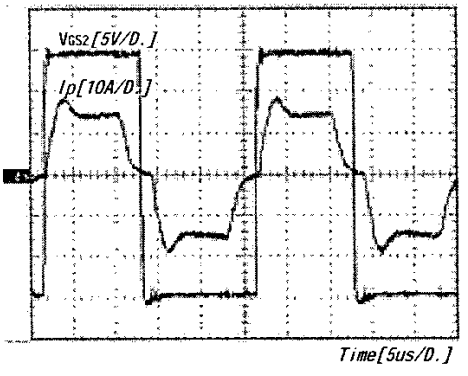

Fig.8 ZCS waveforms of lagging-leg switch *S2* at full load

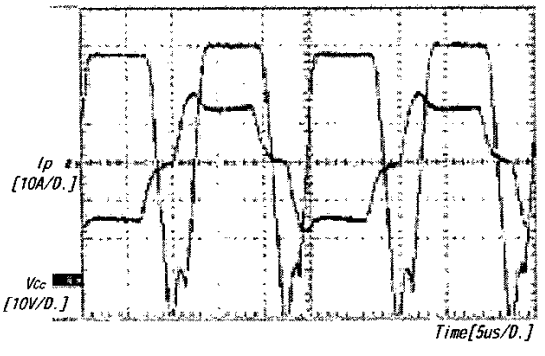

Fig.9 Waveforms of auxiliary capacitor voltage and primary current at full load

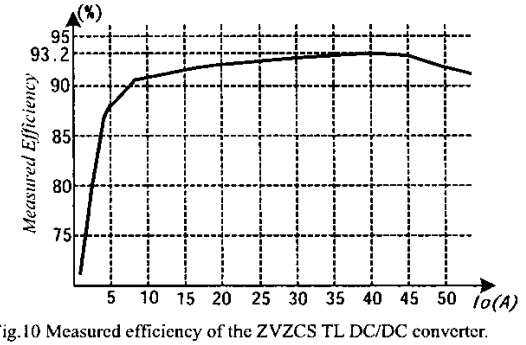

Fig.10 Measured efficiency of the ZVZCS TL DC/DC converter.

Fig. 9 shows the waveforms of auxiliary capacitor voltage and primary current at full load. The auxiliary capacitor voltage goes to the negative, which is because of the stray inductance of rectifier.

Fig. 10 shows the measured efficiency of the proposed converter. Maximum efficiency of the proposed converter is 93.2%. Even at the 10% load, the efficiency of the converter is about 90%.

V. CONCLUSION

An improved ZVZCS-TL-PWM converter using a simple auxiliary circuit is presented. The operation, analysis, and design considerations are illustrated. Experimental results from the 2.5kW, 40KHz IGBT based prototype is shown to verify the operation principle.

It is shown that ZVZCS of the primary switcher are achieved by adding a simple auxiliary circuit in the secondary. The auxiliary circuit is consist of a small capacitor and two small diodes. Most of problems of the previously presented ZVS and ZVZCS TL converters are solved as follows: no lossy components are involved; no additional active switch, no additional device voltage stress and low device current stress. Distinctive advantages of the new circuit including ZVZCS with wide load range (IGBTs can be used), small duty cycle loss, and low cost make the proposed converter very promising for medium power (>2kW) applications with high power density.

REFERENCE

[1] J.Renes Pinheriro, Ivo Barbi, "The Three-level ZVS PWM Converter A New Concept In High Voltage DC-To-DC Converter", IECON, 1992, pp.173-178.

[2] F.Canales, P.M.Barbosa and F.C.Lee, "A Zero Voltage Current Switching Three Level DC/DC Converter," IEEE APEC, 2000, pp.314-320.

[3] E.S.Kim, Y.B.Byun and Y.H.Kim, "An Improved Three Level ZVZCS DC/DC Converter Using A Tapped Inductor And A Snubber Capacitor," IEEE, 2002, pp.115-121.

[4] F.Canales, P.M.Barbosa, J.M.Burdio, and F.C.Lee, "A Zero-Voltage Switching Three-level DC/DC Converter," Proceedings of CPES,2000, pp.366-371.

[5] J.C Cho, J.W Back etc, "Novel Zero-Voltage and Zero-Current-Switching (ZVZCS) Full Bridge PWM Converter Using A Simple Auxiliary Circuit," APEC, 1998, pp.834-839.

[6] Jung-Goo Cho, Ju-Won Back, Chang-Yong Jeong, etc, "Novel Zero-Voltage and Zero-Current-Switching Full Bridge PWM Converter Using Transformer Auxiliary Winding", IEEE Trans. Power Electron., vol.15, No.2, March 2000, pp.250-256.

[7] Xinbo Ruan, Dayu Xu, and Yangguang Yan, "Zero-voltage-switching pwm three-level converter with two clamp diodes," Proceedings of IEEE PESC, 2001, pp.612-622.