

Photoflash Capacitor Charger

REV: 01

General Description

The LD7261 is an ideal charge control IC for flash units with internal soft start, adjustable charging current and output voltage. It provides a proprietary charging algorithm, which charges photoflash capacitor quickly and efficiently. The LD7261 is specially designed for automatically and linearly lowering the charging current at lower battery voltage. As well, a built-in totem pole IGBT driver can drive IGBT quickly and save the board space.

The LD7261 is available in a space-saving MSOP-10 package and is ideal for DSC flash unit.

Features

- Adjustable Charging Current
- Adjustable Output Voltage
- Supports Auto Refresh
- 1.8V~5V Battery Voltage Range
- Internal Soft Start
- Tiny Transformer
- Totem-Pole IGBT Driver

Applications

- **DSC Flash Unit**
- Film Camera Flash Unit

† Patented

Typical Application D1 V_{OUT} < VIN ₹C1 $33\mu F$ C2 160μF ZD1, < Vcc 300V C3 ‡ 1μF ↓ C3 |k Q1 VCC OUT1 **VDD** FΒ ISET R2 } C4 SEC R_{I} CHARGE RS R1 LD7261 3.9Ω 100K CHARGE **READY** READY TRIGGER TRIGGER OUT2 R_G **IGBT GATE GND**

Q1: AOS / AO3402,

T1: 10T: 250T, Lp=8μH / EFD 6.5 (12T: 300T, Lp=10μH/EFD6.5)

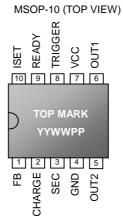
ZD1:Origin / FC0300M

C_S: 4.7~10nF R_I: >600K

Fig. 1



Pin Configuration



YY: Year code WW: Week code PP: Production code

Ordering Information

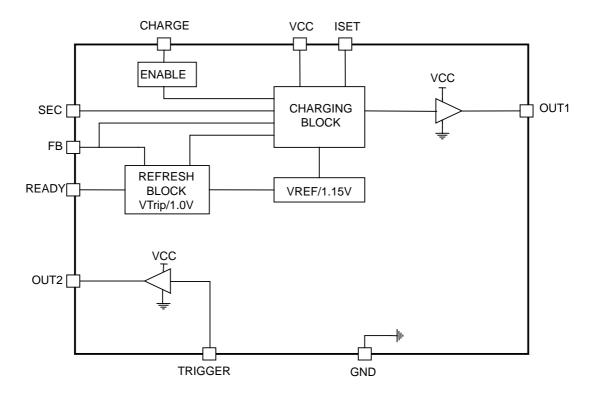
Part number	Package	Top Mark	Shipping
LD7261 CL	MSOP-10	7261CL	2500 /tape & reel
LD7261 PL	MSOP-10 (PB FREE)	7261PL	2500 /tape & reel

Pin Descriptions

PIN	NAME	FUNCTION
1	FB	Output voltage feedback
2	CHARGE	Charging on/off control pin. High=enable low=disable
3	SEC	Secondary winding pin
4	GND	IC GND
5	OUT2	Totem-pole output (IGBT driver)
6	OUT1	Totem-pole output (MOS driver)
7	VCC	Input power of IC
8	TRIGGER	Trigger on/off control pin. High=enable low=disable
9	READY	Charge ready open drain output.
10	ISET	Adjust charging current with R to GND.



Block Diagram



Absolute Maximum Ratings

Supply Voltage Vcc.	-0.3~6.0V
SEC pin	-0.6~(Vcc+0.3) V
FB, Charge, Trigger, ISET pin	-0.3~(Vcc+0.3) V
Operating Temperature Range	-30°C to 85°C
Storage Temperature Range	-55°C to 125°C
Junction Temperature	125°C
Lead Temperature (Soldering, 10sec)(LD7268APL)	260 °C
ESD Level (Human Body Model)	2KV

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not limited.

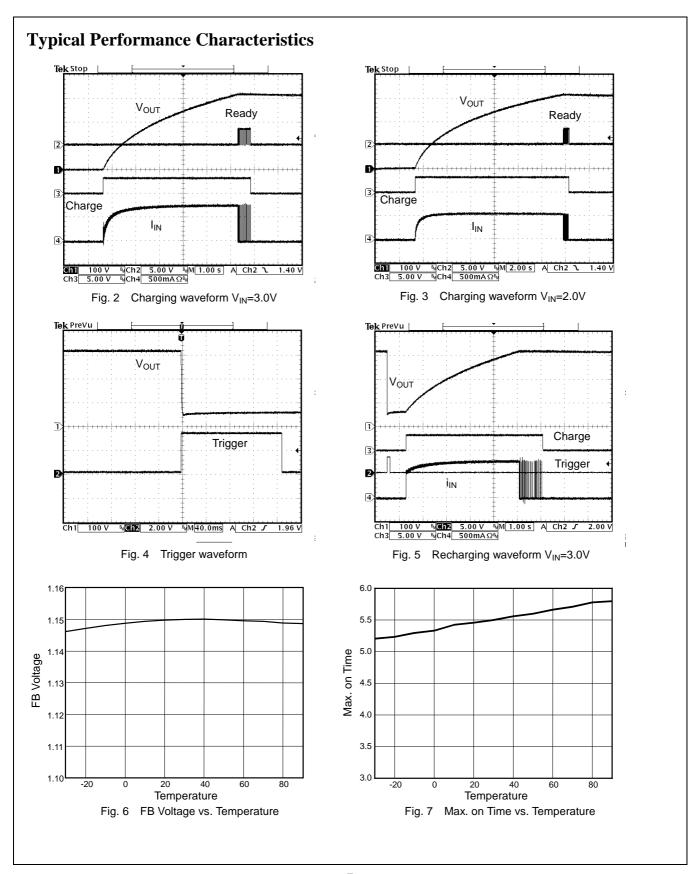


Electrical Characteristics

 $(T_A = +25^{\circ}C \text{ unless otherwise stated}, V_{CC}=3.3V)$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Power					
Operating Voltage V _{CC}		2.2		5.5	V
Standby Current I _{CC}	Charge Off		100		μΑ
Nominal Supply Current	V _{CC} =3.3V, D=50%		0.6		mA
FB					
Reference Voltage			1.15		V
Reference Voltage Tolerance				1	%
Auto Refresh Ref. Voltage1	V _{REF} 1/V _{REF}		88		%
MOS Driver					
Rising Time	V _{CC} =3.3V,C _L =1nF		50		nS
Falling Time	V_{CC} =3.3 V , C_L =1 nF		50		nS
IGBT Driver					
Output ON resistor	V _{CC} =3.3V		8	12	Ω
Output OFF resistor	V _{CC} =3.3V		6	9	Ω
ON/OFF		-			
Trigger On/Off	Enable	2.0			V
Trigger On/Off	Disable	2.0	0.8	V	
Charge On/Off	Enable	2.0			V
Charge On/Off	Disable			0.8	V
Impedance to GND					
Charge Pin to GND			200K		Ω
Trigger Pin to GND			200K		Ω
Others		_		1	
Max Turn On Time	R _I Open		5.5		μS
Max Turn On Time Tolerance				6.6	%
Propagation Delay	(Trigger=High) delay to OUT2		60		nS







Function Description

Transformer Selection

A carefully chosen transformer could result in best performance of the LD7261. The following are the tips for choosing it.

- (1) $L_P=8\mu H$, for 2AA battery (1.8V~3.5V).
- (2) L_P=10μH, for Lithium battery (2.8V~4.2V).

Also, the turn ratio of the transformer should be considered. Choose it according to the VDS rating of Q1. For example, if V_{DS} rating of Q1 is 30V, then please choose N=25.

Adjust Charging Current

The LD7261 provides a flexible way to adjust charging currents.

Just adjust R_I to achieve the desired peak primary charging

$$R_{I} \approx \frac{1.15}{(\frac{33 \times V_{BAT}}{L_{p} \times I_{p}} - 6.2)} M\Omega$$

L_P: primary inductance (μH)

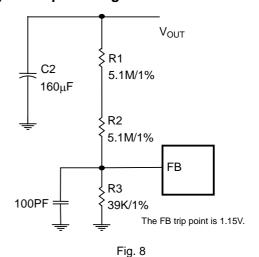
I_P: desired peak primary current (A)

V_{BAT}: battery voltage (V)

Ex: If the desired I_P is 1.6A, L_P =8 μ H, V_{BAT}=3.0V, then R_I=750K/1%

Please always keep R_I larger than 600K to remain the proper operation in the voltage range of 1.8V~5V. If the Ri mentioned above can't meet the application, please use larger Lp to adjust smaller Ip and vice versa.

Adjust Output Voltage



The LD7261 could sense output voltage by using an output resistor divider or a high voltage zener diode.

Fig. 8 shows the application circuit of resistor divider.

$$V_{OUT} = V_{FB} \times (1 + \frac{R1 + R2}{R3})$$

Auto Refresh

The LD7261 supports auto refresh function for some DSC systems.

When V_{OUT} reaches its target value and the READY pin goes high, it means that the output voltage is high enough for the strobe to trigger. Then, V_{OUT} will decrease slightly due to some leakage currents.

The refresh block trip point is 1.0V (1.15V*88%).

Please refer to Fig. 1.

While using a high voltage zener diode to detect Vout, the refresh time could be easily set by R2 and C4,

Trefresh =0.12 R2*C4

For R2=1M and C4=100nF,

Trefresh =12mS

When V_{FB} is decreased to the refresh trip point, it enables



the charging block and disables the refresh block. At the same time, the ready pin goes low, indicating that the LD7261 is in charging mode. This cycle of recharge operation will repeat again until charge pin is pulled low. Thus, the LD7261 could automatically recharge photoflash capacitor to maintain its target value.

To disable auto refresh function, pull low CHARGE pin while the first ready signal goes high.

Interface

CHARGE, READY and TRIGGER can be easily interfaced to a microprocessor.

The CHARGE pin is the on/off control of charging circuit.

High=enable, Low =disable

The READY pin is an indicator of charging and output voltage state.

 $\label{eq:higher_state} \mbox{High= charging is completed and V_{OUT} is still higher} \\ \mbox{than the refresh trip point}$

Low= otherwise

The TRIGGER pin is the on/off control of the strobe to generate a light pulse.

High=enable, Low =disable

Note that the trigger function is only active while the CHARGE pin goes low.

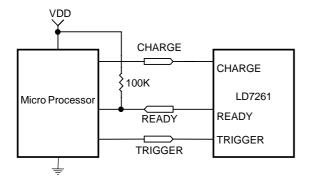


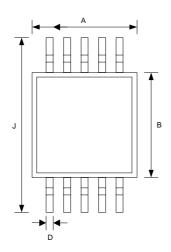
Fig. 9

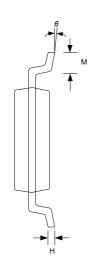
Layout Consideration

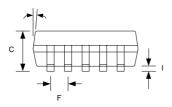
- The layout of this IC should be far away from any high voltage nodes or paths.
- 2. Keep the bypass capacitor $1\mu F$ very close to IC.
- 3. Keep output voltage feed back network, R_I, R2, C4, R_S and C_S very close to the IC.
- 4. The signal ground plane of FB and the SEC pin should be connected to the power ground with a via or only one point to minimize the effect of power ground currents.
- The Switching paths or nodes, such as OUT1, gate or drain of Q1 should be routed away from ISET, FB and SEC pin.
- The PCB traces carrying discontinuous currents and any high current path should be made as short and wide as possible.
- Please refer to the EV kit for the example of the PCB layout.



Package Information MSOP-10







Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
Α	2.896	3.099	0.114	0.122
В	2.896	3.099	0.114	0.122
С	0.813	1.219	0.032	0.048
D	0.152	0.305	0.006	0.012
F	0.470	0.530	0.018	0.020
Н	0.127	0.229	0.005	0.009
ı	0.051	0.152	0.002	0.006
J	4.699	5.105	0.185	0.201
М	0.406	0.660	0.016	0.026
θ	0°	6°	0°	6°

Important Notice

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