A Forward Converter Topology Employing a Resonant Auxiliary Circuit to Achieve Soft Switching and Power Transformer Resetting

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***Abstract*—This paper presents a forward converter topology that employs a small resonant auxiliary circuit. The advantages of the proposed topology include soft switching in both the main and auxiliary switches, recovery of the leakage inductance energy, simplified power transformer achieving self-reset without using the conventional reset winding, simple gate drive and control circuit, etc. Steady-state analysis is performed herein, and a design procedure is presented for general applications. A 35–75-Vdc to 5 Vdc 100-W prototype converter switched at a frequency of 200 kHz is built to verify the design, and 90% overall efficiency has been obtained experimentally at full load.**

***Index Terms*—Forward converter, power transformer, resonant circuit, soft switching, zero-voltage switching (ZVS).**

I. Introduction

IN TELECOM and computer systems, the forward converter topology has been widely used as the dc power supplies for low-voltage and high-current applications with a power level up to 250 W. It employs a single power switch but it has high output current capability, low output voltage ripples, and low input rms current. In addition, it is well understood in industry. Soft-switching techniques are normally used in these applications to achieve high efficiency, high power density, and low electromagnetic interference.

In recent years, some soft-switching forward topologies have been developed, among which are typically the resonant reset forward (RRF) [1]–[3], the active reset/clamp forward (ARF) [4]–[19], and the self-reset forward (SRF) [20]. These topologies not only achieve soft switching but also simplify the forward power transformer by removing the conventional reset winding. A simplified transformer may increase the power density of the converter in addition to reduce its manufacturing costs. However, these topologies have some drawbacks.

The RRF has to be operated with switching frequency modulation to optimize its performance, otherwise the voltage stress on the main switch would be too high. Because the switching ripples and harmonics vary with the variable switching frequency, they become very hard to filter out to meet the noise specifications of the advanced digital systems. The most serious problem with the RRF is the difficulty to drive the synchronous rectifier (SR). In addition, the RRF loses soft switching at light load. When soft switching is lost, the so-called $(1/2)CV^2$ loss related to the MOSFET switch inherent capacitors would be excessive at high switching frequencies. Since this power loss dissipates directly into the switch, it would cause thermal problems on the main switch, even when the conduction losses become negligible at light load. Thus, a large heat sink may have to be used to handle this thermal problem.

The ARF overcomes many of the RRF's drawbacks—it operates at a constant frequency and it is easy to use self-driven SRs. However, a saturable inductor is normally added to achieve zero-voltage switching (ZVS). ZVS may also be achieved by lowering the magnetizing inductance of the power transformer, instead of using the saturable inductor, but this increases conduction losses due to the increased magnetizing current. Circulating current in the clamp circuit results in additional conduction losses.

Other major drawbacks include: 1) the ARF loses ZVS at light load; 2) it requires the variable pulsewidth gating pattern with controllable dead time for the reset/clamp switch; and 3) for the n-channel clamp switch its gate drive shall be isolated from the main switch, and for the p-channel clamp switch it requires a negative bias voltage to turn off.

The SRF overcomes most drawbacks of the RRF and ARF. It employs a simple auxiliary circuit to achieve self-reset of the power transformer and ZVS of the main switch independent of line and load conditions. Besides, the gating of the auxiliary switch is in fixed pulse width and there is no need of gate drive isolation. This greatly simplifies the design of control and gate drive circuits.

However, in the SRF, the auxiliary switch is turned off in hard switching, and the energy of the leakage inductance in the auxiliary circuit is not recovered. These problems limit overall efficiency and the operating frequency to not very high. The auxiliary circuit employs a small flyback-type transformer to store the discharged energy from the snubber capacitor, hence, the auxiliary transformer needs extra processing in manufacturing to have an air gap in the core to prevent saturation.

In this paper, a forward topology employing a resonant auxiliary circuit is presented. In the proposed topology, soft switching is achieved in both main and auxiliary switches, and the energy of the leakage inductance in the auxiliary circuit is recovered, thus to improve the overall efficiency. Self-reset of the power transformer is also achieved without using the

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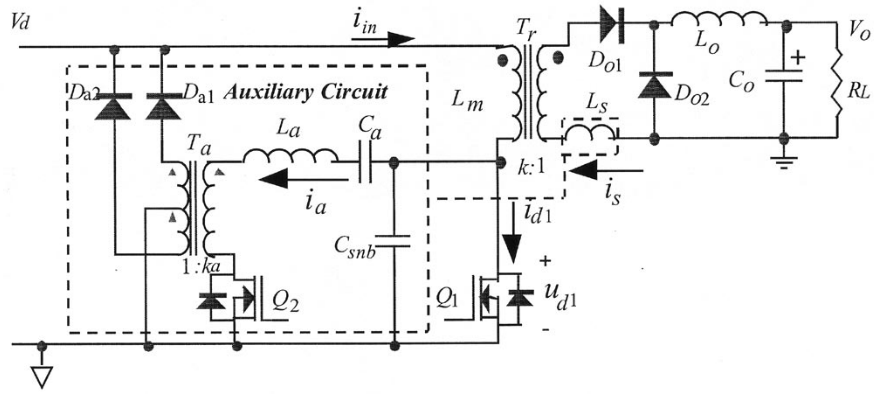


Fig. 1. Proposed ZVS forward converter topology.

conventional reset winding. Unlike the previous SRF, the auxiliary circuit in the proposed topology uses a small forward-type auxiliary transformer that does not require an air-gapped core. Steady-state analysis is performed herein to understand the operation of the circuit and to provide guidance for design. A prototype of 100 W, 35–75 V to 5 V converter operated at 200 kHz is built to prove the concepts of the proposed topology. About 90% overall efficiency is obtained experimentally at full load over the entire range of the input voltage.

II. Circuit Description

Fig. 1 shows the proposed ZVS forward converter topology. It has two functional subcircuits: the power circuit that is the same as the conventional forward converter and the resonant auxiliary circuit.

The power circuit consists of: 1) T_r the simplified power transformer with a magnetizing inductance L_m and a turns ratio of k; 2) Q_1 the main switch; 3) D_{o1} and D_{o2} the output rectifiers; 4) L_o and C_o the output filter; and 5) R_L, the load.

The auxiliary circuit consists of: 1) Q_2, the auxiliary switch; 2) $C_{\rm snb}$ a snubber capacitor for the main switch,; 3) L_s a current limit inductor that is inserted into the secondary side of T_r; 4) L_a and C_a a resonant tank; 5) T_a a center-tapped auxiliary transformer with a turns ratio of k_a; and 6) D_1 and D_2 two auxiliary rectifiers.

The auxiliary circuit fulfills a threefold function: 1) it provides ZVS of the main switch Q_1 at both turn-on and turn-off, thereby eliminating the switching losses of Q_1; 2) it provides zero-current switching (ZCS) of the auxiliary switch Q_2 at turn-on and ZVS at turn-off, thereby removing the switching losses of Q_2; and 3) it resets the transformer T_r.

III. Operating Principle and Steady-State Analysis

Fig. 2 shows key waveforms that highlight the operating principle of the proposed topology. In steady state, each switching cycle can be divided into six intervals.

The following assumptions are made to simplify the steady-state analysis: 1) the input voltage V_d, the rated output power P_o, and the nominal output voltage V_o are all constant; 2) $k_a \ll 1$, and $L_m \gg L_a$; 3) L_o and C_o are infinite; 4) the switches

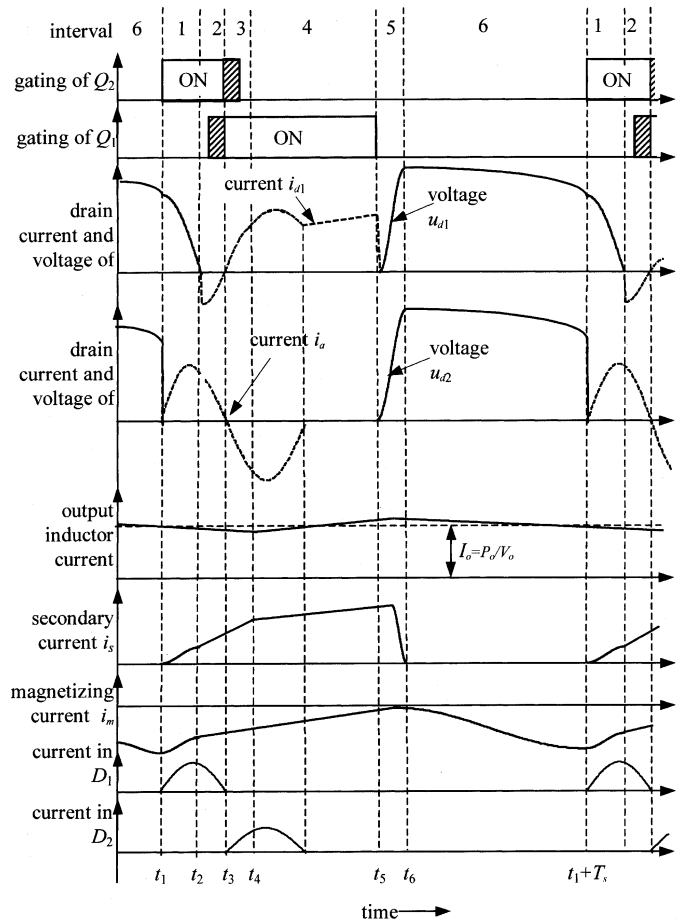


Fig. 2. Key waveforms of the proposed converter topology in steady-state operation.

have negligible Rds(on),; and 5) the capacitors, inductors, transformers, and diodes are ideal devices.

During the last interval of the previous switching cycle, Q_1 and Q_2 are off, D_{a1} is reverse biased, and D_{a2} is in the freewheeling mode to give a path to the output inductor current. No current flows in the auxiliary circuit.

A. Interval 1 ($t_1 \leq t < t_2$)

At the beginning of this interval Q_2 is turned on in ZCS because L_a is in series with it. The equivalent circuit of this in-

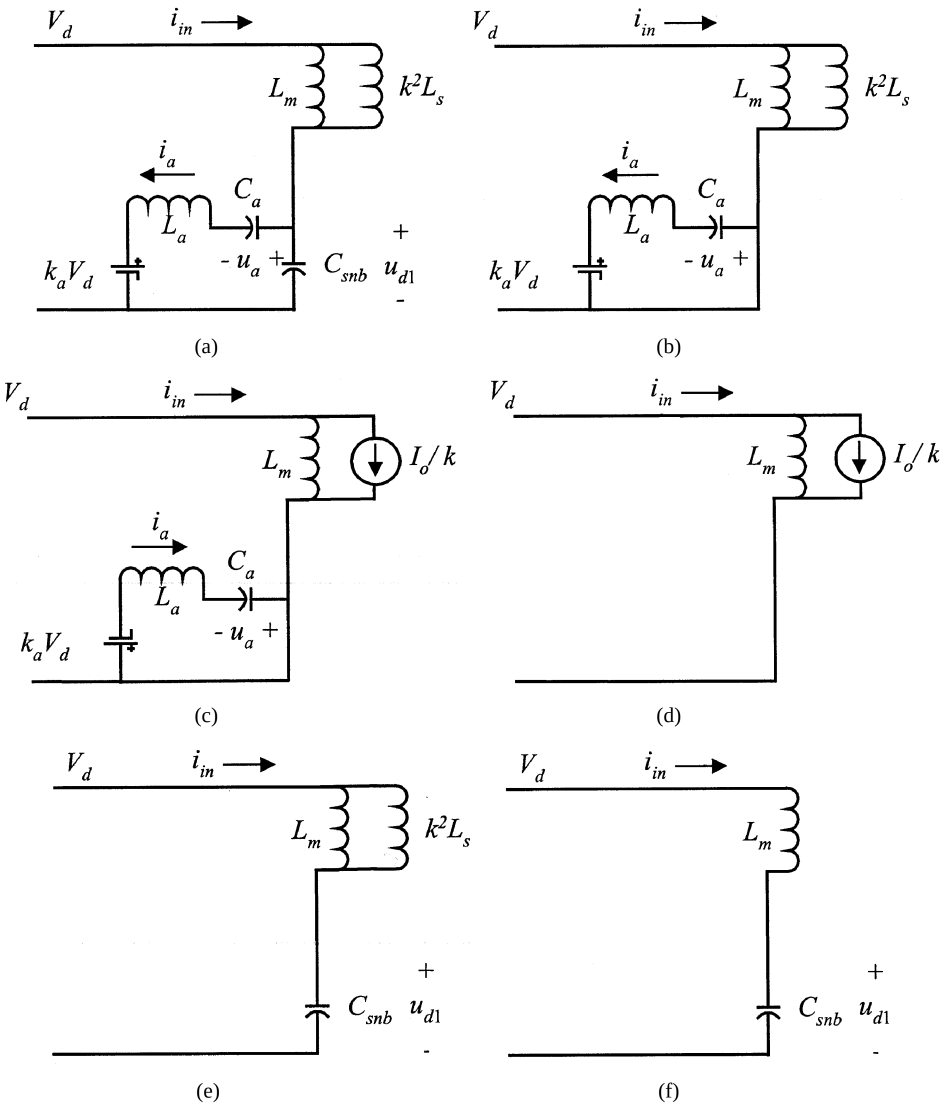


Fig. 3. Equivalent circuits seen from the primary side. (a) Interval 1. (b) Interval 2. (c) Interval 3. (d) Interval 4. (e) Interval 5. (f) Interval 6.

terval is shown in Fig. 3(a), and the following equation governs the drain-to-source voltage u_{d1} of Q_1 during this interval:

$$\alpha \frac{d^4 u_{d1}(t)}{dt^4} + \beta \frac{d^2 u_{d1}(t)}{dt^2} + u_{d1}(t) = V_d \tag{1}$$

where $\alpha = L_a C_a L_e C_{\text{snb}}$, $\beta = L_e C_{\text{snb}} + L_e C_a + L_a C_a$, and $L_e = k^2 L_s L_m / (k^2 L_s + L_m)$.

The solution of (1) is determined by

$$\begin{aligned} u_{d1}(t) = V_d &+ a_1 \cos \omega_1 (t - t_1) + a_2 \sin \omega_1 (t - t_1) \\ &+ a_3 \cos \omega_2 (t - t_1) + a_4 \sin \omega_2 (t - t_1) \end{aligned} \tag{2}$$

where

$$\omega_1 = \frac{1}{2} \sqrt{\frac{2\beta + 2\sqrt{\beta^2 - 4\alpha}}{\alpha}} \tag{3}$$

$$\omega_2 = \frac{1}{2} \sqrt{\frac{2\beta - 2\sqrt{\beta^2 - 4\alpha}}{\alpha}} \tag{4}$$

$$\begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & \omega_1 & 0 & \omega_2 \\ -\omega_1^2 & 0 & -\omega_2^2 & 0 \\ 0 & -\omega_1^3 & 0 & -\omega_2^3 \end{bmatrix}^{-1} \begin{bmatrix} u_{d1}(t_1) - V_d \\ \dot{u}_{d1}(t_1) \\ \ddot{u}_{d1}(t_1) \\ \dddot{u}_{d1}(t_1) \end{bmatrix} \tag{5}$$

where $u_{d1}(t_1)$ and its derivatives $\dot{u}_{d1}(t_1)$, $\ddot{u}_{d1}(t_1)$, and $\dddot{u}_{d1}(t_1)$ are the steady-state initial conditions. These initial conditions can be obtained by an iterative process like Newton–Raphson method.

Similarly, u_a, the voltage across C_a, is governed by

$$\alpha \frac{d^4 u_a(t)}{dt^4} + \beta \frac{d^2 u_a(t)}{dt^2} + u_a(t) = (1 - k_a) V_d. \tag{6}$$

Its solution has a form similar to (2).

A resonant current through C_a, L_a, T_a, and Q_2 starts to build up and discharges C_{snb}, and it is determined by

$$i_a(t) = C_a \frac{du_a(t)}{dt}. \tag{7}$$

This current carries half of the discharged energy over to C_a and L_a, and feeding the rest back to the input dc line via T_a and D_{a1}.

As $C_{\rm snb}$ discharges, u_{d1} starts to decrease and L_m starts to see a positive voltage as soon as u_{d1} becomes lower than V_d. The core of the power transformer starts magnetizing, and the magnetizing current starts to rise as governed by

$$\frac{di_m(t)}{dt} = \frac{V_d - u_{d1}(t)}{L_m}. \tag{8}$$

Seen from the secondary side, the positive voltage forward biases D_{o1}, and the secondary current is determined by

$$\frac{di_s(t)}{dt} = \frac{V_d - V_{d1}(t)}{kL_s}. \tag{9}$$

It is seen from (9) that L_s only allows the secondary current to rise slowly. This secondary current is reflected back into the primary side and it intends to charge $C_{\rm snb}$. The value of L_s shall be so selected that this reflected current is lower than the auxiliary current. Thus, $C_{\rm snb}$ can be discharged completely by the end of this interval.

B. Interval 2 ($t_2 \le t < t_3$)

At the beginning of this interval $C_{\rm snb}$ is discharged completely. Fig. 3(b) shows the equivalent circuit of this interval.

Forced by L_a, the resonant current i_a must continue in the same direction. It is found that the resonant current is now governed by

$$i_a(t) = -[u_a(t_2) + k_a V_d] \times \sqrt{\frac{C_a}{L_a}} \sin \omega_3 (t - t_2) + i_a(t_2) \cos \omega_3 (t - t_2) \tag{10}$$

where $\omega_3 = 1/\sqrt{L_a C_a}$.

As i_a flows, the body diode of Q_1 starts to conduct and this clamps the drain voltage of Q_1 at zero, hence, Q_1 can be turned on under ZVS condition at any time during this interval.

On the other hand, i_a feeds some energy that was stored in L_a and C_a back to the input dc line via T_a and D_{a1}.

During this interval, it is found that

$$u_a(t) = [u_a(t_2) + k_a V_d] \cos \omega_3 (t - t_2) + i_a(t_2) \times \sqrt{\frac{L_a}{C_a}} \sin \omega_3 (t - t_2) - k_a V_a. \tag{11}$$

Now, as u_{d1} is zero, L_m sees a constant voltage V_d, and the magnetizing current start rising linearly, and so does the secondary current i_s.

C. Interval 3 ($t_3 \le t < t_4$)

At the beginning of this interval i_a reaches zero and it starts to reverse its direction. Fig. 3(c) shows the equivalent circuit of this interval.

It is found that

$$u_a(t) = [u_a(t_2) - k_a V_d] \cos \omega_3 (t - t_3) + k_a V_a \tag{12}$$

$$i_a(t) = -[u_a(t_2) - k_a V_d] \sqrt{\frac{C_a}{L_a}} \sin \omega_3 (t - t_3). \tag{13}$$

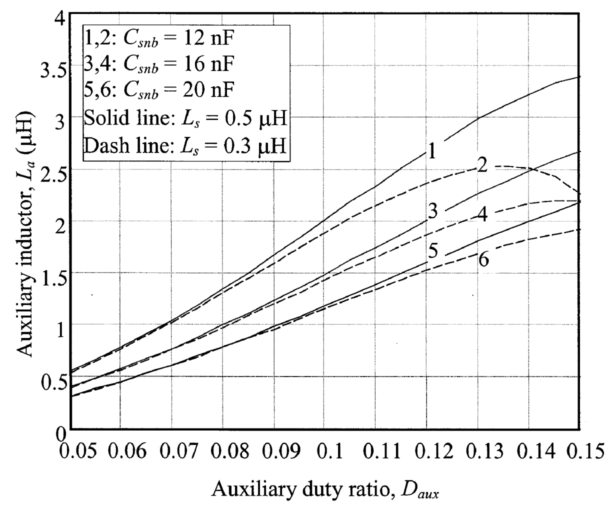


Fig. 4. Example of design curves for selecting L_a, as a function of $C_{\rm snb}$, L_s, and $D_{\rm aux}$. In this example, $V_{d\,\max} = 60$ V, $f_s = 200$ kHz, and $D_{\min} = 0.2$.

The reversed i_a discharges C_a. Through T_a and D_2 i_a feeds the energy stored in C_a during the first two intervals back to the input dc line. This fulfills the total recovery of the discharged energy from $C_{\rm snb}$.

As i_a is reversed, Q_2 sees a negative drain current. Therefore, Q_2 can be turned off under ZVS at or shortly after $t = t_3$, as its body diode can give a path to i_a and this clamps Q_2's drain voltage at zero.

The magnetizing inductor L_m continues to see a constant voltage. Then, the magnetic current is increasing linearly, and so is the secondary current i_s.

D. Interval 4 ($t_4 \le t < t_5$)

At the beginning of this interval the secondary current i_s reaches the value of the current in L_o, that is,

$$i_s(t) = \frac{P_o}{V_o}. \tag{14}$$

The current through D_{o2} decreases to zero and D_{o2} becomes reverse biased. From now on, the power circuit transfers the power from the input to the load in the same way as in a conventional forward converter. Fig. 3(d) shows the equivalent circuit of this interval.

During this interval, i_a continues until it decays to zero. Because Q_2 is already off, this resonant current stops flowing. The magnetic current is increasing linearly as it still sees a constant voltage.

E. Interval 5 ($t_5 \le t < t_6$)

At the beginning of this interval the control circuit determines that the duty ratio of Q_1 is completed to regulate the output voltage and Q_1 is turned off. $C_{\rm snb}$ slows down the rate of rise of u_{d1} and this helps to achieve a nearly ZVS turn-off of Q_1. Fig. 3(e) shows the equivalent circuit of this interval.

u_{d1} now starts to rise as determined by

$$u_{d1}(t) = V_d - V_d \cos \omega_4 (t - t_5) + \frac{P_o}{kV_o} \sqrt{\frac{L_e}{C_{\rm snb}}} \sin \omega_4 (t - t_5) \tag{15}$$

where $\omega_4 = 1/\sqrt{L_e C_{\rm snb}}$.

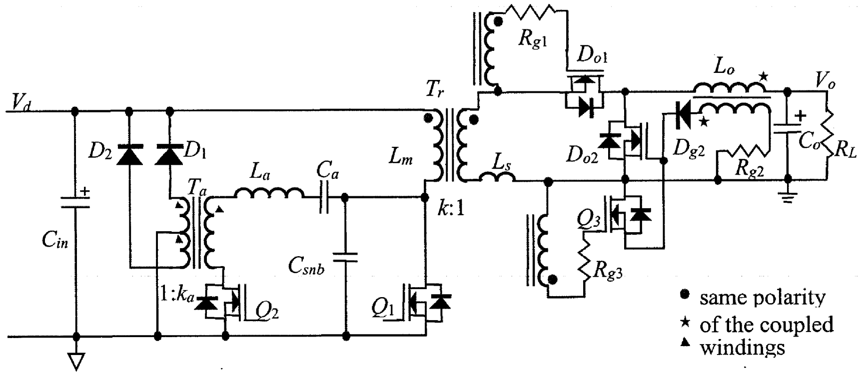


Fig. 5. Prototype converter employing synchronous rectifiers.

When u_{d1} rises above the value of V_d. L_m starts to see a negative voltage. Thus, the magnetizing current starts to decrease as seen from (8) and this sets off the demagnetizing process. The negative voltage is coupled to the secondary side of T_r and i_s also starts to decrease. Because the current in L_o is almost constant, D_{o2} is forced to conduct. Both D_{o1} and D_{o2} now conduct simultaneously and this puts L_s directly across the secondary transformer winding. Therefore, i_s is now governed by

$$i_s(t) = -V_d\sqrt{\frac{C_{\text{snb}}}{L_s}}\sin\omega_4(t-t_5) + \frac{P_o}{V_o}\cos\omega_4(t-t_5). \quad (16)$$

F. Interval 6 ($t_6 \leq t < t_1 + T_s$)

At the beginning of this interval i_s reaches zero and u_{d1} reaches the peak value, or $u_{d1}(t_5)$. Blocked by D_{o1}, i_s cannot continue. Thus, only L_m and C_{snb} now undergo a new resonance. As L_m still sees a negative voltage, the magnetizing current continues to decrease. Fig. 3(f) shows the equivalent circuit of this interval.

It is found that

$$u_{d1}(t) = V_d - [u_{d1}(t_5) - V_d]\cos\omega_5(t-t_5) + i_m(t_5)\sqrt{\frac{L_m}{C_{\text{snb}}}}\sin\omega_5(t-t_5) \quad (17)$$

where $\omega_5 = 1/\sqrt{L_m C_{\text{snb}}}$.

As seen from (8), the demagnetizing of the power transformer core continues as long as u_{d1} is higher than V_d. Since the resonance of L_m and C_{snb} in this interval has comparatively a much slower frequency due to the large value of L_m, the rate of change of u_{d1} during this interval is low. This keeps u_{d1} staying above V_d for a considerable duration of time such that the volt-second product of the demagnetizing process is able to balance that of the magnetizing process in the previous intervals of this switching cycle, and this guarantees the resetting of the power transformer.

During this interval, D_{o2} is in freewheeling of the total current in L_o. At the end of this interval this switching cycle is completed and another cycle starts to repeat the above intervals.

IV. Design Procedure

From the above analysis, it is shown that the magnetizing current behaves in almost the same way as it does in [20], although the auxiliary circuit herein is a different one. Thus, how to achieve optimal operating point of flux of the power transformer will not be repeated in this paper. Neither is the design for the power circuit addressed herein, as it is a conventional forward circuit that has been extensively discussed in the literature.

The design of the auxiliary circuit is given below for generic applications. The following parameters are assumed known: 1) $V_{d\,\text{min}}$ and $V_{d\,\text{max}}$ the minimal and maximal input voltage,; 2) D_{max} and D_{min} the maximum and minimum duty ratio of Q_1; 3) f_s the switching frequency; 4) L_m the magnetizing inductance of T_r; 5) k the turns ratio of T_r; 6) V_o, the nominal output voltage; and 7) P_o the rated output power.

TABLE I
PRINCIPAL COMPONENTS AND PARAMETERS OF THE PROTOTYPE CIRCUIT

parameter	value/selection	parameter	value/selection
$V_{d\,\text{min}}$, $V_{in\text{—max}}$	35, 75V	L_o/C_o	12 μH / 400μF
P_o	100W (V_o=5V,I_o=20A)	Q_1	IRF640*
$D_{\text{min}}/D_{\text{max}}$	0.2 / 0.40	D_{o1}/D_{o2}	MTP75N05*
f_s	200kHz	Q_3	IRF510
L_m	490μH	k_a	1:7
k	3:1	L_s	0.3μH
D_{aux}	0.1	Q_2	IRF634
C_{snb}	16nF	D_1, D_2	HFA08TB
L_a/C_a	1.5μH/66nF	Controller	UC3855AN

* Two in parallel.

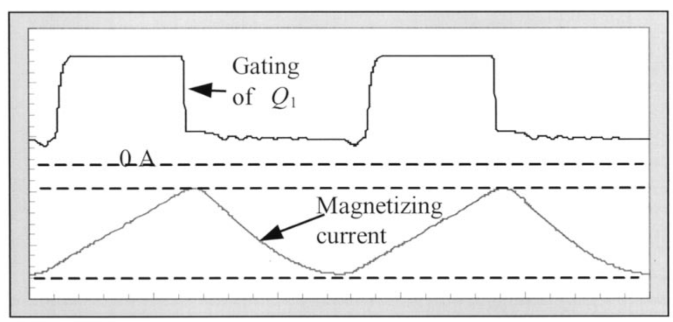


Fig. 6. Simulation results of the magnetizing current of the power transformer. Conditions: $V_d = 50$ V, $f_s = 200$ kHz, and $P_o = 90$ W. Vertical scales:10 V/div for gating signal, 0.5 A/div for magnetizing current. Timing: 2 μs/div.

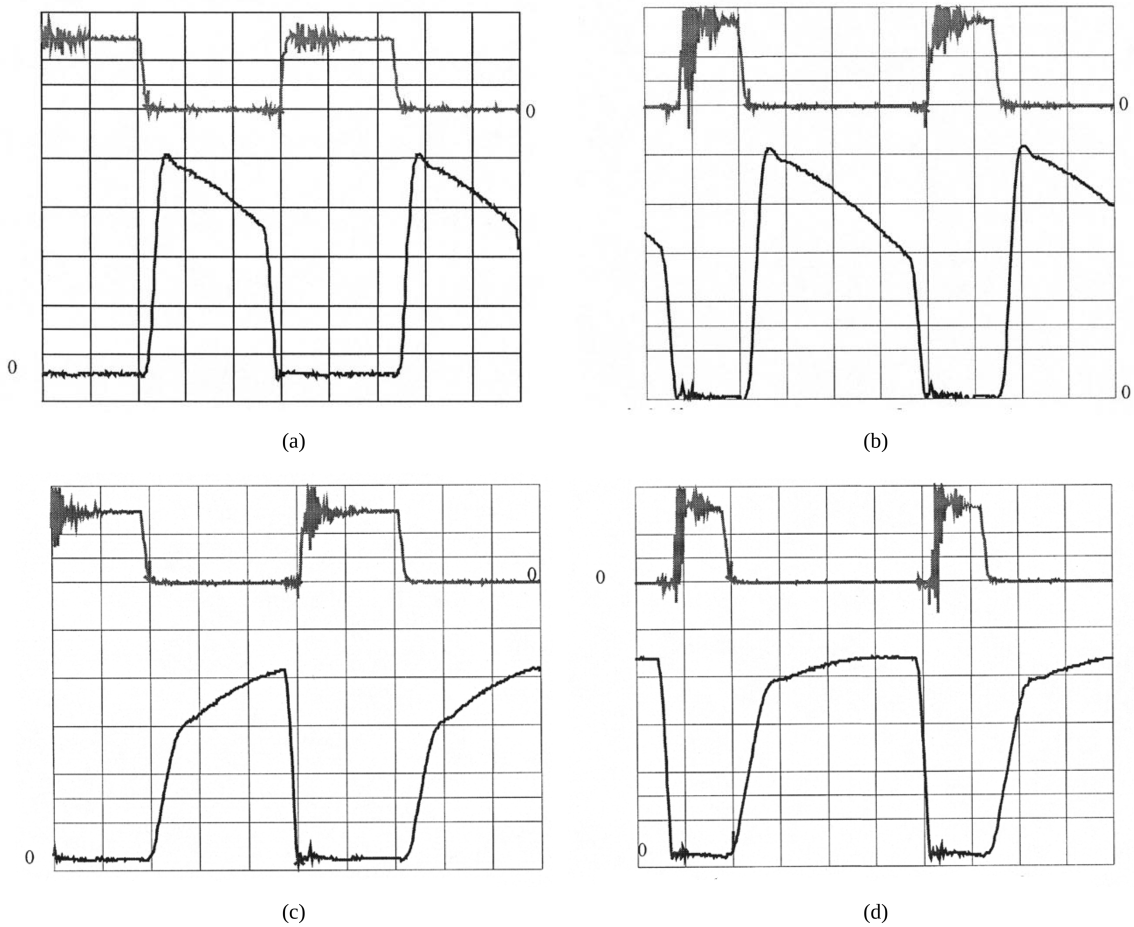


Fig. 7. Experimental waveforms of the main switch. (a) Low line full load ($V_d = 35$ V, $P_o = 90$ W). (b) High line full load ($V_d = 55$ V, $P_o = 90$ W). (c) Low line light load ($V_d = 35$ V, $P_o = 30$ W). (d) High line light load ($V_d = 55$ V, $P_o = 30$ W). Top traces: gating. Bottom traces: drain voltage. Switching frequency: $f_s = 200$ kHz. Scales—vertical: 5 V/div for gating signal, 20 V/div for drain voltage; horizontal: 1 μs/div.

A. Selection of D_{aux}

To overcome the drawbacks of the ARF, the auxiliary switch in the proposed topology is switched with a fixed duty ratio. The auxiliary switch duty ratio has influence on the voltage stress of the main switch. It is because the resetting of the power transformer core requires balanced volt-second product of the magnetizing and demagnetizing process. Since the auxiliary duty ratio steals some time, it reduces the time allowed for demagnetizing, then the main switch will suffer from a higher voltage stress.

It is found that the maximum voltage stress V_{peak} is approximately determined by

$$V_{peak} = \left(1 + \frac{\pi}{2} \cdot \frac{D_{\min}}{1 - D_{\min} - D_{\mathrm{aux}}}\right) V_{d\max}. \tag{18}$$

To limit the maximum voltage stress to 150% of the maximum input voltage, D_{aux} shall be limited by

$$D_{\mathrm{aux}} \leq 1 - (1 + \pi) D_{\min}. \tag{19}$$

On the other hand, the discharging of C_{snb} shall be completed within the auxiliary duty time; D_{aux} shall not be too small to avoid large discharging current. It is reasonable to select the minimum D_{aux} above 50% of the limit of (19), i.e.,

$$D_{\mathrm{aux}} \geq \frac{1 - (1 + \pi) D_{\min}}{2}. \tag{20}$$

B. Selection of C_{snb}

To successfully reset the power transformer without overstressing the main switch, u_{d1} shall always be kept higher than V_d throughout Interval 6. This means the resonance of Interval 6 shall be longer than one-quarter of its resonance cycle. Therefore, the minimum C_{snb} shall be limited by

$$C_{\mathrm{snb}} \geq \frac{4(1 - D_{\mathrm{aux}} - D_{\min})^2}{\pi^2 f_s^2 L_m}. \tag{21}$$

In addition, C_{snb} must be big enough to guarantee ZVS turn-off. From (15), it is seen that C_{snb} determines the rise time of the drain-to-source voltage of Q_1 at turn-off. Limiting u_{d1} below V_d within the required rise time t_r, C_{snb} should be limited by

$$C_{\mathrm{snb}} \geq \frac{P_o t_r}{k V_o V_{d\min}}. \tag{22}$$

However, the rise time should not exceed the gap left by $2D_{\max}$ and D_{aux} in one cycle. Otherwise the resetting time would be reduced and the voltage stress on the power transformer would be increased. This limits the maximum value of C_{snb} by

$$C_{\mathrm{snb}} \leq \frac{P_o}{2k V_o V_{d\min}} (1 - 2D_{\max} - D_{\mathrm{aux}}). \tag{23}$$

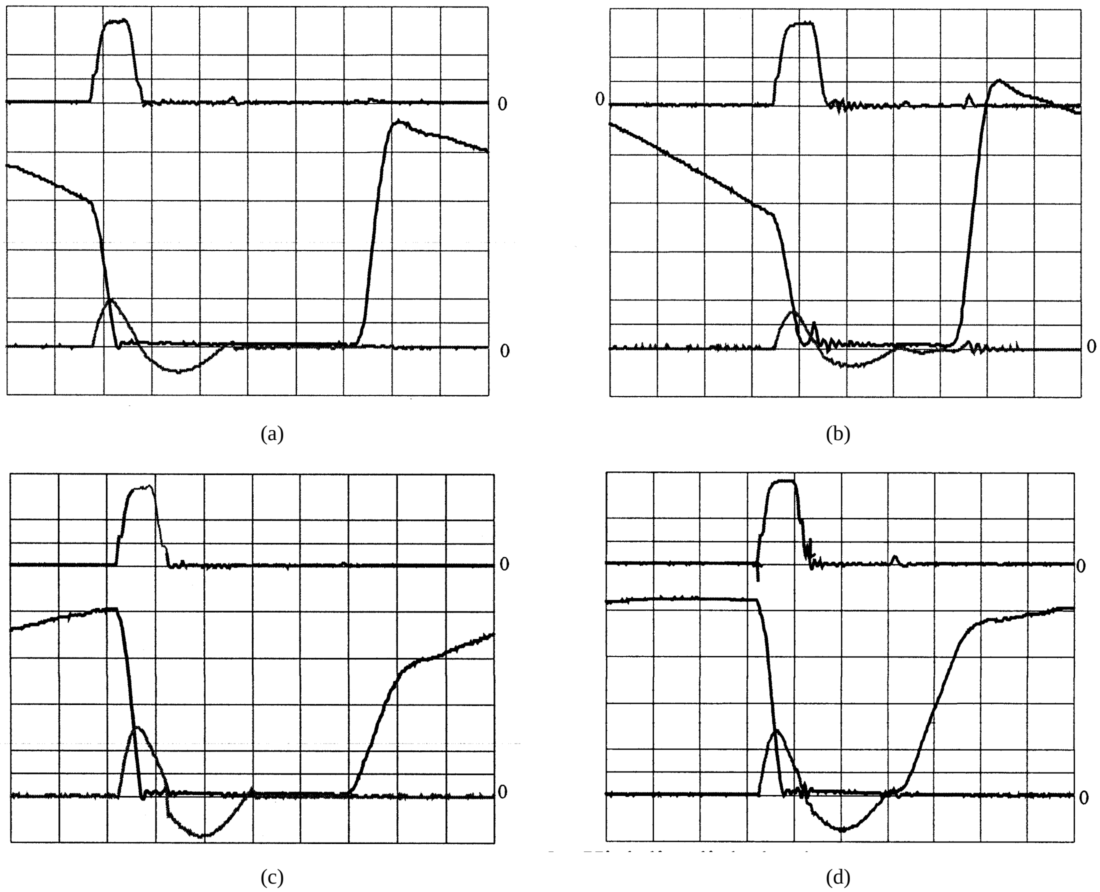


Fig. 8. Experimental waveforms of the auxiliary switch. (a) Low line full load ($V_d = 35$ V, $P_o = 90$ W). (b) High line full load ($V_d = 55$ V, $P_o = 90$ W). (c) Low line light load ($V_d = 35$ V, $P_o = 30$ W). (d) High line light load ($V_d = 55$ V, $P_o = 30$ W). Switching frequency: $f_s = 200$ kHz. Top traces: gating. Middle traces: drain voltage. Bottom traces: drain current. Scales—vertical: 5 V/div for gating signal, 20 V/div for drain voltage, 5 A/div for drain current; horizontal: 0.5 μs/div.

C. Selection of L_s

L_s has two functions: 1) to limit the rise of the secondary current in Intervals 1 and 2 in order to achieve ZVS of Q_1 and 2) to charge $C_{\rm snb}$ and pull u_{d1} up to an enough magnitude to achieve resetting of the power transformer as seen from (15).

To achieve ZVS, the current through L_s shall not exceed the auxiliary current throughout Intervals 1 and 2, otherwise, $C_{\rm snb}$ will not be completely discharged. This requires that

$$L_s \geq \frac{V_{d\,\max} D_{\rm aux}}{k f_s I_{\rm apeak}} \tag{24}$$

where $I_{\rm apeak}$ is the peak current through the auxiliary circuit. $I_{\rm apeak}$, to be determined below, shall be lower than the primary full load current to reduce conduction losses in the auxiliary circuit.

However, the large value of L_s may pull u_{d1} up to an excessive level and, thus, drive the power transformer into saturation due to excessive dc bias current [20]. Assume $I_{\max}$ is the magnetizing current corresponding to allowable flux density $B_{\max}$ in the core beyond which the core will be saturated. Then, L_s shall be limited by

$$L_s \leq \frac{C_{\rm snb} V_{d\max}^2 + L_m I_{\max}^2 - L_m (I_{\max} - \Delta I_m)^2}{I_o^2} \tag{25}$$

where ΔI_m is the swinging range of the magnetizing current.

In addition, L_s reduces the effective duty ratio by Interval 3, as seen in (9) and (14), L_s should also be limited by

$$L_s \leq \frac{V_{d\,\min} V_o}{k f_s P_o} \Delta_d \tag{26}$$

where Δ_d is the allowable reduction of the effective duty ratio. Usually, this reduction should be less than 0.1.

D. Selection of L_a and C_a

To guarantee a strong resonant current such that it is able to discharge $C_{\rm snb}$ in Interval 1, C_a shall be large enough and $u_a(t_1)$ which is the voltage across C_a at the beginning of Interval 1 shall be very low. Let C_{oss} be the internal drain-to-source capacitor of Q_2, and note that C_{oss} and C_a are in series to share u_{d1}. Assuming the residual voltage across C_a, or $u_a(t_1)$, is less than 1% of $u_{d1}(t_1)$, the C_a shall be limited by the following equation:

$$C_a > 100 C_{oss}. \tag{27}$$

However, C_a shall not be too large to limit the size and cost of the part.

The reversed i_a in the auxiliary circuit during Intervals 3 and 4 should complete its negative half cycle of resonance. Hence, as seen in (13), the following equation should be satisfied:

$$L_a \leq \frac{D_{\min}^2}{\pi^2 f_s^2 C_a}. \tag{28}$$

On the other hand, as seen from (7) and (10), L_a should be selected of a large value in order to reduce the magnitude of the resonant current and hence the conduction losses in the auxiliary circuit.

In order to achieve ZVS in Q_1, u_{d1} must reach zero in Interval 1. By letting (2) be zero, the value of L_a can be found by numerical method. It is seen from (1)–(5) that the value of L_a is dependent on C_{snb}, L_s, and D_{aux}. Fig. 4 shows an example of the design curves to select L_a.

E. Selection of T_a

The turns ratio k_a of T_a should be small to limit the reflected voltage of V_d seen by the discharging current i_a. Otherwise, this voltage, which tends to stop i_a in Interval 1, would become significant, C_{snb} could not be completely discharged, and ZVS would be lost in Q_1.

F. Selection of Q_2

A switch with low on-resistance and low inherent capacitance should be selected for Q_2. The voltage rating of Q_2 should be the same as Q_1. The current rating is determined by (10).

G. Selection of D_{a1} and D_{a2}

D_{a1} and D_{a2} should be fast-recovery diodes. Their voltage rating should be higher than $2V_{d\max}$, and their current rating should be higher than $\frac{1}{2}f_s C_{\text{snb}} V_{d\max}$.

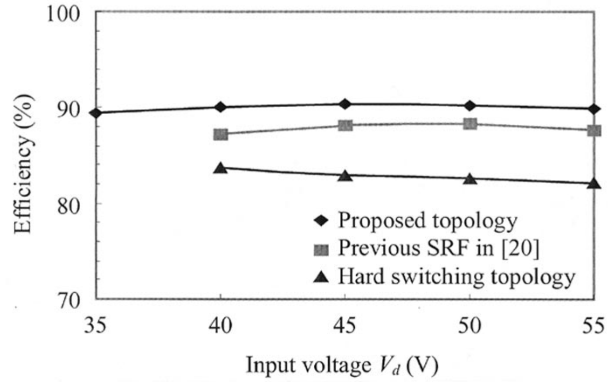
V. Experimental and Simulation Results

A prototype of a 5-V 100-W circuit operated at 200 kHz has been built. The circuit is shown in Fig. 5 and the circuit parameters are shown in Table I. It employs self-driven synchronous rectifiers reported in [21]. The gate drives for synchronous rectifier D_{o1} are generated by a winding coupled to T_r, and for D_{o2} by a winding coupled to L_o. Q_3 helps to quickly turn off D_{o2}. D_{g2} blocks the excessive negative gate voltage when D_{o2} is off to protect D_{o2}.

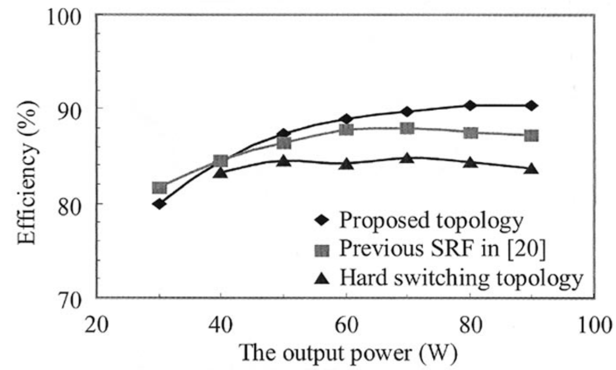
The averaged current-mode control is used as the control scheme for the prototype converter. A Unitrode controller UC3855 is employed to implement the control. This controller produces two gate drives, one of which is the modulated pulsewidth drive for the main switch, and the other is the fixed pulsewidth drive for the auxiliary circuit. Other controllers can also be used, however, a small circuit must be added to generate the required auxiliary gate drive.

Fig. 6 shows typical simulation results of the magnetizing current. The magnetizing current returns to the same point after each cycle, i.e., T_r achieves self-reset.

Fig. 7 shows the experimental results of key waveforms of the main switch Q_1 under different operating conditions. Because at turn-on the gating signal comes after the drain voltage has already dropped to zero, and at turn-off it withdraws completely before the drain voltage starts to rise, ZVS is always achieved in Q_1 under all these conditions.



(a)



(b)

Fig. 9. Overall efficiency of the proposed converter topology. (a) Efficiency versus input voltage at full load (90 W). (b) Efficiency versus output power under fixed input voltage (45 V).

Fig. 8 shows the experimental waveforms of the auxiliary switch Q_2 under different operating conditions. It is seen clearly that ZCS turn-on and ZVS turn-off are always achieved in Q_2 under all these conditions.

Fig. 9 shows the experimental results of the overall efficiency under different operating conditions. In Fig. 9(a), it is shown that the proposed topology has about 90% efficiency over entire input voltage range. The efficiency drops slightly at both ends of the range. Above all, the proposed topology has about 2%–3% better efficiency at full load than the previously published ZVS forward topology in [20].

VI. Conclusions

The proposed forward converter topology employs a small resonant auxiliary circuit and a simplified power transformer, and it achieves soft switching in both the main and auxiliary switches and fulfills power transformer self-reset without the use of the conventional reset winding. Therefore, high-power conversion efficiency at high switching frequency can be obtained at reduced costs. The breadboard prototype converter proves the concepts of this paper and has shown about 90% overall efficiency at full load. It can be concluded that the proposed topology is a promising solution to low output voltage high output current and power level up to 250 W applications in advanced telecom and computer systems.

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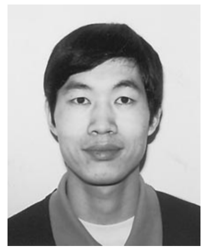

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