A 1.6 kW, 110kHz DC-DC Converter

Optimized for IGBTs

Keming Chen
REM Technologies
29 Vatrano Road
Albany, NY 12205

Thomas A. Stuart
Electrical Engineering Dept.
University of Toledo
Toledo, OH 43606

ABSTRACT

A full bridge DC-DC converter using a zero-current and zero-voltage switching technique is described. This circuit utilizes the characteristics of the IGBT to achieve power and frequency combinations that are much higher than previously reported for this device. Experimental results are included for a 1.6kW, 110kHz converter with 95% efficiency.

INTRODUCTION

Although IGBTs are finding increasing acceptance in higher voltage and power applications, they exhibit a current tailing problem that usually limits the maximum operating frequency to about 20-30 kHz [1]. This current tailing characteristic results from the inability to sweep out the stored charge at turn-off [1],[2]. Some papers [3],[4] have shown the use of IGBTs in zero-current switching resonant converters in which the tailing problem is largely avoided. However, the power switch in the resonant circuit conducts a much higher current pulse. Consequently, a larger conduction loss exists than in its PWM counterpart. Furthermore, zero-current switching resonant converters do not eliminate the current tailing problem since the stored charge cannot be removed.

Fig. 1 shows a DC-DC converter that reduces the effects of this tailing problem by employing zero-current switching on one leg of the bridge and zero-voltage switching on the other. Perhaps the most unusual feature of the circuit in Fig. 1 is the absence of the diodes normally connected in reverse parallel with Q1-4. As will be explained later, the omission of these diodes means that the IGBTs in one leg of the bridge will be subjected to reverse voltage avalanche, but this avalanche provides zero-current switching for the other leg. The reverse avalanche characteristics of the IGBT are now specified by at least one manufacturer [5], and the avalanche loss is offset by the reduced turn-off losses.

THEORY OF OPERATION

The gate drive timing is shown in Fig. 1,while Q3 and Q4 waveforms are shown in Figs. 8 and 9, respectively. The control scheme in Fig. 1 is almost the same as conventional phase-shift control [6] except that the Q2-Q4 deadtime varies inversely with the duty ratio as shown in dashed lines. This provides more delay time between Q2 and Q4 for high line operation and light load conditions. On each half cycle Q1 and Q4 will turn on at almost the same time, but Q4 will turn off first. Thus Q2 and Q4 form the leading leg, and Q1 and Q3 form the trailing leg.

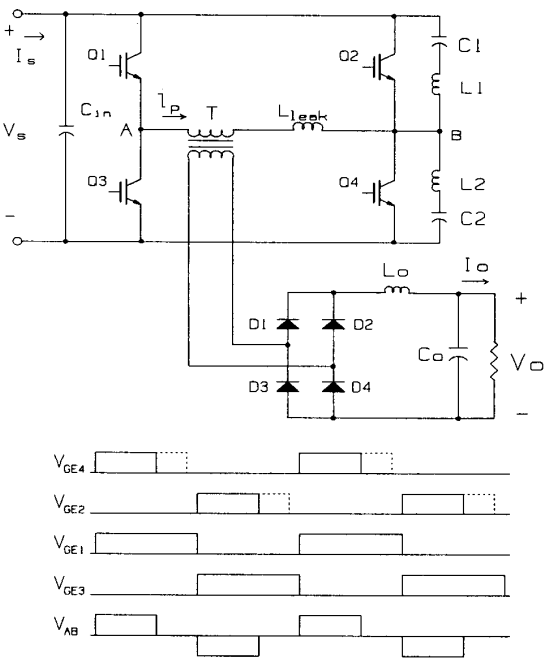

Fig. 1 Zero current and zero voltage switching converter and timing diagram

0-7803-0090-4/91/0700-0139$01.00 ©1991IEEE

Assuming Q1 and Q4 are conducting current initially, C1 and C2 provide zero-voltage switching when Q4 turns off. The primary current splits between capacitances C1 and C2, charging C2 and discharging C1 (the function of L1 and L2 will be explained later, but they are very small and have only a minor effect on zero voltage switching). Tailing still occurs with Q4, but zero-voltage switching greatly reduces the associated turn-off losses. L_{leak} will cause the voltage on C2 to continue to increase until Q2 is forced into reverse avalanche at about 30 volts. Q2 then acts like a zener until the $\frac{1}{2} i_p^2 L_{leak}$ energy is dissipated and i_p is driven to zero. Since the voltage at point B is still higher than the input voltage by an amount equal to the IGBT reverse avalanche voltage, a small current will flow back to the input through Q1. This will help to remove the storage charge in Q1, and therefore the turn-off current tailing of Q1 is virtually eliminated. Q1 can then be turned off at zero current. Because of the voltage on C2, Q2 is turned on at effectively zero voltage with very low turn-on loss. Finally, when Q1 is completely turned off, Q3 turns on, and the next half cycle of operation begins.

ANALYSIS OF SWITCHING TRANSITIONS

The analysis presented in this section is based on the assumptions that switches, diodes and transformer are ideal and inductors and capacitors are lossless. The new converter has been identified as a zero current and zero voltage transient resonant converter. The resonant operation takes place during the switching transient, which is only a fraction of the total operating period. However, the analyses of these switching transitions are important for determining the soft switching conditions.

Fig. 2 shows the switching waveforms for the turn-off transition of the leading leg. $V_{C2}(t)$ is the voltage across C2 (the leg voltage). The primary current $i_p(t)$, the collector current $i_{Q2}(t)$ in Q2 and the capacitor current $i_{C2}(t)$ in C2 are also presented. The switching transition starts with the Q4 turn off at t_0. Four modes can be identified as shown in Fig. 2. The equivalent circuit for mode 1 is shown in Fig. 3. We assume that the current in the output filter inductance is continuous, and the equivalent circuit of Fig. 3 is valid only if this assumption holds. I_{p1} is the initial value of the primary current, V_o' is the output voltage reflected to the primary side, and L_o' is the reflected output filter inductance. If no air gap is used, the magnetizing inductance is much bigger than the reflected output filter inductance L_o'. Usually, the air gap is needed for two reasons. The zero voltage transient resonant converter in [7] uses the air gap to provide a large magnetizing current so that zero-voltage switching can be maintained at light load. An air gap is also occasionally used to avoid saturation caused by a slight dc flux component in the transformer. However,

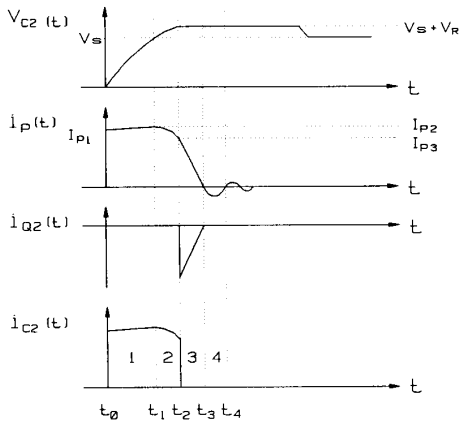

Fig. 2 Waveforms for the turn off transition

for the new zero-current and zero-voltage switching converter, current mode control is used to balance the current and avoid transformer saturation. As will be discussed later, the air gap is also not necessary for the zero-current or zero-voltage switching of the new converter. Therefore, the magnetizing inductance is neglected. A simple calculation results in the following time function for $V_{C2}(t)$: $(t_0 < t < t_1)$

$$V_{c2}(t) = V_s(1-\cos\omega_1 t) - V_o'(1-\cos\omega_1 t) + \frac{I_{p1}}{\omega_1(C_1+C_2)}\sin\omega_1 t \quad (1)$$

where

$$\omega_1 = \frac{1}{\sqrt{(L_{leak}+L_o')(C_1+C_2)}} \quad (2)$$

In practice, the primary current is almost constant during the switching transition of mode 1. This is due to the fact that L_o' is

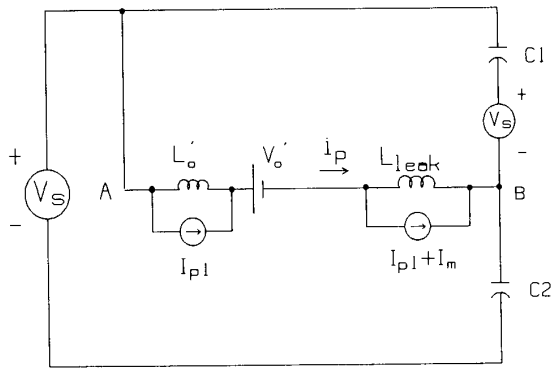

Fig. 3 Equivalent circuit for the turn off transition mode 1

relatively very large. Therefore the transition can be approximated as a linear function of time:

$$V_{c2}(t) \approx \frac{I_{p1}}{C_1 + C_2} t \tag{3}$$

The transition mode 1 ends at t_1, when $V_{c2}(t) = V_s$. Assuming that t_0 starts at zero,

$$t_c = t_1 = V_s \frac{C_1 + C_2}{I_{p1}} \tag{4}$$

It is clear that t_c is the time required for the voltage at point B to reach the high voltage rail. In order to achieve a soft switching transition, the gate drive delay time between Q2 and Q4 has to be greater than t_c.

Fig. 4 shows the equivalent circuit for mode 2 of the turn off transition. Mode 2 starts at time t_1 when the voltage at point B is equal to V_s. The equivalent circuit is simpler than that for the mode 1, because the transformer is shorted out by the output rectifier diodes. I_{p2} is the peak value of the primary current as shown in Fig. 2. We can derive the time function for the primary current and capacitor voltage for transition mode 2: ($t_1 < t < t_2$)

$$i_p(t) = I_{p2} \cos \omega_2 t \tag{5}$$

$$V_{c2}(t) = V_s + \frac{I_{p2}}{\omega_2 (C_1 + C_2)} \sin \omega_2 t \tag{6}$$

where

$$\omega_2 = \frac{1}{\sqrt{L_{leak} (C_1 + C_2)}} \tag{7}$$

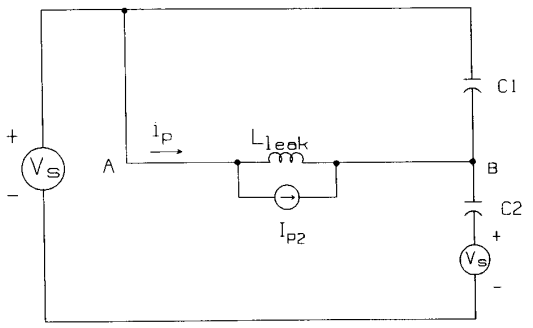

Fig. 4 Equivalent circuit for the turn off transition mode 2

As shown in Fig. 2, the transition mode 2 ends at t_2 when the capacitor voltage is clamped by the reverse avalanche of Q2. V_R is the value of the reverse avalanche voltage. The duration of the transition mode 2 (t_2 - t_1) can be calculated by letting Eq. (6) equal to $V_s + V_R$. Hence:

$$t_{z1} = t_2 - t_1 = \frac{1}{\omega_2} \arcsin \frac{\omega_2 (C_1 + C_2) V_R}{I_{p2}} \tag{8}$$

By substituting Eq. (8) into Eq. (5) the final value of the primary current I_{p3} can be derived as follows:(if $I_{p3} > 0$)

$$I_{p3} = I_{p2} \cos \omega_2 t_{z1} \tag{9}$$

since

$$\sin \omega_2 t_{z1} = \frac{\omega_2 (C_1 + C_2) V_R}{I_{p2}} \tag{10}$$

then

$$I_{p3} = \sqrt{I_{p2}^2 - V_R^2 \frac{C_1 + C_2}{L_{leak}}} \tag{11}$$

If the primary current has reached zero during mode 2, the transition mode 3 will no longer exist. Otherwise, Q2 will be forced into the reverse avalanche mode, as indicated, and we proceed to mode 3. In this mode, Q2 acts like a zener until the rest of the stored energy is dissipated, and the primary current is driven to zero. It is obvious from Eq. (11) that this energy loss can be reduced or avoided altogether if a higher V_R is used. Usually, the leakage inductance is always minimized, and the size of the capacitor is limited by other constraints such as the Q2-Q4 dead-time.

The equivalent circuit for the transition mode 3 is shown in Fig. 5. It is simply an inductor in series with a voltage source. The primary current is a linear function of time, so we have for the transition mode 3: ($t_2 < t < t_3$)

$$i_p(t) = I_{p3} - \frac{V_R}{L_{leak}} t \tag{12}$$

Transition mode 3 ends at t_3, when the primary current reduces to zero.

$$t_{z2} = t_3 - t_2 = \frac{L_{leak}}{V_R} \sqrt{I_{p2}^2 - V_R^2 \frac{C_1 + C_2}{L_{leak}}} \tag{13}$$

The total time required for driving the primary current to zero is

$$t_z = t_{z1} + t_{z2} \tag{14}$$

Once the primary current is reduced to zero, it will change its polarity and flow back to the input source through Q1. This is

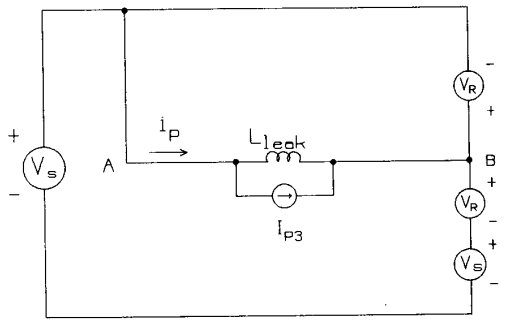

Fig. 5 Equivalent circuit for the turn off transition mode 3

because when mode 3 ends at t_3, the voltage at point B is higher than the input voltage by an amount V_R. Due to the storage charge in Q1, the same amount of reverse avalanche voltage for Q1 cannot be established until all the stored charge is removed. The storage charge of Q1 can be modeled as a non-linear capacitor Cs in parallel with Q1. This results in the turn off transition mode 4. Notice that the energy used to remove the storage charge comes from C1 and C2. Due to the fact that C1 and C2 are much bigger than Cs, they are then modeled as voltage sources. Fig. 6 shows the equivalent circuit for the turn off transition mode 4. It will end at the turn off of Q1 or if the primary current decays to zero before Q1 is turned off, it will end then. The primary current during mode 4 can be derived as follows: ($t > t_3$)

$$i_p(t) = \frac{V_R}{\omega_4 L_{leak}} \sin \omega_4 t \tag{15}$$

where

$$\omega_4 = \frac{1}{\sqrt{L_{leak} C_s}} \tag{16}$$

The time required for removing the storage charge in Q1 is then:

$$t_q = t_4 - t_3 = \pi \sqrt{L_{leak} C_s} \tag{17}$$

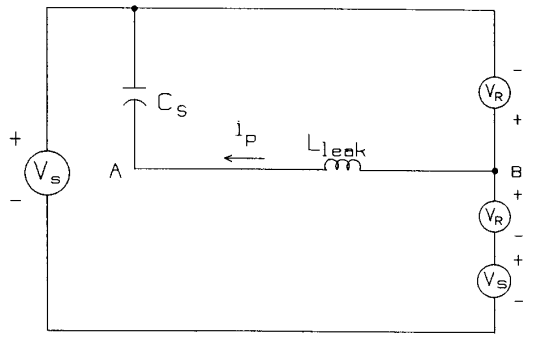

Fig. 6 Equivalent circuit for the turn off transition mode 4

Zero-current switching is achieved if the gate drive is removed from Q1 any time after t_4. Since the trailing leg is turned off at zero current, it will not cause any switching transition as long as the zero-current switching condition is maintained. There will be a switching transition if the trailing leg is not turned off at zero current, but this will only happen at very light load.

The turn on transition is much simpler than the turn off. For the leading leg, the IGBT is turned on when it is still reverse biased. No switching transition will take place as long as the zero-voltage switching condition is maintained. Actually, since the voltage at point B is higher than the source voltage by an amount V_R, when Q3 is turned on it draws current from the snubber capacitors. In other words, although Q2 is already on, it will not conduct any current until the voltage at point B drops to V_s. As a result, a current ringing is induced in the leading leg due to the parasitic inductance of the snubber capacitors.

This oscillation may affect the operation of the circuit if it is not controlled within a certain limit. Obviously, the oscillation can be eliminated if the snubber capacitors have no or very small parasitic inductance. In practice, even if a capacitor with no parasitic inductance is available, the parasitic inductance in the wires can still cause a notable oscillation. Capacitors with low parasitic inductance are also very expensive.

An alternative way to control the oscillation is to do just the opposite, and instead of trying to reduce the parasitic inductance, a small external inductor (whose inductance is relatively large compared to the parasitic inductance) is put in series with each snubber capacitor. It is found that the additional inductor does not have a significant affect on the zero-voltage switching and offers two advantages: (a) a large inductance will limit the peak oscillation current, and (b) at light load, the additional inductor can limit the current surge when the zero-voltage switching condition is lost. We will have more discussion on this issue later.

CONDITIONS FOR SOFT SWITCHING

For the new proposed circuit, high efficiency is achieved by providing zero-voltage switching on the leading leg and zero-current switching on the trailing leg. Low switching losses must be maintained over a wide range of operating conditions. Zero-voltage switching for the leading leg is achieved by having snubber capacitors in parallel with the switches, but turn-on loss results if the switch charges a partially charged capacitor. For the trailing leg, turn-off loss will result if the current is not yet zero at turn off.

The turn-on of the opposite switch in the leading leg must be delayed by the time required for the capacitor to be fully charged. From Eq. (4), the transition time for the capacitor voltage to reach V_s is

$$t_c = V_s \frac{C_1 + C_2}{I_{p1}} \tag{18}$$

I_{p1} is peak value of the primary current, and it is a function of the input voltage and the output current. In practice, a large output filter inductance is used to keep a low current ripple. Therefore, I_{p1} can be approximated by NI_o. Where N is the turns ratio of the transformer and I_o is the output current. For soft switching, the delay time t_d must be larger than that given in Eq. (18). Notice that during the transition of the leading leg, the capacitor is driven by a current source NI_o, and its voltage always

reaches the new rail if given enough time. Therefore, soft switching for the leading leg is achieved naturally by the intrinsic circuit operation. After replacing I_{p1} with NI_o in Eq. (18), the delay time for the leading leg is

$$t_{d,\text{leading leg}} = V_s \frac{C_1 + C_2}{NI_o} \tag{19}$$

The turn-off of the switches in the trailing leg must be delayed until the current is reduced to zero and the storage charge is completely removed. Therefore, the additional delay time for the trailing leg is the sum of the transition time in modes 2, 3 and 4. If we assume that the primary current is constant during the switching transition period, we have:

$$I_{p2} = I_{p1} = NI_o$$

Then from Eqs. (8), (13) and (17), the additional delay time for the trailing leg can be represented as follows:

$$t_{d,\text{trailing leg}} = \pi\sqrt{L_{leak}C_s} + \frac{L_{leak}}{V_R}\sqrt{N^2I_o^2 - V_R^2\frac{C_1+C_2}{L_{leak}}}$$

$$+ \sqrt{L_{leak}(C_1+C_2)}\arcsin\frac{V_R}{NI_o}\sqrt{\frac{C_1+C_2}{L_{leak}}} \tag{20}$$

The total delay time between Q4 turn-off and Q1 turn-off is,

$$t_{d,\text{total}} = t_{d,\text{leading leg}} + t_{d,\text{trailing leg}} \tag{21}$$

Since $i_p = 0$ prior to removing the Q1 gate drive, no deadtime is required between Q1 and Q3. For simplicity, the Q1, Q2, and Q3 switching transitions can be simultaneous, as shown in Fig. 1.

Under light load conditions, the delay time required for the leading leg increases as the output current decreases. Since the delay time for the trailing leg is proportional to the load current, it will tend to compensate for the extra time required by the leading leg. However, it can only compensate up to the point where the second term in Eq. (20) reduces to zero. Since the delay time for the trailing leg is not a function of the input voltage, there will be no compensation for the extra time required by the leading leg as the input voltage increases.

For a converter with conventional phase shift PWM control, the worst case occurs with maximum input voltage. So the minimum delay time between Q2 and Q4 has to be greater than the minimum delay time required on the leading leg to maintain soft switching with maximum input voltage. The maximum delay time is limited by the total duty cycle available. From the above two requirements, the following bounds can be obtained for the delay time:

$$t_{d,\text{total}} < T\left(1 - \frac{V_o}{NV_{s,\min}}\right) \tag{22}$$

$$t_{d,\text{total}} > (t_{d,\text{leading leg}} + t_{d,\text{trailing leg}})\big|_{V_s=V_{s,\max}} \tag{23}$$

CONTROL STRATEGY

A new control strategy is implemented to help preserve soft switching at light loads and high input voltage. As shown in Fig. 1, the zero-voltage turn-on condition for Q2 is always maintained as long as Q1 is on long enough. In other words, there is no need to turn on Q2 right after Q4 is turned off. Now, Q2 is turned on at the time Q1 is turned off. Consequently, the delay between Q2 and Q4 varies inversely with the duty cycle. Since the output voltage V_o is regulated, as the input voltage increases, the duty cycle will decrease. The time required for charging C1 and C2 will increase because of the increase of the input voltage. However, the delay time available for Q2 and Q4 is also increased as the duty cycle is decreased. Therefore, with the new control strategy, the minimum delay time required for the leading leg to maintain soft switching occurs with minimum input voltage.

As we have seen, the new control strategy is advantageous when the duty cycle changes inversely with the delay time demanded between Q2 and Q4. This is obviously the case when input voltage changes. If we change the load and still keep the same output voltage, the primary current will change proportionally with the load current. As we have discussed earlier, the compensation provided by the trailing leg extends the operating range for soft switching, regardless the change of duty cycle. However, this compensation is very limited. As we will see in the following discussion, the new control strategy greatly extends the operating range for soft switching over a wide variation of load. Under light load conditions, as the turn off switching transient of the leading leg becomes more dominant, the steady state operation is no longer the same as the traditional PWM full bridge converter.

Fig. 7 shows the simplified equivalent circuits and related waveforms for the zero-current and zero-voltage switching converter operated under light load. For simplicity, it is assumed that (a) the switches, diodes and transformer are ideal, (b) inductors and capacitors are lossless, and (c) the output is modeled as a constant current source reflected to the input side by N. D and D' have been defined as shown in Fig. 7 (a) and (b). As shown in Fig. 7 (d), three distinct operating modes have been identified. Mode 1 is defined as the active mode represented by D. Power is transferred from input to the output during this mode. Mode 2 is the switching transition mode designated by D'. This is the distinctive mode which sets the new circuit apart from the conventional PWM circuit. During this mode, there is still a significant amount of power transferred to the output. As we will see, the most important feature of this mode is that D' is a function of the

output current. In the freewheeling portion, defined as mode 3, the voltage across transformer is zero and therefore no power is transferred to the output. The output voltage is the average voltage across the transformer during a half cycle, and it can be calculated as follows:

$$V_o' = V_s D + \frac{1}{2} V_s D' \qquad (24)$$

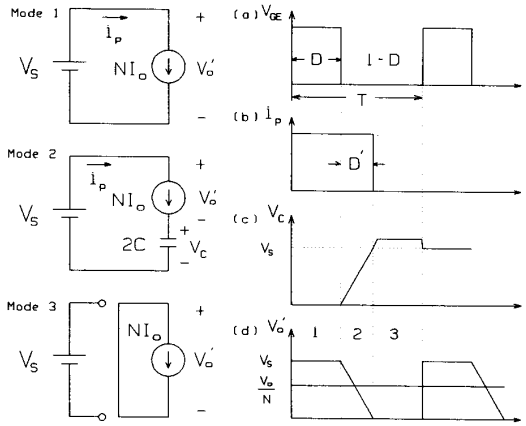

Fig. 7 Steady state equivalent circuits and waveforms
(a). Gate drive signals for the leading leg IGBTs
(b). Primary current
(c). Snubber capacitor voltage
(d). Voltage across transformer primary

From Fig. 7 (c) and the equivalent circuit for mode 2, D' is given by:

$$D' = \frac{2CV_s}{NI_oT} \qquad (25)$$

From Eqs. (24) and (25), the equation for the duty cycle in terms of input voltage and output current is derived:

$$D = \frac{V_o}{NV_s} - \frac{CV_s}{NI_oT} \qquad (26)$$

Under light load conditions, the duty cycle is an inverse function of the load current. This means that the zero-current and zero-voltage switching converter can also take advantage of the new control strategy at light load. However, at very light load or no load, the circuit will eventually have the same problem as most soft switch circuits in that C1 and C2 will not be fully charged when Q2 turns on [6]-[8]. The resulting current transient creates an additional turn-on loss for Q2, but this loss is usually not serious since it occurs when the turn-off and conduction losses are relatively low. L1 and L2 are helpful in this respect, since they limit these transients, and yet they are small enough to have only a minor effect on the zero-voltage switching.

The obvious advantage of zero-current and zero-voltage switching with the new control strategy is that it allows larger C1 and C2 values than conventional phase shift circuits with reverse parallel diodes. These larger capacitors provide a significant reduction in the turn-off losses of Q2 and Q4.

EXPERIMENTAL RESULTS

A prototype of the full bridge zero-current and zero-voltage switching DC-DC converter with the new control strategy has been implemented in the laboratory. The converter operated satisfactorily over the entire no load to full load range with an input voltage range of 260V-340V. A complete component list for the circuit shown in Fig. 1 is given in Table 1, and the converter was tested under the following conditions:

V_s = 260Vdc	I_s = 6.5Adc	P_s = 1690 W	fre = 110kHz
V_o = 126Vdc	I_o = 12.8Adc	P_o = 1613 W	eff = 95.4%

Part	Type	Part	Value
Q1,Q3	IXGH20N50	C_{in}	20uF
Q2,Q4	IXGH20N60A	C1-2	0.01uF
D1-4	MUR3020PT	C_o	140uF
T Core	EC 70		
36:25 Material	N 27	L1-2	0.22uH
CT Core	2616P	L_{leak}	1.3uH
1:120 Material	3B7	L_o	557uH

Table 1 Parts list for prototype power circuit

Voltage and current waveforms for Q3 with zero-current switching and Q4 with zero-voltage switching are shown in Figs. 8 and 9, respectively. Noteworthy observations include the fact that Q3 conducts longer than Q4 in order to charge C1 and C2. The maximum level of Vce4 is determined by the avalanche of Q2 whereas the minimum is determined by the avalanche of Q4.

The various losses for Q3 and Q4 are itemized in Table 2, and the related waveforms are shown in Figs. 11 and 12. All were obtained using a Tektronix 11401 digitizing Oscilloscope. No attempt was made to measure conduction losses in the circuit due to the lack of a convenient method of compensation for oscilloscope overdrive errors [9], but the estimated saturation voltage is

Losses (W)	Q3	Q4
Conduction loss	4.7	3.4
Turn on loss	1.6	0.7
Turn off loss	4.6	4.8
Avalanche loss	---	3.3
Total loss	10.9	12.2

Table 2 Various losses for Q3 and Q4

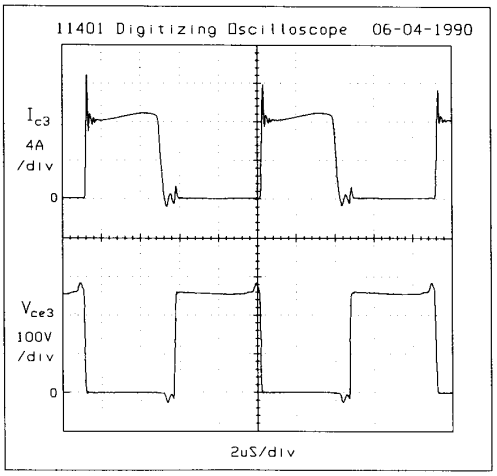

Fig. 8 Voltage and current waveforms for Q3

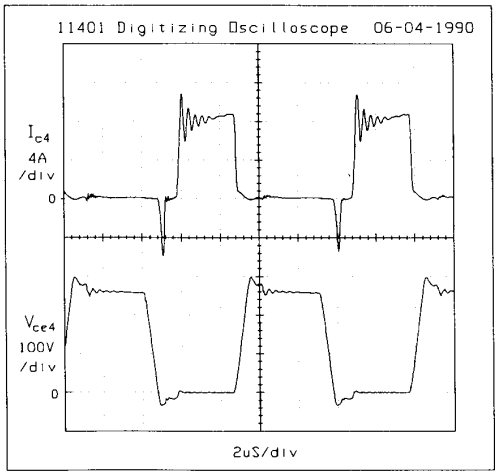

Fig. 9 Voltage and current waveforms for Q4

$V_{ce(sat)} = 1.2V$ at $i_c = 9A$. From Figs. 8 and 9, the conduction losses for Q3 and Q4 are calculated as follows:

$$P_{cond3} \approx 9 \times 1.2 \times \frac{3.9}{9} = 4.7\ W$$

$$P_{cond4} \approx 9 \times 1.2 \times \frac{2.8}{9} = 3.4\ W$$

The above data indicates that the losses on Q3 and Q4 are well balanced. The Q3 turn off loss is still less than that of Q4 even though it does not have the snubber capacitor that is required for the leading leg. This snubber capacitor helps to reduce the turn off loss of Q4 to the same level as that of Q3. Zero-current switching for Q3 is achieved at the expense of the avalanche loss on Q4. Although this increases the total loss of Q4 by 27%, the total loss of Q4 is higher than that of Q3 by only 12%. This is

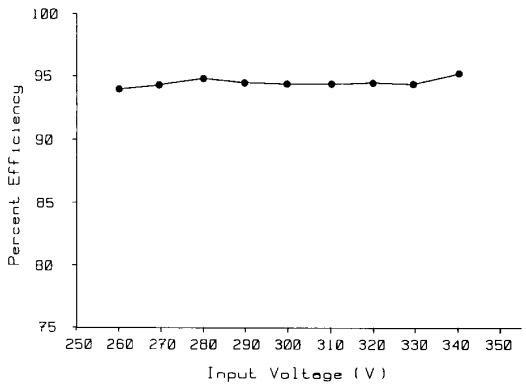

Fig. 10 Efficiency as a function of input voltage

because Q4 has lower conduction and turn on loss. It should also be pointed out that the avalanche loss represents the energy stored in the leakage inductance of the transformer. For conventional full bridge phase shift circuits, this energy will be lost as turn off loss and conduction loss in Q3 and a diode in reverse parallel with Q2.

The prototype circuit was tested for a input voltage range of 260V-340V. A plot of efficiency as a function of input voltage is shown in Fig. 10. The prototype circuit was also tested over the entire load range. Fig. 4.13 shows the switching waveforms for the minimum load where hard switching occurs. The corresponding operating conditions were as follows:

$V_s = 260$ Vdc	$I_s = 1.96$ Adc	$P_s = 509.6$ W	fre = 110 kHz
$V_o = 131$ Vdc	$I_o = 3.65$ Adc	$P_o = 477.4$ W	eff = 93.7%

Notice that hard switching does not occur until the load current decreases to 28% of full load current. The total efficiency drops by just 1.7%. Even though hard switching occurs after this point, it is tolerable because of the relatively light load.

Fig. 4.14 shows the switching waveforms for circuit operation under hard switching at 15% of full load. The operating conditions were as follows:

$V_s = 260$ Vdc	$I_s = 1.16$ Adc	$P_s = 302$ W	fre = 110kHz
$V_o = 131$ Vdc	$I_o = 1.98$ Adc	$P_o = 259$ W	eff = 85.9%

Although efficiency starts to drop significantly, the switching losses on the switching devices are not excessive as long as the peak surge current does not exceed the maximum rating of the device. As shown in Fig. 4.14, the surge current in leading leg is limited by the small inductor in series with the snubber capacitor. Finally, the circuit was also tested under no load. Operation was satisfactory, but due to the random switching of the circuit, no waveforms were taken.

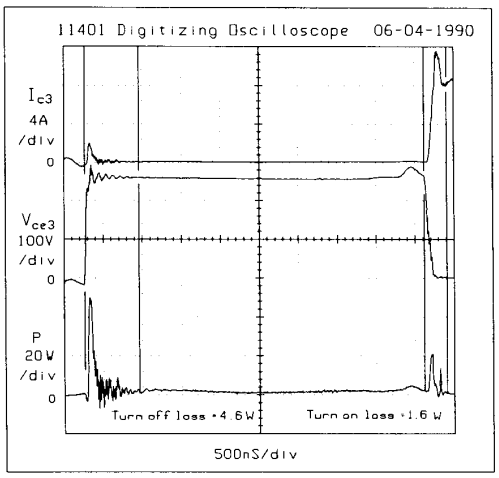

Fig. 11 Switching loss measurements for Q3

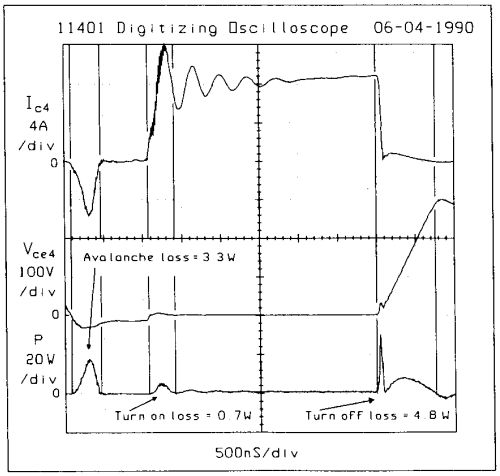

Fig. 12 Switching loss measurements for Q4

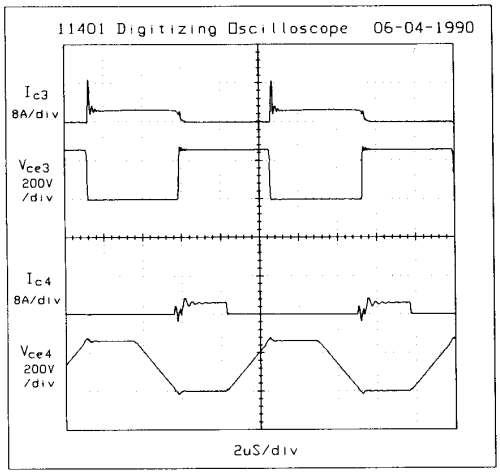

Fig. 13 Waveforms for the minimum load where hard switching occurs.

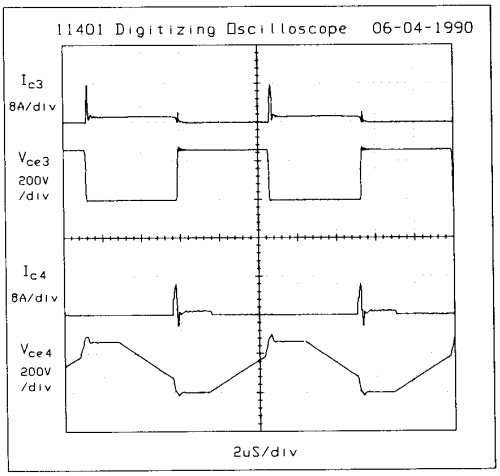

Fig. 14 Waveforms for hard switching

SUMMARY

This topology uses a new combination of zero-current and zero-voltage switching which is optimized for IGBTs. The effects of the current tailing problem are reduced by employing zero-current switching on the trailing leg and zero-voltage switching on the leading leg. The turn-off loss of the trailing leg is now transferred to the leading leg in the form of avalanche loss. However, the highly asymmetrical characteristic of the circuit coupled with a new control strategy allows larger snubber capacitors in the leading leg. Consequently, the switching loss on the leading leg is greatly reduced by the larger snubber capacitor. The new control strategy takes advantage of the asymmetrical characteristic of the circuit to ensure soft switching over a wide operating range. Therefore, unlike other soft-switching circuits, no air gap or additional commutating elements are needed. This allows much higher power and frequency combinations than previously reported, and a 1.6kW, 110kHz converter has been tested at an efficiency of 95%.

This zero-current and zero-voltage switching converter provides a new technique for applying IGBTs. It is optimized for IGBTs in the sense that it uses the reverse avalanche characteristic of the IGBT and also provides a means to remove the

storage charge of the IGBT. However, the zero-current and zero-voltage switching technique can also be adopted for bipolar transistors. In this case reverse avalanche must be achieved by inserting a Schottky diode in series with the switching device. Since bipolar transistors use minority carriers, it is also advantageous for them to turn off at zero current. The larger snubber capacitors on the leading leg are even more important for bipolar transistors, since they have higher turn-off loss than IGBTs.

ACKNOWLEDGEMENT

This research was sponsored by the NASA Lewis Research Center, Cleveland, OH, under Grants NAG 3-959 and NAG 3-1102.

REFERENCES

[1] "IXYS Mosbloc IGBT Modules," IXYS Corp. publication #4100C, San Jose, CA, Oct. 1988.

[2] T. Tsunoda, M. Hideshima, M. Kuwahara, T. Kuramoto and A. Nakagawa, "Improved 600 and 1200V IGBT with Low Turn-off Loss and High Ruggedness," PESC'90 Record, pp. 9-16, June 1990.

[3] R. Rangan, D. Y. Chen, J. Yang, and J. Lee, "Application of Insulated Gate Bipolar Transistor To Zero-Current Switching Converters," IEEE Transactions on Power Electronics, Vol. 4, No. 1, January 1989. pp. 2-7.

[4] T. Schneider and R. Bayerer, "Performance of IGBTs in Resonant Power Converters," PCIM, Vol. 16, No. 1, January 1990, pp. 15-18.

[5] "IGBT Product Catalog," International Rectifier, El Segundo, CA, January 1990.

[6] R. Fisher, K. Ngo, and M. Kuo, "A 500kHz, 250W DC-DC converter with Multiple Outputs controlled by Phase-Shifted PWM and Magnetic Amplifiers," Proceedings of HFPC, May 1988, pp. 100-110.

[7] L. H. Mweene, C. A. Wright and M. F. Schlecht, "A 1kW, 500kHz Front-End Converter for a Distributed Power Supply System," Proceedings of HFPC, 1989, pp. 423-432.

[8] R. Redl, N. Sokal and L. Balogh, "A novel Soft-Switching Full-Bridge DC/DC Converter: Analysis, Design Considerations, and Experimental Results at 1.5kW, 100kHz," PESC'90 Record, pp. 162-172, San Antonio, TX, June 1990.

[9] E. Carroll, R. Chokhawala and R. Huard, "Oscillographic Energy-Per-Event Measurement Techniques for Power Semiconductors," Proceedings of the 1989 Power Conversion Conference, pp. 302-321, October 1989.