Zero-Voltage and Zero-Current-Switching Full-Bridge PWM Converter Using Secondary Active Clamp

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***Abstract*— A new zero-voltage and zero-current-switching (ZVZCS) full-bridge (FB) pulsewidth modulation (PWM) converter is proposed to improve the performance of the previously presented ZVZCS FB PWM converters. By adding a secondary active clamp and controlling the clamp switch moderately, ZVS (for leading-leg switches) and ZCS (for lagging-leg switches) are achieved without adding any lossy components or the saturable reactor. Many advantages including simple circuit topology, high efficiency, and low cost make the new converter attractive for high-voltage and high-power (>10 kW) applications. The principle of operation is explained and analyzed. The features and design considerations of the new converter are also illustrated and verified on a 1.8-kW 100-kHz insulated gate bipolar transistor (IGBT)-based experimental circuit.**

***Index Terms*—DC–DC power conversion.**

I. Introduction

INSULATED gate bipolar transistors (IGBT's) are widely used in switching power conversion applications because of their distinctive advantages such as easiness in drive and high-frequency switching capability. The performance of IGBT's has been continuously improved, and the latest IGBT's can be operated at 10–20 kHz without including any snubber circuit. Moreover, IGBT's are replacing MOSFET's for the several or several tens of kilowatts power range applications since IGBT's can handle higher voltage and power with higher power density and lower cost compared to MOSFET's. The maximum operating frequency of IGBT's, however, is limited to 20–30 kHz [1] because of their tail-current characteristic. To operate IGBT's at high switching frequencies, it is required to reduce the turn-off switching loss. Zero-voltage switching (ZVS) with a substantial external snubber capacitor or zero-current switching (ZCS) can be a solution. The ZCS, however, is deemed more effective since the minority carrier is swept out before turning off [6].

ZVS full-bridge (FB) pulsewidth modulation (PWM) converters have received considerable attention in recent years [2]–[5]. This converter is controlled by a phase-shifted PWM technique which enables the use of all parasitic elements in the bridge to provide ZVS conditions for the switches. Distinctive advantages including ZVS with no additional components, and low-device voltage/current stresses make it very attractive for high-frequency high-power applications, where MOSFET's are predominantly used as the power switches. The IGBT's, however, are not suited for the ZVS FB PWM converter because the ZVS range is quite limited unless the leakage inductance is very large. In addition, several demerits such as duty-cycle loss and parasitic ringing in the secondary limit the maximum power rating of the converter.

To apply IGBT's for a high-frequency converter, a ZVZCS FB PWM converter was presented [7]. IGBT's with no antiparallel diodes are used for all primary switches. During the freewheeling period, the primary current is reset by using reverse avalanche-breakdown voltage of the leading-leg IGBT's, which provides ZCS condition to lagging-leg IGBT's. However, it has some drawbacks as follows. The stored energy in the leakage inductance is completely dissipated in the leading-leg IGBT's. There is parasitic ringing in the primary during the freewheeling period. The maximum controllable duty cycle is limited since the reverse avalanche-breakdown voltage is low (15–30 V) and fixed. Therefore, the overall efficiency will be deteriorated unless the leakage inductance is very low.

Another approach for ZVZCS FB PWM converter was presented [8]. By utilizing a dc blocking capacitor and adding a saturable inductor in the primary, the primary current during the freewheeling period is reset, which provides ZCS condition to the lagging-leg switches. Meanwhile, the leading-leg switches are still operated with ZVS. The stored energy in the leakage inductance is recovered to the dc blocking capacitor and finally transferred to the load. By increasing the blocking capacitor voltage (i.e., by reducing the capacitance of the blocking capacitor), wide duty-cycle control range is attainable even when the leakage inductance is relatively large. This converter can be effectively applied to several kilowatts power range applications. Some demerits including loss in saturable inductor and its cooling problem hinder further increase of the power level above 10 kW.

This paper proposes a novel ZVZCS FB PWM converter (see Fig. 1) to improve the performance of the previously presented ZVZCS FB PWM converters [7], [8]. The ZVS mechanism of leading-leg switches is the same as that of the converters [2]–[5], [8]. The ZCS of lagging-leg switches, how-

Manuscript received July 18, 1996; revised October 14, 1997. Recommended by Associate Editor, L. Xu.

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Publisher Item Identifier S 0885-8993(98)04842-X.

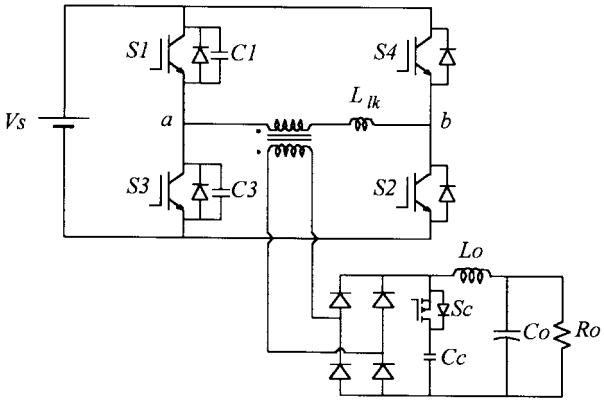


Fig. 1. Circuit topology of the proposed ZVZCS FB PWM converter.

ever, is achieved by adding an active clamp in the secondary rectifier and by controlling it moderately. No lossy components are added to achieve ZVZCS operation. The duty-cycle loss is almost negligible although the leakage inductance is a little bit large since a high voltage (higher than input voltage) is applied to the leakage inductance to reset the primary current during freewheeling period. So, the new converter overcomes most of the limitations of the soft-switching FB PWM converters, which makes the new converter very attractive for high-voltage high-power (>10 kW) applications, where IGBT's are predominantly used as the power switches.

The basic operation and features of the proposed converter are illustrated. A 1.8-kW 100-kHz prototype has been built using IGBT's (a MOSFET for the clamp switch) and tested to verify the principle of operation.

II. Operation and Analysis

The basic structure of the proposed ZVZCS FB PWM converter is the same as that of the ZVS FB PWM converter with the active clamp in the secondary side [3]. The control of the primary switches is also the same—phase-shift PWM control. The control of active clamp is a little different, which will be explained later in this section.

To illustrate steady-state operation, several assumptions are made as follows.

1) All components are ideal.
2) The output filter inductor is large enough to be treated as a constant current source during a switching period.
3) The clamp capacitor is large enough to be treated as a constant voltage source during a switching period.

The new converter has eight operating modes within each operating half cycle. The equivalent circuits and operation waveforms are shown in Figs. 2 and 3, respectively.

A. Mode 1

$S1$ and $S2$ are conducting, and the input power is delivered to the output. At the beginning of this mode, the rectifier voltage, which was increasing, is clamped by V_c through the body diode of Sc. The stored energy in the leakage inductance, which is generated by the resonance between the leakage inductance and parasitic capacitance, is recovered to the clamp

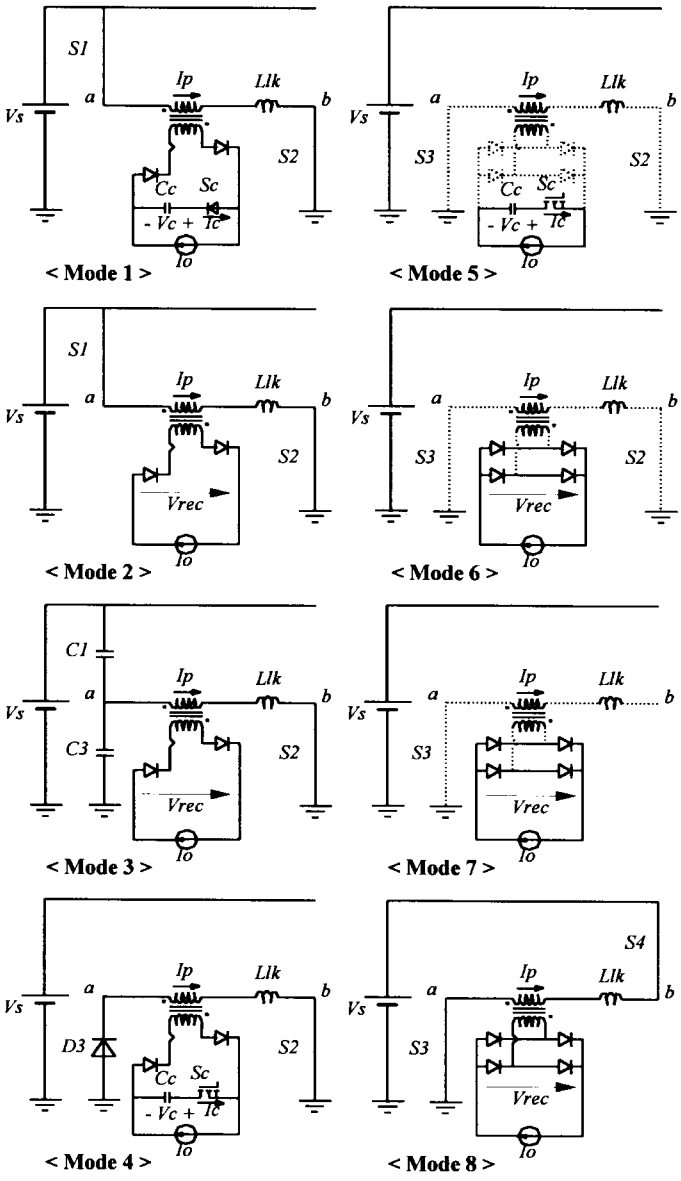


Fig. 2. Operation mode diagrams for eight modes.

capacitor. So, the primary current is decreased as follows:

$$I_p(t) = \frac{1}{L_{\text{lk}}}\left(V_s - \frac{V_c}{n}\right) \cdot t \tag{1}$$

where n is the transformer turns ratio and the clamp capacitor current can be expressed as follows:

$$I_c = \frac{I_p}{n} - I_o. \tag{2}$$

This mode ends when I_c becomes zero. The duration of this mode depends on the leakage inductance and the junction capacitance and the reverse recovery time of the rectifier diodes.

B. Mode 2

The body diode of Sc blocks and the secondary rectifier voltage becomes

$$V_{\text{rec}} = nV_s. \tag{3}$$

$S1$ and $S2$ are still on and the powering mode is sustained during this mode.

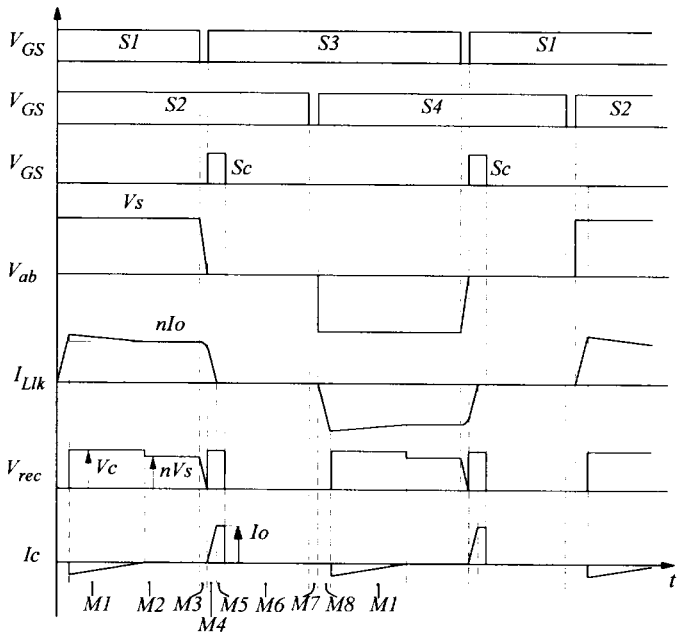


Fig. 3. Operation waveforms.

C. Mode 3

According to the given duty cycle, $S1$ is turned off and then the reflected load current to the primary charges $C1$ and discharges $C3$. The switch voltage increases linearly as follows:

$$V_{S1}(t) = \frac{nI_o}{C1 + C3} \cdot t. \tag{4}$$

The turn-off process of $S1$ is low loss if the external capacitor is large enough to hold the switch voltage at near zero during the switch turn-off time. During this mode, the secondary rectifier voltage is also decreased with almost same rate. At the end of this mode, $D3$ is turned on.

D. Mode 4

After $D3$ starts conducting, $S3$ can be turned on with ZVS. The load current freewheels through the primary side, $D3$ and $S2$. To reset the primary current, the clamp switch is turned on and then the rectifier voltage becomes V_c. This voltage is applied to the leakage inductance, the primary current is linearly decreased with the slope of $V_c/nL_{\rm lk}$, and I_c is linearly increased satisfying (2). The primary current reaches zero at the end of this mode.

E. Mode 5

The rectifier diodes are turned off since the primary current is zero and Sc is still on. During this mode, the primary current sustained at zero and Cc supplies whole load current.

F. Mode 6

The Sc is turned off and then the rectifier voltage is dropped to zero. The load current freewheels through the rectifier itself. No current flows through the primary.

G. Mode 7

$S2$ is turned off with ZCS. No tail current exists since all minority carriers are eliminated by recombination. This mode is dead time between $S2$ and $S4$.

H. Mode 8

At the end of freewheeling mode, $S4$ is turned on. This turn-on process is also ZCS since the primary current cannot be increased abruptly and no diode reverse recovery is involved. The primary current I_p is linearly increased with the slope of $V_s/L_{\rm lk}$. The rectifier voltage is still zero. This is the end of an operating half cycle.

III. Features of the Proposed Converter

A. Effective Soft Switching (ZVZCS)

Soft-switching mechanism (ZVS for leading-leg switches and ZCS for lagging-leg switches) of the proposed converter has exactly the same as those of the ZVZCS converters presented in [7] and [8]. The converters [7], [8] use lossy components to achieve ZCS of lagging-leg switches. The stored energy in the leakage inductance is completely dissipated in the leading-leg IGBT's during freewheeling mode [7] or there exists the core loss of saturable reactor [8]. In addition, additional loss exists in the clamp resistor for both converters if the passive clamp circuit is used to clamp the secondary rectifier voltage. Therefore, both converters have limited power range (several kilowatts). In the proposed converter, however, ZCS of lagging-leg switches is achieved more efficiently by modifying control of the active clamp [3]. No lossy components are involved in achieving ZCS, and no parasitic ringing is generated in the secondary rectifier. So, the proposed converter can handle a higher power level (>10 kW).

The ZCS of lagging-leg switches is achieved with whole load ranges, and the ZVS of the leading-leg switches is also achieved with a wide load range. The ZVS and the ZCS ranges are also the same as those of [7] and [8].

B. More Reduced Conduction Loss

The primary voltage, current, and secondary voltage of the proposed converter are compared to those of the ZVS [2]–[5] and ZVZCS converters [7], [8] as shown in Fig. 4. The ZVS converter has considerable duty-cycle loss since large leakage inductance is required to obtain reasonable ZVS range. The ZVZCS converters [7], [8] improves the overall efficiency by removing the freewheeling current in the primary and reducing the duty-cycle loss, and large leakage inductance is not necessary. The maximum duty cycle, however, is limited by the primary current reset time $T_{\rm reset}$, which is determined by the applied voltage to the leakage inductance $V_{L_{\rm lk}}$ during freewheeling period as follows:

$$T_{\rm reset} = L_{\rm lk} \frac{nI_o}{V_{L_{\rm lk}}}. \tag{5}$$

The $T_{\rm reset}$ of the ZVZCS converters in [7] and [8] is considerably large since low reverse voltage (several tens of volts)

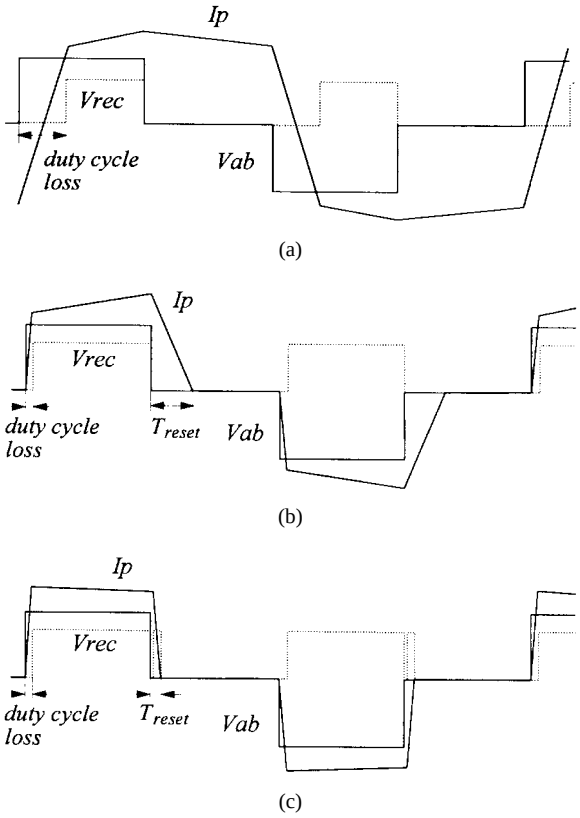


Fig. 4. Comparison of the simplified waveforms of primary voltages and currents and secondary rectifier voltages. (a) ZVS PWM converter. (b) ZVZCS PWM converters [7], [8]. (c) Proposed converter.

is applied to the leakage inductance, which is a kind of duty-cycle loss. In the proposed ZVZCS converter, however, a small $T_{\rm reset}$ is achieved since the high reverse voltage (V_c/n) is applied to the leakage inductance. So, the overall efficiency of the proposed converter is improved due to low duty-cycle loss as well as small $T_{\rm reset}$.

C. Duty-Cycle Boost Effect

The duty cycle of the secondary rectifier is usually lower than that of the primary because of the duty-cycle loss. In the proposed converter, however, the duty cycle of the rectifier can be higher than that of the primary as shown in Fig. 5. This phenomenon is named as *duty-cycle boost effect*. The duty-cycle boost effect is caused by the operation of the active clamp from the beginning of freewheeling period to provide ZCS condition to the lagging-leg switches. This means that the stored energy in the leakage inductance is recovered to the clamp capacitor and finally transferred to the load by means of the duty-cycle boost effect. This feature is very important for the ZVZCS converters, which use IGBT's for main switches. The duty cycle of the primary is more limited than MOSFET-based ZVS converters since the minimum dead time ($T_{\rm ZCS}$ in Fig. 5) is required to achieve a complete ZCS turn off of the lagging-leg switches which is the required time for minority carrier recombination in the IGBT. The effective duty cycle of the proposed converter, however, can be increased to near unity due to the duty-cycle boost effect. The effective duty

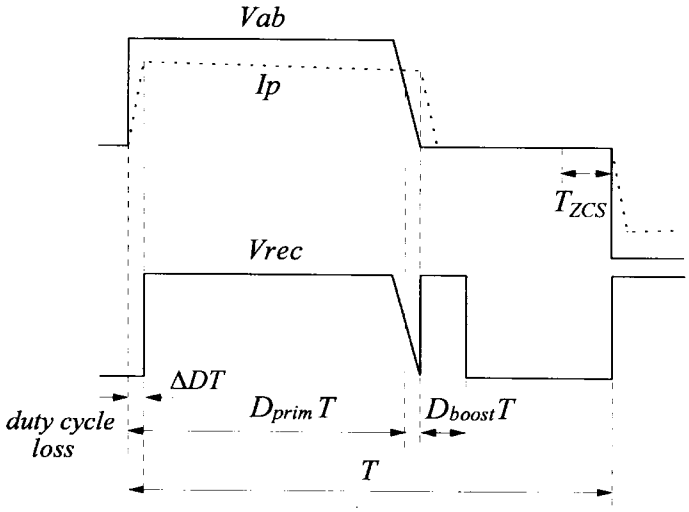


Fig. 5. Primary and secondary rectifier voltage waveforms.

cycle of the proposed converter can be expressed as follows:

$$D_{\rm eff} = D_{\rm prim} - \Delta D + D_{\rm boost} \tag{6}$$

where ΔD is the duty-cycle loss. The $D_{\rm boost}$ is determined directly by the turn-on time of the clamp switch. The duty-cycle boost effect also helps to improve the overall efficiency.

IV. Design Considerations

A. Decision of Dead Times

An appropriate dead time is required for both leading- and lagging-leg switches to achieve maximum performance.

1) Dead Time for Leading-Leg Switches: The dead time for leading-leg switches is determined by two factors—the ZVS range and maximum duty cycle of the primary side. The minimum dead time is determined by ZVS range as follows:

$$T_{d,\rm lead} \geq (C1 + C3)\frac{V_s}{nI_{o,\rm ZVS}} \tag{7}$$

where $I_{o,\rm ZVS}$ is given ZVS range as one of design parameters. The maximum dead time is limited by the maximum duty cycle of the primary side.

2) Dead Time for Lagging-Leg Switches: The minimum dead time of lagging-leg switches is determined by the time $T_{\rm ZCS}$ to achieve a complete ZCS of the lagging-leg switches as follows:

$$T_{d,\rm lag} \geq T_{\rm ZCS} \tag{8}$$

where the $T_{\rm ZCS}$ is the minority carrier recombination time of IGBT's. The maximum dead time is also limited by the maximum duty cycle of the primary side.

B. Decision of Clamp Switch On Time

The illustrative waveforms of the secondary rectifier voltage and the clamp capacitor current according to the turn-on time of Sc are depicted in Fig. 6. To achieve a complete ZCS of lagging-leg switches, the primary current should be reset. The

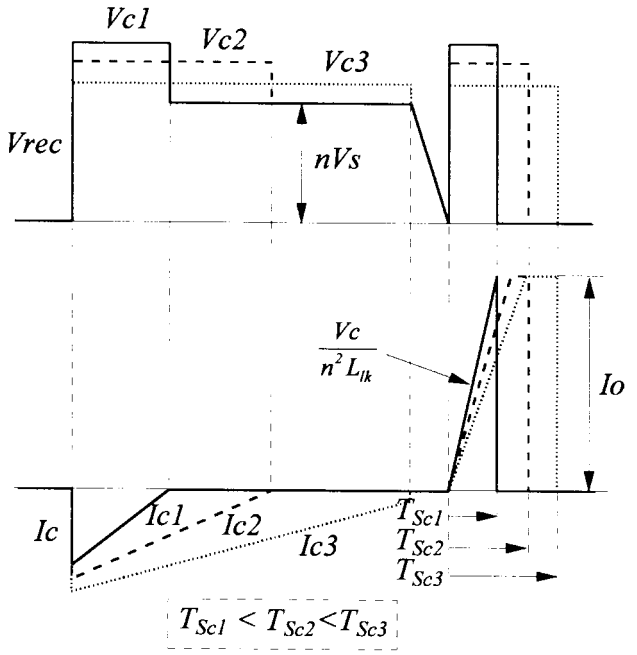


Fig. 6. Illustrative waveforms of the rectifier voltage and the clamp capacitor current.

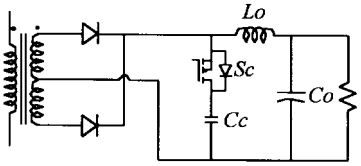


Fig. 7. Circuit diagram of the active clamp circuit for a center-tapped transformer.

required turn-on time $T_{\rm Sc}$ of Sc is obtained as follows:

$$T_{\rm Sc} \geq \frac{n^2 L_{\rm lk}}{V_c} I_{o,\max}. \tag{9}$$

The clamp capacitor is charged up during powering period and discharged by turning on of Sc as shown in Fig. 6. The discharging current is quickly increased with the slope depicted in Fig. 6 and stays constant after it reaches load current I_o. The increasing rate of discharging current is the same as the decreasing rate of the primary current. If the turn-on time of Sc is increased, the clamp capacitor voltage V_c is decreased and more current flows through the clamp capacitor as shown in Fig. 6. Therefore, $T_{\rm Sc}$ needs to be kept as small as possible to reduce the conduction loss of clamp switch and in turn allow use of a small switch for Sc. The clamp capacitor voltage is regulated automatically as shown in Fig. 6.

C. Active Clamp Circuit for Center-Tapped Transformer

The proposed ZVZCS power conversion technique can also be applied for the center-tapped transformer as shown in Fig. 7. The basic operation principle is exactly the same as that of the simple output transformer except diode voltage.

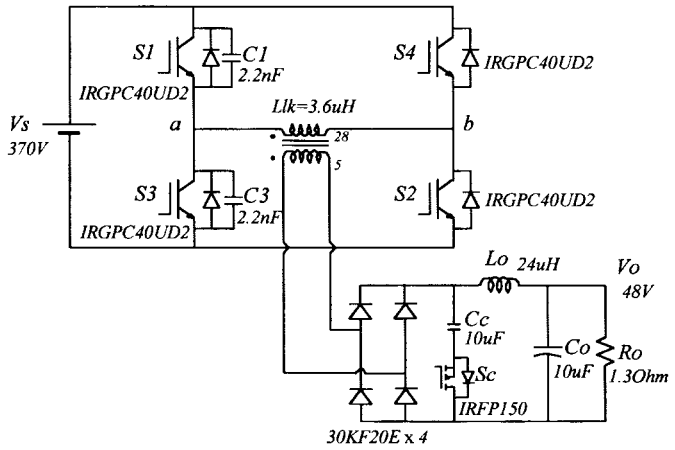


Fig. 8. Experimental circuit diagram of the proposed converter.

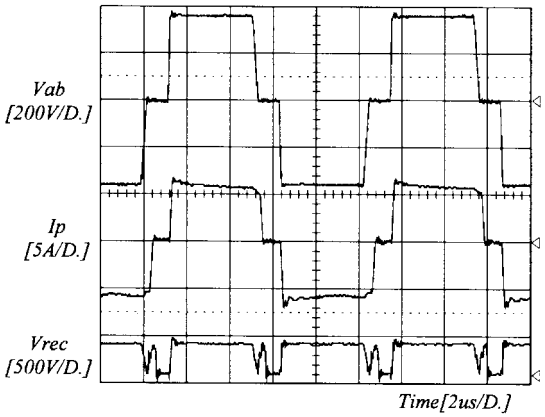
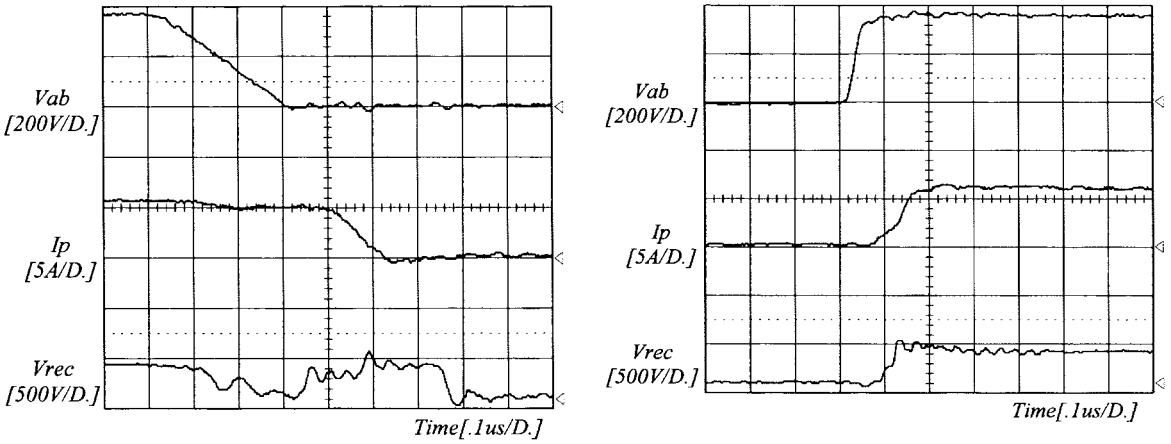


Fig. 9. Experimental waveforms of primary voltage and current and secondary rectifier voltage.

V. Experimental Results

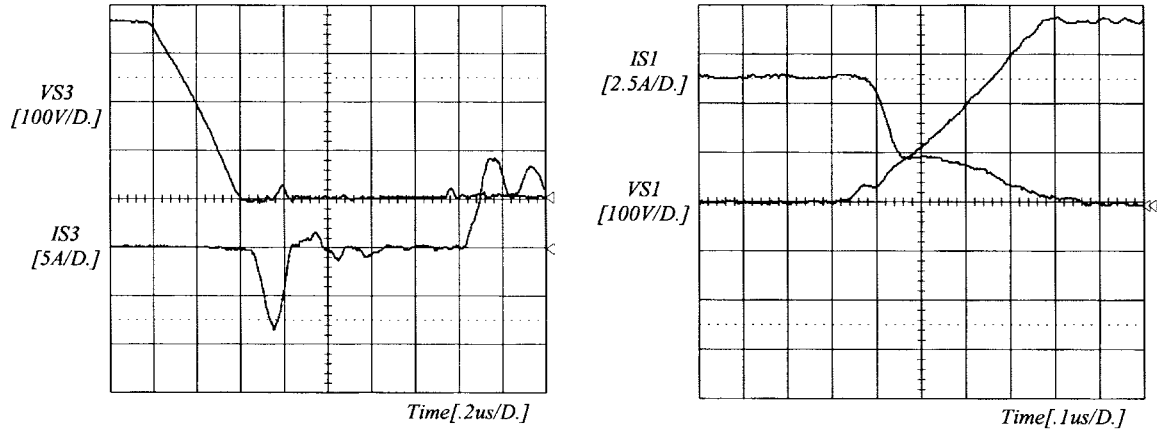
A 1.8-kW 100-kHz prototype of the proposed ZVZCS FB PWM converter has been built and tested to verify the principle of operation. Fig. 8 shows the experimental circuit with the part numbers and the circuit parameters. The transformer is built using an EE/55/55 core with the turns ratio of $Np : Ns = 28 : 5$. The leakage inductance measured at the switching frequency is 3.6 uH. IRGPC40UD2 IGBT's are used for the primary switches. The recommended switching frequency for the IRGPC40UD2 provided by the data sheet is only 10–20 kHz. As will be shown, these IGBT's can be operated at 100 kHz without any detrimental effects on the efficiency.

Fig. 9 shows the waveforms of the primary voltage and current and the secondary rectifier voltage at full load (nominal duty cycle of 0.78), and Fig. 10 shows the extended waveforms at the switching transitions of leading and lagging legs. All waveforms are well matched with the expected ones. The primary voltage shows a slow downslope due to the external capacitors added to the leading-leg switches and fast upslope. The duty-cycle loss is about 0.1 μs. The primary current is quickly reset right after the primary voltage is dropped to zero and sustained during the freewheeling period. The primary current reset time is only 0.15 μs. The turn-on time of the active switch is about 0.35 us. Fig. 11 shows the extended switching



(a) (b)

Fig. 10. Extended waveforms at (a) leading-leg and (b) lagging-leg switching transitions.



(a) (b)

Fig. 11. Extended ZVS switching waveforms of leading-leg switches: (a) turn on and (b) turn off.

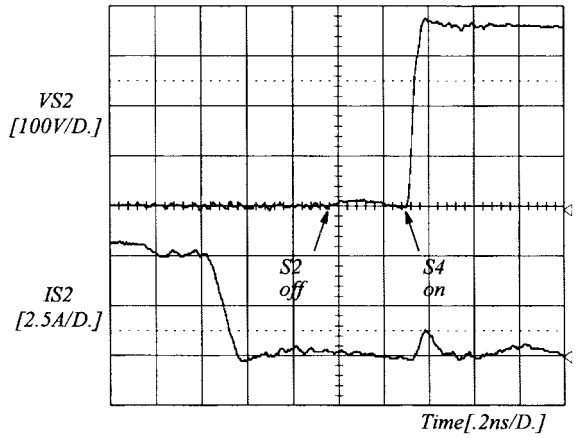


Fig. 12. Extended ZCS waveforms of lagging-leg switches.

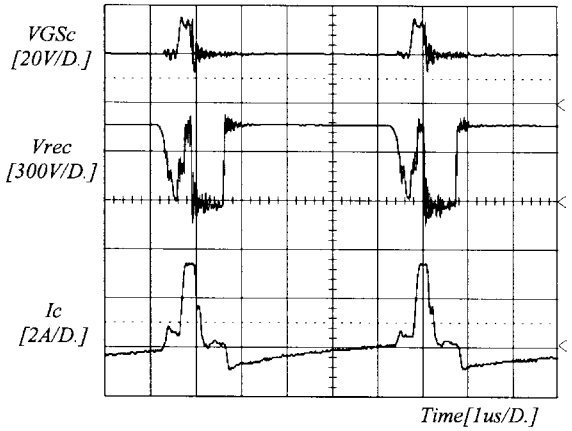


Fig. 13. Waveforms of secondary active clamp.

waveforms of leading-leg switches. It can be seen that the antiparallel diode current flows for a short time and stays zero, and, thus, a complete ZVS turn on is achieved. The tail current is seen, but the turn-off switching loss is remarkably reduced comparing to hard switching since the rising slope of the switch voltage is slow. The ZVS range for the leading-leg switches is about 20% of full load. Fig. 12 shows the extended switching waveforms of lagging-leg switches. It can be seen that a complete ZCS turn off is achieved since the primary current is zero during the whole freewheeling period and the turn-on process of the other switch is almost ZCS. Small pulse current during turn-on transition is the charging current of the switch output capacitor. Fig. 13 shows the waveforms of the secondary active clamp. The clamp switch is turned on for a

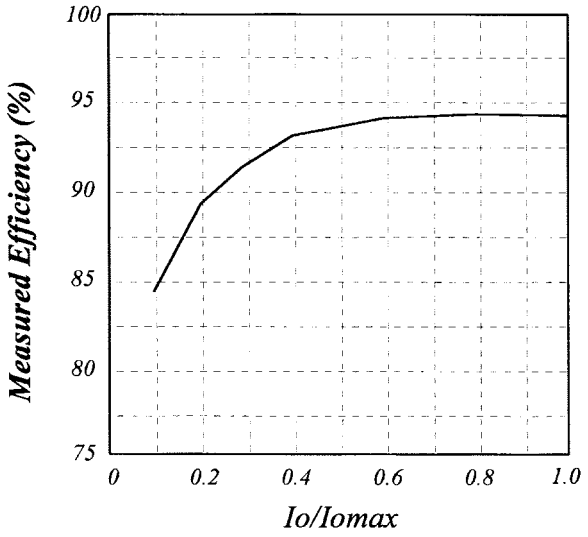


Fig. 14. Measured efficiencies.

very short time compared to the operating period (7%). The rectifier voltage waveform is a little noisy since the clamp switch operates under hard switching. The clamp capacitor current waveform is the same as the expected.

Fig. 14 shows the measured efficiencies of the proposed ZVZCS FB PWM converter. The maximum overall efficiency is about 94% at full load. The efficiency improvement is not much comparing to the previous ZVZCS converter [8], but it will be considerable at higher power (>10 kW) applications.

VI. Conclusion

A novel ZVZCS FB PWM converter using a secondary active clamp is presented. The operation, features, and design considerations are illustrated and verified by the experimental results on a 1.8-kW 100-kHz IGBT-based prototype.

It is shown that ZVS for leading-leg switches and ZCS for lagging-leg switches are achieved by the help of the active clamp. The efficiency attained at full load was about 94%. The proposed converter has distinctive advantages over the previously presented ZVZCS converters as follows:

1) ZVS and ZCS without any lossy components;
2) wide ZVS and ZCS range;
3) high duty cycle is attainable;
4) more reduced conduction loss in the primary;
5) no severe parasitic ringing.

Many advantages of the new circuit make the proposed converter very promising for high-voltage (400–800 V) high-power (>10 kW) applications with high-power density.

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