A Unified SPICE Compatible Average Model of PWM Converters

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Abstract—A simple, unified, and topology-independent model of basic PWM converters is developed using the switched inductor approach presented in [1]. The model is compatible with SPICE or other similar general purpose electronic circuit simulators. It can be used to simulate dc, small signal, and transient behavior of PWM converters operating in both DCM (discontinuous conduction mode) and CCM (continuous conduction mode). During simulation, the model automatically follows the CCM and DCM operation, with fewer convergence problems compared to previous simulation models. An effective measurement technique using the HP3562A dynamic signal analyzer (DSA) is presented and applied to compare simulation runs with experimental data. The two were found to be in good agreement.

I. INTRODUCTION

PWM DC-DC converters are nonlinear systems with a high switching rate as compared to their inherent time constants. Hence, exact time domain simulation calls for a heavy numerical computation which has to be carried out for each switching cycle. This problem can be alleviated by applying models which emulate the average behavior of such systems in the low frequency range. Averaging models were developed using two main approaches: Analytical averaging, particularly state-space averaging [2] and "circuit-oriented" averaging methods [1], [4]–[9].

A common feature of the models that have been described hitherto is that each applies to a specific conduction mode. Hence, a severe limitation of these models is their inability to cope with 'real life' situations which are encountered, for example, when converters are subjected to large load changes or during turn-on transients. This limitation hampers the use of previous described models by general purpose circuit simulators such as SPICE [10]. Circuit simulation can be based, in principle, on the state-space averaging method [11]–[12], on circuit-averaging techniques or on PWM switch models [6]–[7]. But previous models assume that the converters are in the CCM or in the DCM. Some authors have proposed [11]–[13] SPICE models which are capable of switching between the CCM and DCM modes. However, these models are still topology dependent and are relatively complex since

they are basically composed of two separate circuits: one for the CCM and the other for the DCM.

In this paper we propose a simple unified circuit-oriented model for PWM converters, which explore two basic ideas:

1) Switched inductor modeling.
2) Application of the fact that the CCM is a limit, or special case, of the DCM.

The accuracy and validity of the proposed simulation approach were tested by measuring the large and small signal response of a boost converter with an HP3562A Dynamic Signal Analyzer (DSA) [14].

II. THE UNIFIED SWITCHED INDUCTOR MODEL (USIM)

In this section, the SIM (switched inductor model) originally introduced in [1] for PWM converters operating in CCM, is extended to describe both the CCM and the DCM conditions. Practical PWM converters consist of a linear part and a nonlinear part which include the PWM switch or switches. Close examination of PWM converters (buck, boost, buck-boost) reveals that they all rely on a nonlinear subcircuit: a switched inductor, which serves as a temporary energy storage element between the input and output terminals (Fig. 1). Hence, modeling and simulation of switch mode converters can be simplified if the nonlinear part is replaced by an equivalent circuit that is compatible with general purpose simulators such as SPICE [10]. The basic switched inductor assembly (Fig. 2(a)) consists of an inductor that is switched at one end between two terminals (B) and (C) at a frequency f_s and a duty-ratio D_{ON}, for port (B), and D_{OFF} for port (C), where

$$D_{OFF} = 1 - D_{ON} \quad \text{for CCM}$$

$$D_{OFF} < 1 - D_{ON} \quad \text{for DCM}.$$

The equivalent circuit of the switched inductor is easily developed by considering the average signals of the ports (A), (B), and (C) under the assumption that the switching period is much smaller than the basic time constants of the converter system. Under these assumptions, the terminal voltage of ports (B) and (C) do not change markedly over a switching period. Hence, the average voltage across the inductor terminals for CCM and DCM can be expressed by

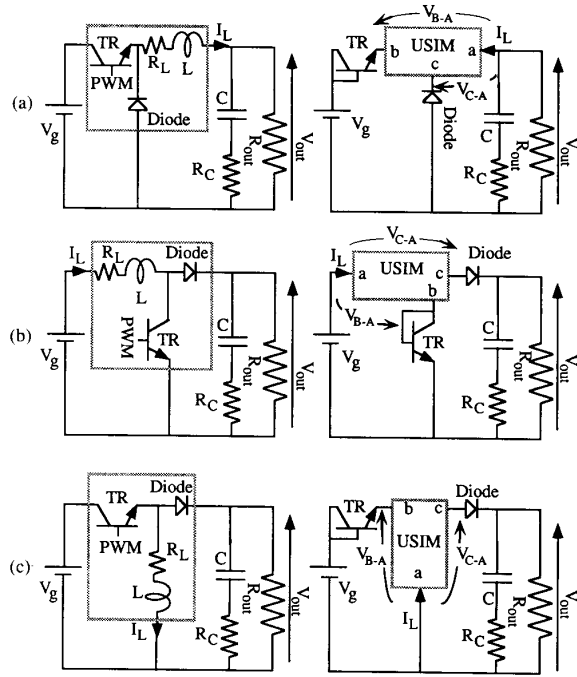$$V_L = V_{C-A} D_{OFF} + V_{B-A} D_{ON}. \tag{1}$$

Fig. 1. Basic converter topologies and their equivalent circuit when represented by USIM. (a) Buck. (b) Boost. (c) Buck-boost.
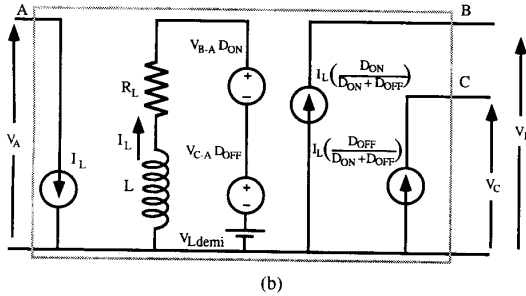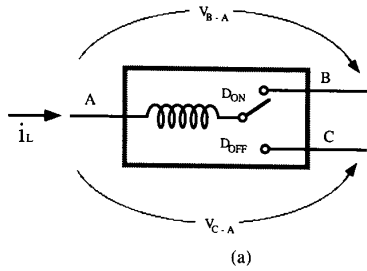

Fig. 2. Switched inductor. (a) Hardware configuration. (b) Unified Switched Inductor Model (USIM).

To derive the average currents through ports (A), (B), and (C) we consider the various possibilities of the inductor current waveforms (Fig. 3). Notice that Fig. 3 is normalized to I_{pk}, the inductor current at the switching instant from ON to OFF. In the general case, one can distinguish between types of operation: (a) which corresponds to the
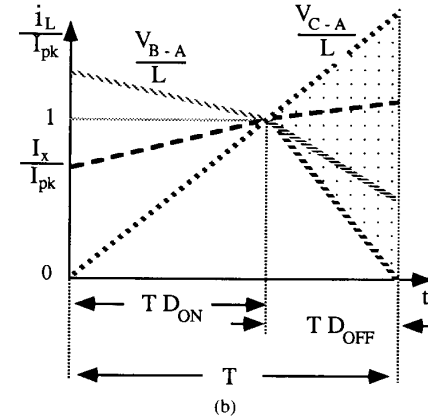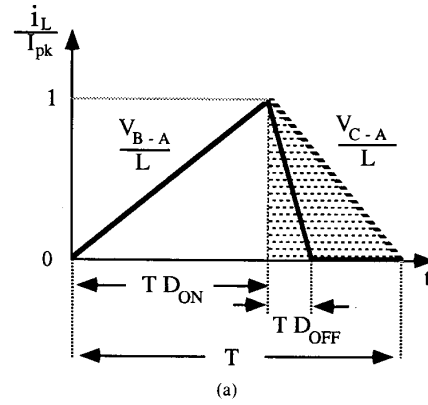

Fig. 3. Possible inductor current wave forms in various transient cases. (a) DCM. (b) CCM.

DCM and (b) which corresponds to the CCM (see Fig. 3(a)-(b)).

The USIM is developed in two steps as follows:

First Step: We develop the model for the DCM. In this case, the inductor current wave form is described by the solid curve of (Fig. 3(a)). I_{pk} is in this case the peak inductor current during the DCM operation. The relationship between I_{pk} and I_L (the average inductor current which will always have the same polarity as I_{pk}) can be expressed as

$$I_L = \frac{I_{pk}(D_{ON} + D_{OFF})T}{2T} = \frac{1}{2}I_{pk}(D_{ON} + D_{OFF}) \quad (2)$$

where $T = 1/f_s$ is the switching period.

Similarly, the average currents of the ports are found to be

$$I_A = I_L \quad (3a)$$

$$I_B = \frac{I_{pk}D_{ON}T}{2T} = \frac{1}{2}I_{pk}D_{ON} \quad (3b)$$

$$I_C = \frac{I_{pk}D_{OFF}T}{2T} = \frac{1}{2}I_{pk}D_{OFF} \quad (3c)$$

Simple manipulation of (2) and (3) yields the following relationships:

$$I_A = I_L \tag{4a}$$

$$I_B = \frac{D_{ON}}{D_{ON} + D_{OFF}} I_L \tag{4b}$$

$$I_C = \frac{D_{OFF}}{D_{ON} + D_{OFF}} I_L. \tag{4c}$$

It should be emphasized that the method of expressing the average current of the ports as a function of the inductor's average current is compatible with the concept of average behavior of the USIM.

Since (4) converges to the CCM case when $D_{OFF} = 1 - D_{ON}$, the model is in fact an extension of the model described in [1].

A SPICE-compatible equivalent circuit that emulates the relationships of (1) and (4) is given in Fig. 2(b). Note that except for I_L the dependent voltage and current sources are nonlinear. That is, they are a function of a product of two variables. This, however, does not pose any problem when the dc, large signal, or small signal behavior of such a circuit is simulated by readily available electronic circuit simulators. Practically all commercially available simulators include, as a standard feature, the capability of handling nonlinear dependent sources of this type. In dc and transient analysis the simulators will solve numerically the nonlinear node equations of the system. In small signal analysis, the simulators first evaluates the linearized equivalent circuit, around the working point, and then solve the linear node equations of the system.

The equivalent circuit of Fig. 2(b) is topology independent but must be placed in the correct orientation for each structure. In a buck converter, for example (Fig. 1(a)), the input power will be connected to port (B), the steering diode to port (C), and the load to port (A). In this case, the steady-state currents and the voltage V_{C-A} are negative with respect to the sign convention of Fig. 2(a). In a boost converter (Fig. 1(b)), the steady-state currents and the voltage V_{C-A} are positive, and in the buck-boost converter (Fig. 1(c)) they are negative with respect to the sign convention of Fig. 2(a).

To run a numerical simulation, the user must provide the values of the components as well as complete information on the sources. That is, to run a simulation one has to supply equivalent signal sources that represent D_{ON} and D_{OFF}. D_{ON} is normally an externally supplied signal, either from an independent generator (for open loop systems) or from a controller that generates a D_{ON} as a function of the error signal. In the CCM D_{OFF} is simply $1 - D_{ON}$. For the DCM, D_{OFF} has to be calculated as a function of V_{C-A} and the inductor's peak current (I_{pk}). That is, by evaluating the time it takes the inductor current, with an initial value of I_{pk}, to reach zero level:

$$T_s D_{OFF}^* = -L \frac{I_{pk}}{-V_{C-A}} \tag{5}$$

For the DCM:

$$D_{OFF} = D_{OFF}^*.$$

It is important to note that in the DCM, V_{C-A} and I_{pk} will be either both positive or both negative (as per the sign convention of Fig. 2(a)), hence D_{OFF}^* is always a positive value.

Since a USIM-based simulation continuously produces the averaged values of the converter variables, I_{pk} can be constantly linked to I_L by reapplying (2) and (3):

$$I_{pk} = \frac{2I_B}{D_{ON}} = \frac{2I_C}{D_{OFF}} = \frac{2I_L}{D_{ON} + D_{OFF}} \tag{6}$$

Equations (5) and (6) can now be combined to derive the expression for D_{OFF}^*

$$D_{OFF}^* = \frac{2L}{T} \frac{I_L}{V_{C-A}(D_{ON} + D_{OFF}^*)} \tag{7}$$

Equation (7) is a quadratic equation in D_{OFF}^* and may have one, nonphysical, negative root. Hence, only the positive root is chosen as the solution of (7).

Second Step: The model for the DCM is extended to describe the CCM. In this case,

$$D_{OFF} = 1 - D_{ON}.$$

Close examination of (7) reveals that, for the CCM, it will always yield a solution $D_{OFF}^* > 1 - D_{ON}$ if only the positive solution of D_{OFF}^* is chosen. Hence, D_{OFF} (for the CCM) can be easily obtained by 'clamping' the positive root of (7) to $(1 - D_{ON})$. This will automatically produce the correct D_{OFF}^* for both the DCM and the CCM operations.

During a CCM transient, the polarity of V_{C-A} could be reversed with respect to the sign convention of Fig. 2(a) while I_L still retains the polarity shown in Fig. 2(a). This will cause the inductor current to continue to increase during the OFF period as illustrated in Fig. 3(b). This special case is found only in a boost converter, when the output voltage is lower than the input voltage. The worst case is when the output voltage is zero, a situation which is depicted by the straight line in Fig. 3(b). It should be noted that for buck and buck-boost topologies, V_{C-A} and I_L are always negative values (as per the convention of Fig. 2(a)). Hence, during a CCM transient in a boost converter, D_{OFF}^* might assume negative values when calculated by (5). To remedy this nonphysical situation, the ratio (V_{C-A}/I_L) is replaced by its absolute value in (5) and (7). The corrected equation for the evaluation of D_{OFF}^* is thus:

$$D_{OFF}^* = \frac{2L}{T_s} \frac{|I_L|}{|V_{C-A}|(D_{ON} + D_{OFF}^*)} \tag{8}$$

The magnitude of D_{OFF}^* can now be used to select the correct D_{OFF} during simulation:

$$D_{OFF} = 1 - D_{ON} \quad \text{when} \quad D_{OFF}^* \geq 1 - D_{ON} \text{ (CCM)}$$

$$D_{OFF} = D_{OFF}^* \quad \text{when} \quad D_{OFF}^* < 1 - D_{ON} \text{ (DCM)}. \tag{9}$$

Fig. 4. Equivalent circuit for evaluation of D_{OFF} by HSPICE simulation.

It can easily be shown that for a boost converter operating in the CCM, if V_{C-A} is negative with respect to I_L (Fig. 2(a)), I_L is greater than zero and the positive root of (8) is chosen, it will still yield $D_{OFF}^* > 1 - D_{ON}$. Hence, (8) and (9) cover all practical cases. However, during the initial computation steps, and if the initial conditions are $D_{OFF}^* = 0$, $I_L = 0$ and $V_{C-A} < 0$, the first one or two calculated values of D_{OFF}^* will be smaller than $1 - D_{ON}$. In this CCM transient stage, D_{OFF} will be wrongly calculated. However, practical simulation runs show that this error is negligibly small (see experimental results (Fig. 9).

Another numerical problem that could be encountered when applying the USIM in numerical simulation, occurs when V_{C-A} is zero. In these cases the numerical computation of the simulation program may not converge. This problem arises when the output voltage of the buck or the buck-boost is zero or when the input voltage is equal to the output voltage in the boost converter. The problem is easily solved by limiting the minimum of the absolute value of V_{C-A} to be greater than some small arbitrary positive number (e.g., 10^{-6} V).

III. THE D_{OFF} GENERATOR

The USIM circuit of Fig. 2(b) is a direct equivalent circuit implementation of (1) and (4). Note that in this model, the duty cycles D_{ON} and D_{OFF} are represented by voltages and that a 1 : 1 scaling factor is conveniently chosen (i.e., D is expressed in volts). To run this model on a general purpose simulator, D_{ON} and D_{OFF} should be specified as voltage sources. As already pointed out, D_{ON} will normally be provided by either an 'external' source (for open loop simulation) or as a function of the output (in closed loop simulation). D_{OFF} however, is a dependent variable and must be continuously evaluated through (8) and (9).

An HSPICE [15] compatible D_{OFF} generator that realizes (8), including the D_{OFF} limiter for the CCM, is depicted in Fig. 4(a)–(d). Actual input file listings are given in the Appendix. Although the realization is shown in terms of HSPICE, the model is by no means limited to one particular computer circuit simulation package. Nor does the application of this simulator, imply endorsement of this package or indicate its superiority over other products.

It can be easily shown that the circuit of Fig. 5(a) realizes the relationship:

$$V_{3001} = \sqrt{\frac{I_L^2}{V_{C-A}^2}} = \left| \frac{I_L}{V_{C-A}} \right|. \tag{10}$$

Note that V_{3001} is forced to be a positive number by using the HSPICE limiter feature as shown in the Appendix. Hence, circuit (4a) produces positive roots only.

The circuit of Fig. 4(b) realizes the expression:

$$V_{4000} = \frac{|I_L|}{(D_{ON} + D_{OFF}^* |V_{C-A}|}. \tag{11}$$

The magnitude of V_{4004} (which is equal to D_{OFF}^*) is also forced to be a positive number using the HSPICE limiting option as shown in the Appendix.

The circuit of Fig. 4(c) realizes the limiter that clamps D_{OFF}^* to $1 - D_{ON}$ under CCM conditions, while the circuit of Figure 4(d) performs the calculation:

$$V_{7001} = \frac{D_{OFF}}{D_{ON} + D_{OFF}}. \tag{12}$$

The signals: V_{6003} and V_{7001}, can now be used as inputs to the basic switched inductor equivalent circuit of Fig. 2(b).

The HSPICE equivalent circuit for the USIM can be included in the simulator's library of components as a macro file of a three-port network.
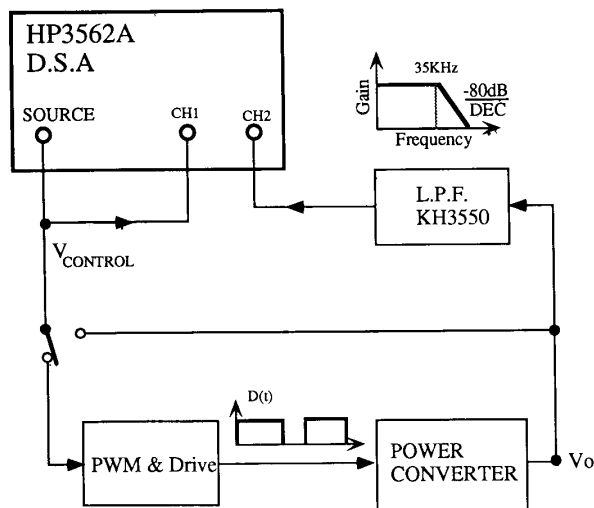
Fig. 5. Block diagram of setup for frequency response measurement by the HP3562A analyzer.

IV. APPLYING THE USIM

In this section, the flexibility and simplicity of applying the USIM in simulation, using HSPICE [15], is illustrated. We used HSPICE, but other simulation packages can obviously be applied.

To build the simulation program the following steps are suggested:

1) Define a three-port network subcircuit that describes the USIM, including the 'D_{OFF} generator,' as given in the Appendix. The subcircuit can be defined as a macro file and added to the library of components of the specific simulator used.

2) Identify the switched inductor configuration in the converter under study and replace it by the USIM.

3) The switching diodes and transistors can be replaced by their equivalent circuits in the saturation state (Fig. 1(a)–(c).)

4) Enter the converter's equivalent circuit, developed in steps 2 and 3, along with a nodal description of the rest of the circuit, as an input file to the simulator and perform the desired analyses.

A sample of HSPICE input files for buck, boost, and buck-boost converters are given in the Appendix. Observe that D_{ON} will be an independent voltage source for open-loop analysis, but an output of a controller circuit in closed-loop simulation. The controller operation could be based on voltage feedback or on current mode operation. The controllers equivalent circuit and closed-loop simulation are beyond the scope of this paper.

V. FREQUENCY RESPONSE MEASUREMENTS USING THE HP3562A DYNAMIC SIGNAL ANALYZER

The experimental data of this study was obtained by a fast and simple measurement technique using the HP3562A (Hewlett-Packard, Palo Alto CA) D.S.A. [14]. This measurement method overcomes the problems usually encountered when attempting to measure the fre-

quency responses of switch-mode converters, especially at the high frequency end where the switching ripple masks the forced perturbations.

The use of a dual-channel spectrum analyzer to measure switch mode systems was introduced in [16] and the references cited in it. We improved the experimental setup described in [16] by including a low pass filter that increases the signal to noise ratio by attenuating the switching ripple and noise. The HP3562A D.S.A. has extended capabilities and functions compared to the HP3582A described in [16]; the use of the HP3562A is simpler and more flexible. This flexibility is enhances by the fact that the analyzer can be interfaced to a computer system, a disk drive, or a plotter. Here we emphasize the setup and measurement method (rather than the detailed description of the D.S.A. functions as was done in [16]). Detailed description of HP3562A operation and capabilities can be found in its manual [14].

The operation of the HP3562A D.S.A. hinges on an FFT-based signal processing algorithm that is carried out on the sampled signals of its two channels (CH1 and CH2, Fig. 5). The frequency response of a system is measured by injecting at the input of the system under test, a test signal that has a flat spectrum over the frequency range of interest (1 kHz–10 kHz in our case), such as white noise or a sinusoidal chirp (the HP3562A includes internal random noise sources). From the input and output sampled sequences, the analyzer estimates the frequency response of the system. Linear averaging of any desired number of repeated measurements, which is also available on the HP3562A, can be applied to improve the accuracy of the estimated response.

The proposed setup for measuring the frequency response of switch mode converters is shown in Fig. 5. The low pass filter is used to attenuate the switching ripple which could causes erroneous FFT results, especially in the high frequency range. The corner frequency of the L.P.F. is chosen to be higher than half the switching frequency but lower than the switching frequency. The attenuation and phase shift of the L.P.F., in the useful frequency range, is corrected for by the following steps:

1) The frequency response of the L.P.F. is first measured and stored in the memory of the HP3562A.

2) The frequency response of the converter-L.P.F. assembly is measured and stored in the memory of the HP3562A.

3) The frequency response of the converter in series with the L.P.F. is divided by the frequency response of the L.P.F. using a built-in arithmetic function of the HP3562A. The result is the desired frequency response of the converter itself.

The HP3562A has been connected by us to computer systems (a PC and a VAX minicomputer) and to a plotter for easy manipulation of the measured responses.

VI. EXPERIMENTAL RESULTS

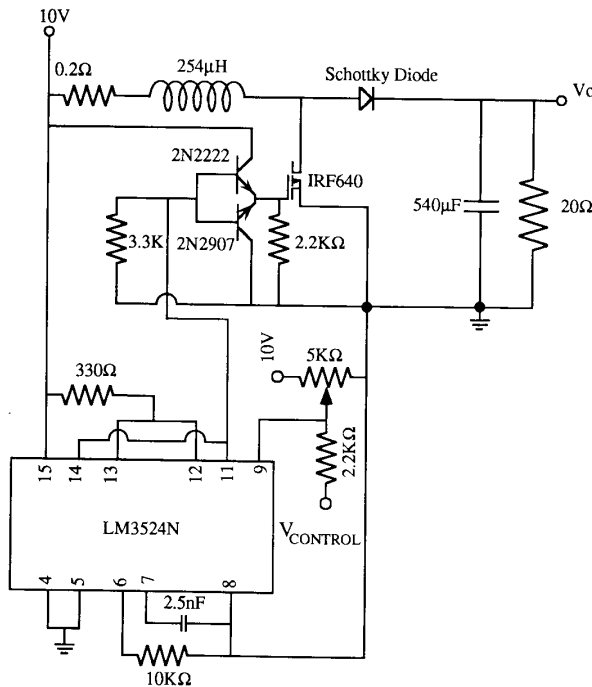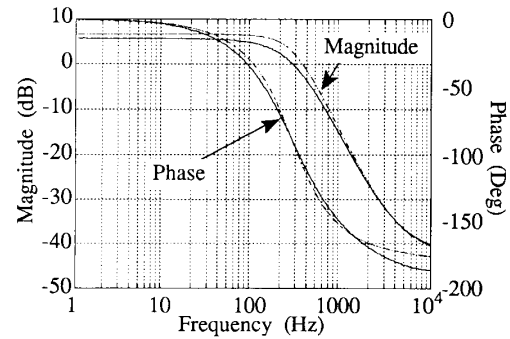The boost converter, described in Fig. 6 was used to test the USIM. The switching frequency (f_s) was 57.5 KHz.

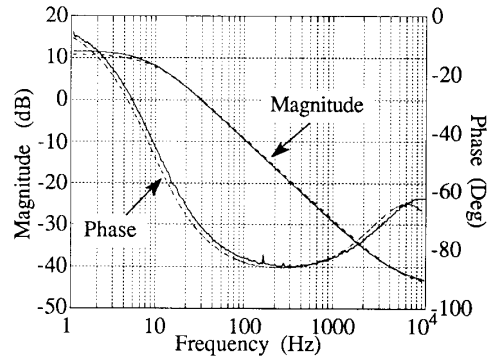Fig. 6. Boost converter circuit used in experimental study.

(a)

(b)

Fig. 7. Control-to-output frequency response of boost converter. Continuous lines: experimental data. Dashed lines: USIM simulation results. (a) CCM: $L = 254~\mu H$, $R_L = 0.4~\Omega$, $C = 516~\mu F$, $R_C = 0.07~\Omega$, $R_O = 20~\Omega$, $V_g = 10$ V. (b) DCM: $L = 48.5~\mu H$, $R_L = 0.1~\Omega$, $C = 516~\mu F$, $R_C = 0.07~\Omega$, $R_O = 97.5~\Omega$, $V_g = 10$ V.

The frequency responses of the boost converter were measured using the HP3562A analyzer for $D_{ON} = 0.4$ and for the DCM and the CCM. The measured responses were compared to the USIM simulations carried out by HSPICE on a VAX-8300/VMS (Digital Equipment Co.) computer. The experimental data and the simulation results (Fig. 7) were found to be in good agreement. The differences between the measured data and the HSPICE simulations are probably due to an inaccurate estimate of the values of the converter's components, especially the parasitic resistances. Also, the mesurement range of HP3562A was chosen to be 10 kHz and hence good precision is limited to the frequency range of 0–9 kHz.

The transient response for step changes of the load (R_o) between 117 and 20 Ω, which correspond to the DCM and the CCM respectively, were measured using the HP3562A and compared to USIM-based simulations. The results (Fig. 8) show that there is good agreement between experiment and simulation results. To illustrate the power of USIM over models that do not cover both the CCM and the DCM, the same transient was simulated under the (wrong) assumption that the converter operates only in the CCM. This simulation (Fig. 8) exhibits a large deviation (about 33%) from the measured value for the DCM period, as compared to an error of about (4–6%) when USIM is applied.

The turn-on transient of the boost converter (Fig. 1(b)) was simulated using both the USIM and 'exact' time domain simulation for a constant D_{ON} of 0.5. The results of the two simulations are in excellent agreement (Fig. 9).

VII. DISCUSSION AND CONCLUSION

The few simulation examples given here clearly demonstrate the power of the proposed USIM approach. Once the basic equivalent circuit of the switched inductor is constructed, large and small signal simulation becomes trivial. All that is required for simulating a given topology is the node connection and the values of the components. This simple procedure replaces the rather laborious task of deriving a canonical models for each case. Furthermore, the proposed procedure can provide in a simple and straightforward way the large signal response of a system that passes through both the DCM and the CCM.

The examples of Fig. 7 clearly show the fundamental difference in behavior between the CCM and the DCM. Whereas the CCM response is typical of a second-order system (Fig. 7(a)), the DCM response resembles a first-order system (Fig. 7(b)) with a maximum phase shift of 90°. Obviously, a feedback network that optimizes one mode of operation does not necessarily optimize the other. Furthermore, a reasonable phase-compensating network for one mode of operation can cause instability in the other. Hence, application of the proposed USIM can simplify and acclerate the design phase of switch mode systems.
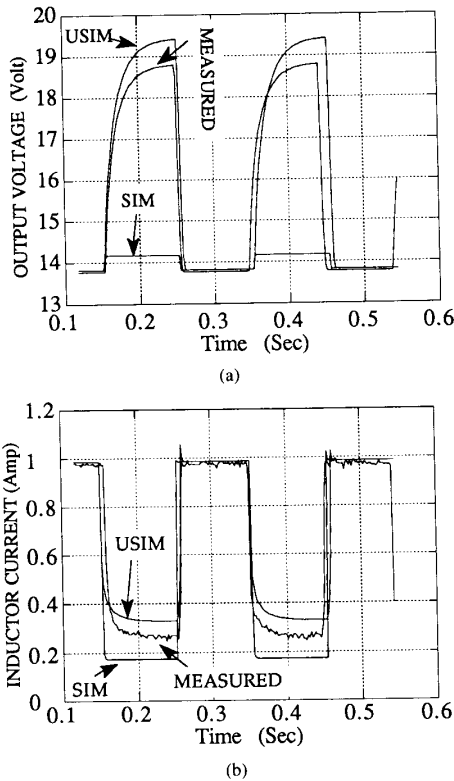
(a)

(b)

Fig. 8. Transient responses of a boost converter, $L = 48.5$ μH, $R_L = 0.1$ Ω, $C = 516$ μF, $R_C = 0.07$ Ω, $V_g = 10$ V, to load steps between 20-117 Ω.
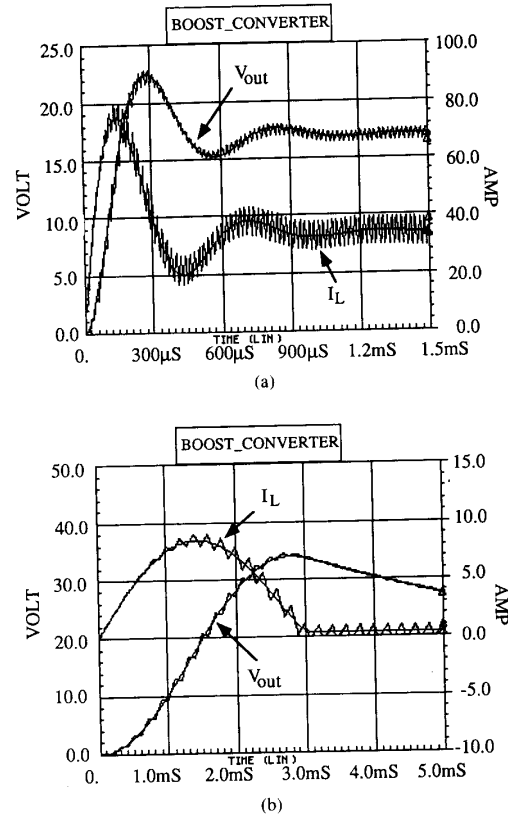

(a)

(b)

Fig. 9. Turn-on transient of a boost converter. Smooth line: USIM simulation. Rippled lines: time-domain simulation. Steady-state conditions: (a) CCM: $L = 10$ μH, $R_L = 0.001$ Ω, $C = 200$ μF, $R_C = 0.001$ Ω, $R_O = 1$ Ω, $V_g = 10$ V, $D_{ON} = 0.5$, $T_s = 20$ μS; (b) DCM: $L = 1000$ μH, $R_L = 0.01$ Ω, $C = 200$ μF, $R_C = 0.001$ Ω, $R_O = 40$ Ω, $V_g = 10$ V, $D_{ON} = 0.5$, $T_s = 200$ μS.

In the example of Fig. 8, the converter was designed to be in the DCM at low current and in the CCM when the current level is high. Consequently, when such a converter is subjected to a large decrease in load current, it will switch from the CCM to the DCM. If D_{ON} is kept constant, D_{OFF} will change and therefore the output voltage will increase (Fig. 8). The effect should be much smaller (only due to voltage drop on parasitic resistors) for a converter that is kept in CCM. In closed-loop configurations, D_{ON} will be obviously corrected by the feedback path. However, to simulate the actual closed-loop response, one has to consider the fact that the small signal responses of the CCM and the DCM operations are markedly different (Fig. 7). Hence, models that cannot switch automatically between the CCM and the DCM will not provide accurate information on the converter's behavior both for open- and closed-loop operation.

The examples of Fig. 9 demonstrate the ability of USIM simulation to cope with the large signal transients, associated with power turn-on, in which the converter might pass through both the CCM and the DCM (e.g., Fig. 9(b)). This time domain behavior can, in principle, be carried out by readily available simulators by emulating the actual switching action of the nonlinear portion of the converter. This is, in fact, how the time domain simula-

tions results, given in Fig. 9, were obtained. There is, however, a fundamental difference between this time domain simulation and the USIM-based large signal simulation. Whereas the 'exact' time domain simulation produces the actual signal wave forms within the switching period (see for, example, Fig. 9(b)), the USIM simulation follows the average values of the signals. Consequently, the numerical calculation for time domain simulation has to be carried out in much smaller steps than is necessary for the USIM simulation. The computer time saved, when applying the USIM, could be significant for long simulation runs. For the examples given here, the CPU time for the USIM simulations was smaller by a factor of five than the time required for the time domain simulation.

Application of the proposed model can simplify and ease the design of the phase compensating networks to obtain a desired dynamic behavior of the closed-loop system. Based on the simulated response, which is effortlessly obtained, the designer can introduce possible phase compensation schemes and test the overall, closed-loop performance by simulation. This numerical approach is in no way inferior to procedures that are based on analytical

expressions. The design of a feedback loop for a specific converter system must deal with the actual, numerical, response of the system under study. Hence, any design procedure must eventually converge to the responses that are obtained in a simple way by the proposed model and

simulation procedure. It is thus safe to predict that the proliferation of powerful workstations will eventually make interactive computer analysis and asimulation method, such as the one proposed here, the dominant design procedures.

<center>APPENDIX
EXAMPLE OF HSPICE INPUT FILES</center>

Note: Lines starting with asterisks are comments.

Switched_Power_Stage_Models

```
* This is a macro that represents the USIM
* As a three port network
.MACRO L&S_MODEL port_A   port_B   port_C   D_ON   GM
+
+            Lm = L   RLm = RL   Tm = T.

.PARAM   Am = '2*Lm/Tm'
Fport_B port_B port_A POLY(2) VLdemo VCdemo 0 1 −1
Fport_C port_C 1000 POLY(2) VLdemo VI_C 0 0 0 0 1
VCdemo 1000 port_A 0
E_B_A_D_ON 2001 2000 POLY(2) port_B port_A D_ON GM 0 0 0 0 1
E_C_A_Dof 2000 GM POLY(2) port_C port_A D_OFF GM 0 0 0 0 1
VLdemo 2001 2002 0
RL 2002 2003 RLm
L 2003 GM Lm

* This part of the circuit is the D_OFF generator
* D_OFF = [(2L/T)*{IL/[(D_ON + D_OFF)Vca]}
E3000 3000 GM POLY(1) port_C port_A MIN=0.1 0 0 1
E3001 3001 GM 3002 GM MIN= 1E-8 1
R3001 3001 GM 100K
H3002 3002 3003 POLY(1) VLdemo 0 0 1
E3003 GM 3003 POLY(2) 3001 GM 3000 GM 0 −1 0 0 0 0 1
E4000 4000 GM 4001 GM MIN=1E-8 1
E4001 4001 4002 3001 GM 1
E4002 GM 4002 POLY(2) 4000 GM 4003 GM 0 −1 0 0 1
E4003 4003 GM POLY(2) 4004 GM D_ON GM 0 1 1
E4004 4004 GM 4000 GM Am
* V(4004)  =D_OFF

* Clamping D_OFF to 1−D_ON
E6000 6000 GM POLY(1) D_ON GM 100  −100
E6002 6002 GM 4004 GM 100
R6002 6002 6003 2K
D6003 6003 6000 D1N
.Model D1N D(IS=100E-15 RS=0.01 IBV=1E-16)
ED_OFF D_OFF GM 6003 GM 0.01
RD_OFF D_OFF GM 100K

* Calculating D_OFF/(D_ON + D_OFF)
E7000 7000 GM POLY(2) D_OFF GM D_ON GM 0 1 1
E7001 7001 GM 7002 GM MIN=1E-3 1
R7001 7001 7004 1
VI_C 7004 GM 0
E7002 7002 7003 D_OFF GM 1
E7003 GM 7003 POLY(2) 7001 GM 7000 GM 0 −1 0 0 1
```

```
* I(VI_C) = D_OFF/(D_ON + D_OFF)
.EOM
*End of the Macro File

* Sample Input Files for Various Topologies
* To simulate one of the the converters (buck, boost, buck-boost),
    remove the ($) sign from the beginning of the lines of the desired topology

VIN 1 0 Vg

$RTR TR 1 0.01
$XBUCK OUT 1 Diodp D_ONP 0 L&S_MODEL Lm=L RLm=RL Tm=T
$D1 0 Diodp DNN

$XBOOST 1 TR Diodp D_ONP 0 L&S_MODEL Lm=L RLm=RL Tm=T
$RTR TR 0 0.01
$D1 Diodp OUT DNN

$RTR TR 1 0.01
$XBUCKBOOST 0 TR Diodp D_ONP 0 L&S_MODEL Lm=L RLm=RL Tm=T
$D1 Diodp OUT DNN

RCC 6 OUT RC
C1 6 0 Cout IC=0.1
R1 OUT 0 Rout

*Independent generator for generating D_ON (for open loop simulation)
VD_ONP D_ONp 0 AC 1 DC D_ON
RD_ONP D_ONp 0 10K
.MODEL DNN D (IS=100E-15 RS=0.1 IBV=1E-16)

* To avoid convergence problems in dc and ac analysis, estimate the
* steady-state D_OFF manually or by running a transient analysis, and specify the
* estimated value of D_OFF in the .PARAM line below. This value will be used
* by theinitial conditions command .NODSET given below to help the
* numerical calculation to converge in dc and ac analysis.

*The values used in this Study:
.PARAM D_OFF=0.48 A='2*L/T'
.NODESET V(1:D_OFF)=D_OFF V(1:3001)='D_OFF*(D_OFF+D_ON)/A'
+V(1:4000)='D_OFF/A' V(1:7001)='D_OFF/(D_ON+D_OFF)' V(OUT)='Vg/D_OFF'

*Circuit parameters of this study
.PARAM Vg =10 D_ON=0.52 Rout=20 Cout = 516U L=254U T=17.5U
+RL=.6 RC=.02

*Analysis options
.TRAN 20E-6 45E-3 UIC
.AC DEC 80 1 10K
. PZ V(OUT) VD_ONp

* HSPICE output command
.OPT POST
.END
```

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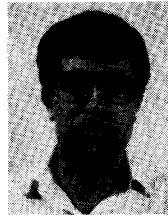
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