Product Brief
Rev 0, 10/2004

ACT30

ACT30 HIGH PERFORMANCE OFF-LINE CONTROLLER
ActiveSwitcher™ IC Family

FEATURES

- Lowest Total Cost Solution
- 0.15W Standby Power
- Emitter Drive Allows Safe NPN Flyback Use
- Hiccup Mode Short Circuit
- Current Mode Operation
- Over-Current Protection
- Under-voltage Protection with Auto-restart
- Proprietary Scalable Output Driver
- Flexible Packaging Options (including TO-92)
- 6-Terminal Die Available
- 65kHz or 100kHz Switching Frequency
- Selectable 0.4A to 1.2A Current Limit

APPLICATIONS

- Battery Chargers
- Power Adaptors
- Standby Power Supplies
- Appliances
- Universal Off-line Power Supplies

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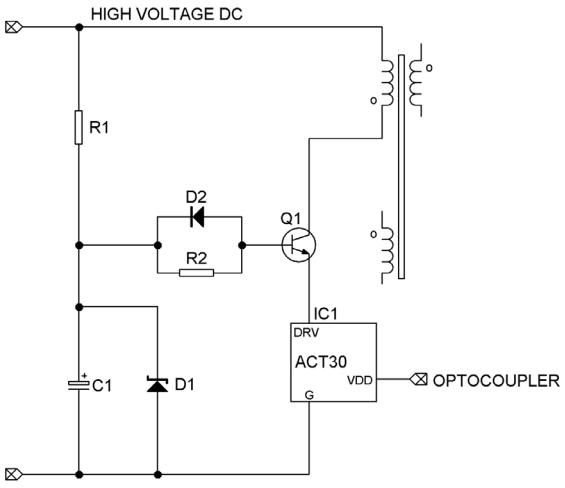


Figure 1. Simplified Application Circuit

GENERAL DESCRIPTION

OUTPUT POWER CAPABILITY				
DEVICE	230VAC ± 15%		85-265VAC	
	OPEN FRAME	ADAP-TOR	OPEN FRAME	ADAP-TOR
ACT30A	TBDW	TBDW	TBDW	TBDW
ACT30B	TBDW	TBDW	TBDW	TBDW
ACT30C	TBDW	TBDW	TBDW	TBDW
ACT30D	TBDW	TBDW	TBDW	TBDW
ACT30E	TBDW	TBDW	TBDW	TBDW

The ACT30 is a high performance green-energy offline power supply controller. It features a scalable driver for driving external NPN or MOSFET transistors for line voltage switching. This proprietary architecture enables many advanced features to be integrated into a small package (TO-92 or SOT23-5), resulting in lowest total cost solution.

The ACT30 is a 6-terminal medium-voltage pulse frequency and width modulation IC with many flexible packaging options for generating power to more than 10W. One combination of internal terminals is packaged in the space-saving TO-92 package (A/B/C/D versions) for 65kHz or 100kHz switching frequency and with 400mA or 800mA current limit. The E version (SOT23-5, DIP-8 or Die) can be configured for up to 1.2A current limit.

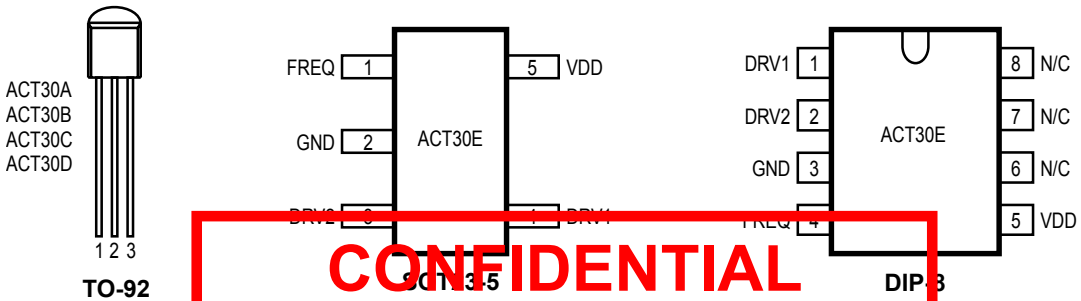
Consuming only 0.15W in standby, the IC features over-current, hiccup mode short circuit, and under-voltage protection mechanisms.

The ACT30 is ideal for use in high performance universal adaptors and chargers. For highest performance versus cost and smallest PCB area, use the ACT30 in combination with the ACT32 CV/CC Controller.

ORDERING INFORMATION

PART NUMBER	SWITCHING FREQUENCY	CURRENT LIMIT	TEMPERATURE RANGE	PACKAGE	PINS
ACT30AHT	65kHz	400mA	-40°C to 85°C	TO-92	3
ACT30BHT	65kHz	800mA	-40°C to 85°C	TO-92	3
ACT30CHT	100kHz	400mA	-40°C to 85°C	TO-92	3
ACT30DHT	100kHz	800mA	-40°C to 85°C	TO-92	3
ACT30EUC-T	SELECTABLE	ADJUSTABLE	-40°C to 85°C	SOT23-5	5
ACT30EDH	SELECTABLE	ADJUSTABLE	-40°C to 85°C	DIP-8	8
ACT30EZZ	SELECTABLE	ADJUSTABLE	-40°C to 85°C	DIE	6

PIN CONFIGURATION



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PIN DESCRIPTION

PIN NUMBER			PIN NAME	PIN DESCRIPTION
TO-92	SOT23-5	DIP-8		
1	5	5	VDD	Power Supply Pin. Connect to optocoupler's emitter. Internally limited to 5.5V max. Bypass to GND with a proper compensation network.
2	2	3	GND	Ground
3			DRV	Driver Output. Connect to emitter of the high voltage NPN or MOSFET. For ACT30A/C, DRV pin is connected to DRV1 only. For ACT30B/D, DRV pin is connected to both DRV1 and DRV2.
	4	1	DRV1	Driver Output 1. Also used as supply input during startup.
	3	2	DRV2	Driver Output 2. For TO-92, this terminal is internally wire-bonded to DRV1 for B and D versions, and left unconnected for A and C versions. For E version, this pin can be arranged with DRV1 to set current limit at any value between 400mA and 1.2A.
	1	4	FREQ	Frequency Select. This terminal has an internal 200kΩ pull down resistor. Connect to VDD for 100kHz operation. Connect to GND or leave unconnected for 65khz operation. For TO-92 ACTA/B versions, this terminal is N/C. For ACT30C/D versions, this terminal is internally wire-bonded to VDD.

ABSOLUTE MAXIMUM RATINGS

(Note: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

PARAMETER		VALUE	UNIT
VDD, FREQ Pin Voltage		-0.3 to 6	V
VDD Current		20	mA
DRV, DRV1, DRV2 Voltage		-0.3 to 18	V
Continuous DRV, DRV1, DRV2 Current		Internally limited	A
Maximum Power Dissipation	TO-92	TBD	W
	SOT23-5	TBD	
	DIP-8	TBD	
Operating Junction Temperature		-40 to 150	°C
Storage Temperature		-55 to 150	°C
Lead Temperature (Soldering, 10 sec)		300	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 4V, T_J = 25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD} Start Voltage	V_{START}	Rising edge		4.75	5	5.25	V
DRV1 Start Voltage	V_{DRVST}	DRV1 must be higher than this voltage to start up.			10.6	10.5	V
DRV1 Short-Circuit Detect Threshold	V_{SCDRV}				1.8		V
V_{DD} Under-voltage Threshold	V_{UV}	Falling edge		3.17	3.35	3.53	V
V_{DD} Clamp Voltage		10mA		5.15	5.45	5.75	V
Startup Supply Current	I_{DDST}	V_{DD} = 4V before V_{UV}			0.23	0.45	mA
Supply Current	I_{DD}				0.7	1	mA
Switching Frequency	f_{SW}	ACT30A/B or FREQ = 0		55	65	85	kHz
		ACT30C/D or FREQ = V_{DD}		75	100	125	
Maximum Duty Cycle	D_{MAX}	V_{DD} = 4V		67	75	83	%
Minimum Duty Cycle	D_{MIN}	V_{DD} = 4.6V			3.5		%
Effective Current Limit	I_{LIM}	V_{DD} = V_{UV} + 0.1V	ACT30A/C		400		mA
			ACT30B/D; ACT30E with DRV1 = DRV2		800		
V_{DD} to DRV1 Current Coefficient	G_{GAIN}				-0.29		A/V
VDD Dynamic Impedance	R_{VDD}				9		kΩ
Driver Output 1 On-Resistance	R_{DRV1}	I_{DRV1} = 0.05A			3.6		Ω
Driver Output 2 On-Resistance	R_{DRV2}	I_{DRV2} = 0.05A			3.6		Ω
DRV1 Rise Time		1nF load, 15Ω pull-up			30		ns
DRV1 Fall Time		1nF load, 15Ω pull-up			20		ns
DRV1 and DRV2 Switch Off Current		Driver off, V_{DRV1} = V_{DRV2} = 10V			12	30	µA

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FUNCTIONAL DESCRIPTION

Figure 2 shows the *Functional Block Diagram* of the ACT30. The main components include switching control logic, two on-chip medium-voltage power-MOSFETs with parallel current sensor, driver, oscillator and ramp generator, current limit VC generator, error comparator, hiccup control, bias and undervoltage-lockout, and regulator circuitry.

As seen in Figure 2, there are 4 non-GND terminals. VDD is power supply terminal. DRV1 and DRV2 are linear driver outputs that can drive the emitter of an external high voltage NPN transistor or N-channel MOSFET. This emitter-drive method takes advantage of the high V_{CBO} of the transitor, allowing a low cost transistor such as '13003 (V_{CBO} = 700V) or '13002 (V_{CBO} = 600V) to be used for a wide AC input range. The slew-rate limited driver coupled with the turn-off characteristics of an external NPN result in lower EMI. (See *External Power Transistor* in *Application Information* section) Finally, FREQ terminal is for frequency selection.

The driver peak current is designed to have a negative voltage coefficient with respect to supply voltage V_{DD}, so that lower supply voltage automatically results in higher DRV1 peak current. This way, the optocoupler can control V_{DD} directly to affect driver current.

STARTUP SEQUENCE

Figure 1 shows a *Simplified Application Circuit* for the ACT30. Initially, the small current through resistor R1 charges up the capacitor C1, and the BJT acts as a follower to bring up the DRV1 voltage. An internal regulator generates a V_{DD} voltage equal V_{DRV1} – 3.6V but limits it to 5.5V max. As V_{DRV1} increases pass 8.6V (and V_{DD} reaches 5V), the regulator sourcing function stops and V_{DD} begins to drop due to its current consumption. As V_{DD} voltage decreases below 4.75V, the IC starts to operate with increasing driver current. When the output voltage reaches regulation point, the optocoupler feedback circuit stops V_{DD} from decreasing further. The switching action also allows the auxiliary windings to take over in supplying the C1 capacitor. Figure 3 shows a typical startup sequence for the ACT30.

Even though up to 2MΩ startup resistor (R1) can be used due to the very low startup current, actual R1 value should be chosen as a compromise between standby power and startup time delay.

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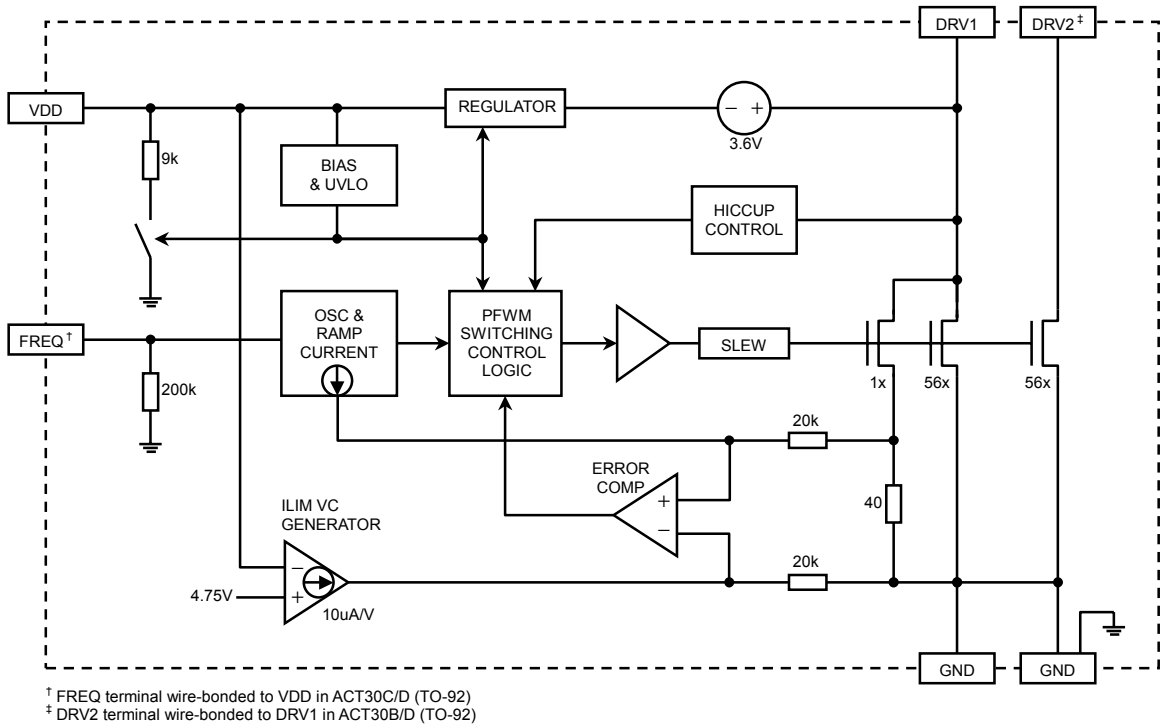

† FREQ terminal wire-bonded to VDD in ACT30C/D (TO-92)
‡ DRV2 terminal wire-bonded to DRV1 in ACT30B/D (TO-92)

Figure 2. Functional Block Diagram

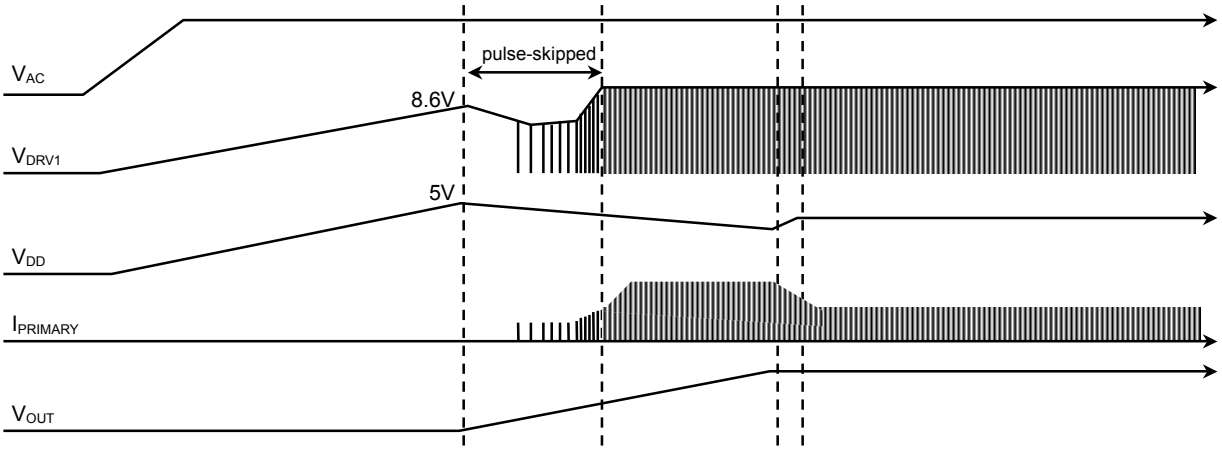

Figure 3. Startup Waveforms

NORMAL OPERATION

In normal operation, the feedback signal from the secondary side is transmitted through the optocoupler as a current signal into VDD pin, which has dynamic impedance of 9kΩ. The resulting V_{DD} voltage affects the switching of the IC. As seen from the *Functional Block Diagram*, the Current Limit VCO Generator uses the V_{DD} voltage difference with 4.75V to generate a proportional offset at the negative input of the Error Comparator.

The drivers turn on at the beginning of each switching cycle. The current sense resistor current, which is a fraction of the transformer primary current, increases with time as the primary current increases. When the voltage accross this current sense resistor plus the oscillator ramp signal equals Error Comparator's negative input voltage, the drivers turn off. Thus, the peak DRV1 current has a negative voltage coefficent of -0.29A/V and can be calculated from the following:

$I_{DRV1PEAK} = 0.29A/V \bullet (4.75V - V_{DD})$

for V_{DD} < 4.75V and duty cycle < 50%.

When the output voltage is lower than regulation, the current into VDD pin is zero and V_{DD} voltage decreases. At $V_{DD} = V_{UV} = 3.35V$, the peak DRV1 current has maximum value of 400mA.

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CURRENT LIMIT ADJUSTMENT

The IC's proprietary driver arrangement allows the current limit to be easily adjusted between 400mA and 1.2A. To understand this, the drivers have to be utilized as linear resistive devices with typically 3.6Ω (rather than as digital output switches). The current limit can then be calculated through linear combination as shown in Figure 4. For TO-92 package, the ACT30A/C are preprogrammed to 400mA current limit and

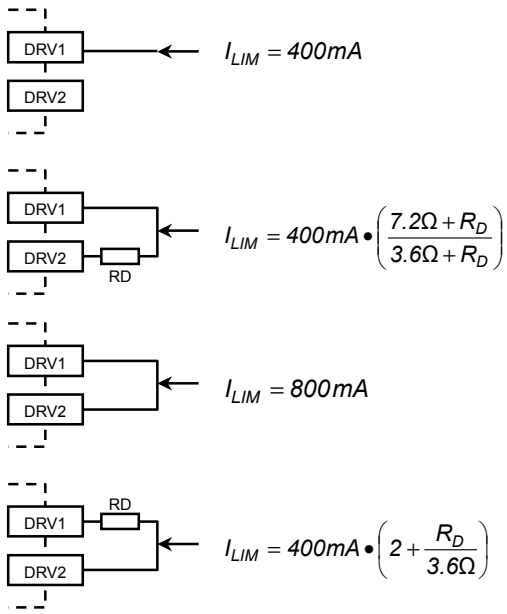

Figure 4. Driver Output Configurations

the ACT30B/D are preprogrammed to 800mA current limit. For ACT30E (SOT23-5 or DIP-8) packages, both DRV1 and DRV2 terminals are provided.

PULSE SKIPPING

The PFWM Switching Control Logic block operates in different modes depending on the output load current level. At light load, the V_{DD} voltage is around 4.75V. The energy delivered by each switching cycle (with minimum on time of 500ns) to the output causes V_{DD} to increase slightly above 4.75V. The FPWM Switching Control Logic block is able to detect this condition and prevents the IC from switching until V_{DD} is below 4.75V again. This results in a pulse-skipping action with fixed pulse width and varying frequency, and low power consumption because the switching frequency is reduced. Typical system standby power consumption is 0.15W.

SHORT CIRCUIT HICCUP

When the output is short circuited, the ACT30 enters hiccup mode operation. In this condition, the auxiliary supply voltage collapses. An on-chip detector compares DRV1 voltage during the off-time of each cycle to 6.8V. If DRV1 voltage is below 6.8V, the IC will not start the next cycle, causing both the auxiliary supply voltage and V_{DD} to reduce further. The circuit enters startup mode when V_{DD} drops below 3.35V. This hiccup behaviour continues until the short circuit is removed. In this behavior, the effective duty cycle is very low resulting in very low short circuit current.

To make sure that the IC enters hiccup mode easily, the transformer should be constructed so that there is close coupling between secondary and auxiliary, so that the auxiliary voltage is low when the output is short-circuited. This can be achieved with the primary/auxiliary/secondary sequencing from the bobbin. Refer to *Design Guide* section of this datasheet for optimal transformer construction techniques.

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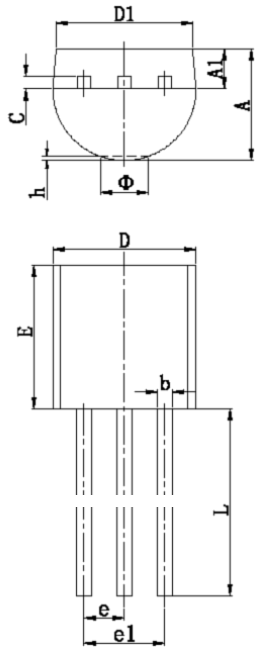
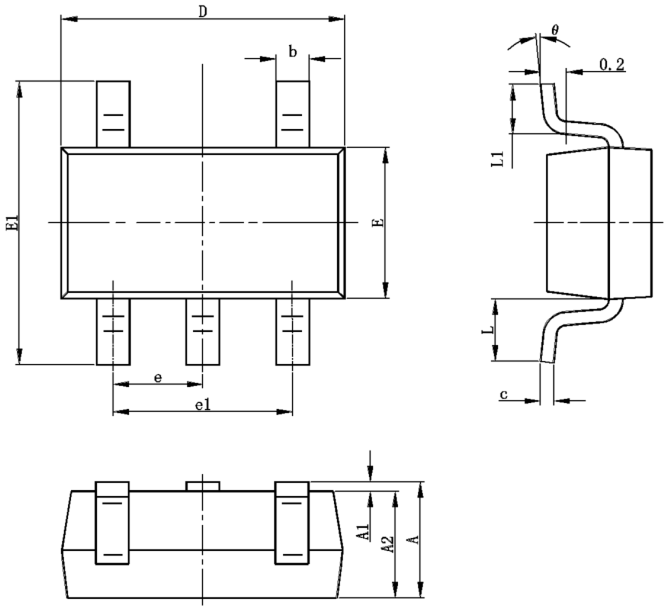
PACKAGE OUTLINE

TO-92 PACKAGE OUTLINE AND DIMENSIONS



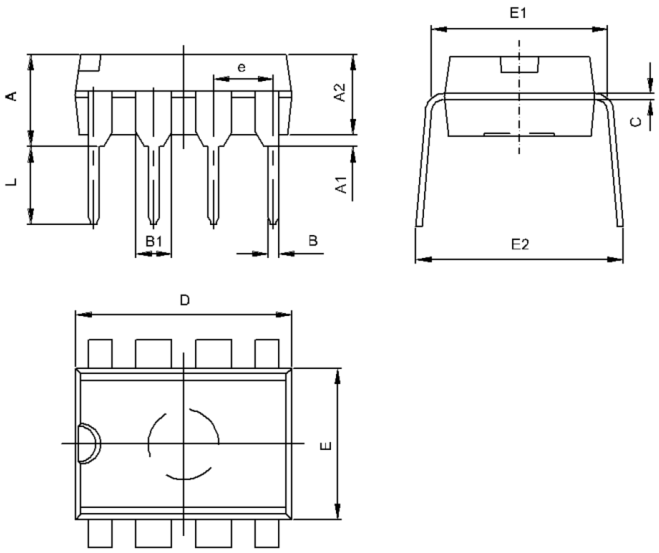
SYMBOL	DIMENSION IN MILIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	3.300	3.700	0.130	0.146
A1	1.100	1.400	0.043	0.055
b	0.380	0.550	0.015	0.022
c	0.360	0.510	0.014	0.020
D	4.400	4.700	0.173	0.185
D1	3.430		0.135	
E	4.300	4.700	0.169	0.185
e	1.270 TYP		0.050 TYP	
e1	2.440	2.640	0.096	0.104
L	14.100	14.500	0.555	0.571
Φ		1.600		0.063
h	0.000	0.380	0.000	0.015

SOT23-5 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.700 REF		0.028 REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

DIP-8 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.360	0.560	0.014	0.022
B1	1.524 TYP		0.060 TYP	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.620 TYP		0.300 TYP	
e	2.540 TYP		0.100 TYP	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370

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