VESA®

Video Digital Flat Panel Standard

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VESA Digital Flat Panel (DFP)

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Purpose

The purpose of this standard is to provide for an interface between a personal computer and a digital flat panel monitor. The Digital Flat Panel (DFP) interface allows a host computer to connect directly to an external digital flat panel monitor over several meters of cable without the need for analog-to-digital conversion. This interface makes use of existing VESA standards to allow for the implementation as a simple low-cost industry standard. This includes the graphics controller interface functions to support the digital video data, configuration management, and power management. As the standard embraces only the essential components necessary for digital display monitor functions, it enables a simple and low-cost implementation in both the host and monitor.

Summary

The Digital Flat Panel (DFP) Standard is based largly on the existing P&D standard. Transmisison Minimized Differential Signaling (TMDS) is used to transport the digital video to the monitor. DDC and EDID Standards are supported for configuration management. To insure compatibility with the P&D standard, a pin is reserved for Hot Plug Detection support. For simplicity, no other electrical interfaces are supported in this standard. The physical interface part of this standard is based on the MDR20 connector.

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VESA DIGITAL FLAT PANEL (DFP) STANDARD

The DFP Standard is the result of expert input from many sources. VESA acknowledges and thanks the DFP Workgroup members who contributed to and combined the industry expertise that resulted in this standard.

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Digital Flat Panel (DFP) Standard

1. INTRODUCTION

The purpose of this standard is to provide for an interface between a personal computer and a digital flat panel monitor. The Digital Flat Panel (DFP) interface allows a host computer to connect directly to an external digital flat panel monitor over several meters of cable without the need for analog-to-digital conversion.

This interface makes use of existing VESA standards to allow for the implementation as a simple low-cost industry standard. This includes the graphics controller interface functions to support the digital video data, configuration management, and power management. As the standard embraces only the essential components necessary for digital display monitor functions, it enables a simple and low-cost implementation in both the host and monitor.

1.1. DFP OVERVIEW

Noted below are several key features and advantages for the DFP system. While a subset of these features may be allowed on the monitor, all features are mandatory for the host system.

- TMDS digital interface capable of driving up to 5 meters of cable.
- Support for a large variety of flat panel monitors, including DSTN and TFT using a 24-bit TFT interface.
- DDC2B and EDID support for display detection and configuration.

1.2. COMPATIBILITY WITH VESA STANDARDS

1.2.1. VESA Plug and Play (P&D) Standard

The electrical interface of the DFP Standard is compatible with the VESA P&D Standard Version 1.0. This document refers to several sections of the P&D Standard for the electrical specifications.

1.2.2. VESA Display Data Channel (DDC) Standard

This standard incorporates the Display Data Channel for operation between a DDC compliant host and DDC compliant monitor. The DDC level supported in this specification is DDC2B only. Compatibility with earlier DDC versions is not supported.

1.2.3. VESA Extended Display Identification Data (EDID) Standard

This standard depends upon the support of EDID for the identification of the display by the host. Information about EDID structures 1.1, 1.2, and 2.0 can be found in version 3.0 of the VESA EDID Standard.

2. HOST AND MONITOR COMPATIBILITY

The DFP system is designed in such a way to ensure the highest level of compatibility between a DFP compliant host and monitor. Several key features are instituted within the physical and logical layers to allow operation between monitors with a wide range of performance characteristics to any DFP compliant host. The details of these features will be covered in subsequent sections. The primary system features to accomplish this goal are as follows:

1. The host will provide support ONLY for the "TFT" data mapping (one pixel per clock, up to 8 bits per channel, MSB-justified) as defined in the VESA Plug & Display standard. Support for the other data mappings (e.g., the STN and DSTN mappings) WILL NOT be provided by hosts complying with this implementation standard.
2. The DFP system must support the VESA DDC and EDID standards for identifying the display and its capabilities. The host is expected to automatically configure the appropriate video interface based on the information obtained from this channel. Information about EDID structures 1.1, 1.2, and 2.0 can be found in version 3.0 of the VESA EDID Standard.
3. All DFP compliant monitors (except those bundled with a video card or host that support scaling or centering) must support the resolutions 640x400, 720x400, and 640x480 to insure the minimum level of interoperability. The DFP compliant monitor must produce a viewable image (so that all pixels are viewable to the end user) with any of these resolutions.

3. HOST AND MONITOR COMPATIBILITY

3.1. SYSTEM OVERVIEW

The DFP architecture is comprised of several logical and physical components necessary to define the complete set of features shared between the host and monitor.

3.2. DFP ELECTRICAL AND LOGICAL INTERFACES

The DFP interface is comprised of 2 electrical layer components: a TMDS interface for low-voltage differential serial encoding of the digital display data and a DDC2B electrical interface that can be shared with the standard 15 pin DDC2B compliant VGA connector (if present). The following table defines the minimal requirements for a DFP compliant host and monitor:

Electrical Layer	DFP Host	DFP Monitor
TMDS	3 channel TMDS transmitter, single pixel 24 bit MSB-aligned RGB TFT	3 channel TMDS receiver, single pixel 24 bit MSB-aligned RGB TFT
DDC	DDC2B	DDC2B
Logical Layer		
EDID	EDID Structure 1.2	EDID Structure 1.2
DDC	DDC version 3.0 host functions	DDC version 3.0 monitor

Table 3-1. Electrical and Logical Interface Requirements for a DFP System

3.3. DFP CONNECTOR

The following diagram depicts the physical connector and associated pin assignment. This connector is categorized as a 20 pin mini-D ribbon (MDR) type receptacle. Table 3-2 contains the functional description for each pin.

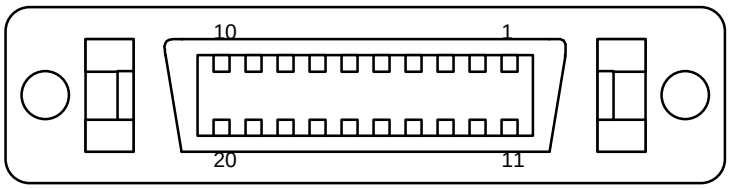


Figure 3-1. DFP Host Receptacle Connector

Pin #	Signal Name	Description	Pin #	Signal Name	Description
1	TX1+	TMDS positive differential output, channel 1	11	TX2+	TMDS positive differential output, channel 2
2	TX1-	TMDS negative differential output, channel 1	12	TX2-	TMDS negative differential output, channel 2
3	SHLD1	Shield for TMDS channel 1	13	SHLD2	Shield for TMDS channel 2
4	SHLDC	Shield for TMDS clock	14	SHLD0	Shield for TMDS channel 0
5	TXC+	TMDS positive differential output, reference clock.	15	TX0+	TMDS positive differential output, channel 0
6	TXC-	TMDS negative differential output, reference clock.	16	TX0-	TMDS negative differential output, channel 0
7	GND	Logic Ground	17	No Connect 17	No Connection
8	+5V	Logic +5V DC Supply from the Host	18	HPD	Hot Plug Detection (+5V DC to Host)
9	No Connect 9	No Connection	19	DDC_DAT	DDC2B Data
10	No Connect 10	No Connection	20	DDC_CLK	DDC2B Clock

Table 3-2. DFP Connector Pin Assignment and Description

3.4. DISPLAY POWER MANAGEMENT

The monitor is only required to support a single low-power mode.

For support of a single low-power mode, the monitor will use the activity of the digital video interface to determine its power state. If the TMDS interface is active, the monitor shall be On. If the TMDS interface is not active or any of the signals are out of range, the monitor shall be Off. A monitor using this method of power management would only report the support of Active-Off in the EDID data.

The host is required to deactivate the digital video interface for all low-power modes when the monitor EDID data indicates that only Active-Off is supported. If the monitor indicates the support of other low-power modes, the host will not deactivate the digital video interface for these modes.

3.5. DISPLAY SAFEGUARDS

The monitor must provide for a basic means to safeguard for invalid conditions that may corrupt or damage the flat panel device. Listed below are conditions that the monitor must respond to such that no corrupt data is visible on the screen or temporary/permanent damage is done to the monitor circuitry:

1. Invalid or loss of any TMDS signal.
2. Unsupported resolutions and refresh rates (as best can be determined by H and V sync).

3.6. HOT PLUG DETECTION

Pin 18 of the MDR20 connector is to be used for the support of Hot Plug Detection. Hot Plug Detection allows the host to detect when a monitor is attached or detached. Hot Plug Detection support is required for the DFP monitor and optional for the host.

For Hot Plug Detection in the monitor, pin 18 is required to be connected internally to pin 8 (+5V DC source from the host). This configuration allows the monitor to be detected when it is not powered. Note that PC98 requires the monitor to provide EDID data to the host when the monitor is not powered.

If Hot Plug Detection is supported on the host, pin 18 will be monitored and the host will read the EDID data if the voltage transitions to greater than 2.0V. If the voltage on pin 18 drops below 2 V, the host will disable the TMDS transmitter.

Refer to the VESA P&D Standard V1.0 for more information on the operation of Hot Plug Detection.

Note that the P&D Standard defines optional Charge Power support on the Hot Plug Detection line. As a result, a P&D monitor may source up to 20 V on this pin. To insure compatibility with a P&D monitor, it is required that the DFP host be tolerant of a 20 V input on pin 18. If the host does not support Hot Plug Detection, pin 18 shall not be connected.

3.7. REQUIREMENTS FOR LOWER RESOLUTION SUPPORT

In order to insure the minimum level of interoperability between a DFP compliant monitor and host, both the monitor and host must support the video modes 640x400-60Hz, 720x400-60Hz, and 640x480-60Hz. The DFP monitor must produce a viewable image with all of these video modes. The pixel clock for 640x400 and 720x400 shall be scaled down so the refresh rate is adjusted from 70 Hz to 60 Hz.

The definition of a viewable image is all pixels are visible to the end user. Note that this does not mean that the monitor must support scaling or centering. It is considered acceptable for the image to be displayed in the upper left corner of the LCD. Monitors that have a native resolution of 640x480 are not required to fully display 720x400.

If a DFP monitor is bundled with a DFP host or video card that does support scaling or centering, the monitor may rely on the host and is not required to provide this lower resolution support.

3.8. SCALING ARBITRATION

If both the host and monitor support scaling, the host must decide which scaler will be used.

The following is a list of requirements for scaling arbitration:

1. If a digital monitor states support of more than one resolution in EDID, the host shall assume the monitor supports scaling or centering.
2. If both the host and monitor support scaling, the host shall default to monitor scaling. Note this requirement only defines the default state and does not prevent the host from scaling.
3. The monitor shall only list the video modes in EDID that are supported with a quality image (centering or scaling).
4. The host shall assume the resolution listed in the first detailed timing block is the native resolution of the monitor.
5. The host shall assume the monitor only provides minimal support of the video modes 640x400-60Hz, 720x400-60Hz, and 640x480-60Hz if these modes are not listed in EDID.

3.9. MONITOR CONFIGURATION

To insure compatibility between a DFP host and monitor, the following restrictions are placed on the DFP monitor:

1. Data Enable (DE) shall be active high
2. H and V syncs shall be active high
3. The Digital Interface Data Format shall be 24-bit MSB-aligned RGB TFT

3.10. EDID SUPPORT

DFP hosts and monitors are required to support EDID structure 1.2.

In addition to the support of EDID structure 1.2, it is also recommended that the host and monitor support EDID structure 2.0 to insure compatibility with P&D hosts and monitors.

If the DFP monitor only supports EDID 1.X (1.1, 1.2, etc.) without extensions, the host will make the following assumptions:

1. 24-bit MSB-aligned RGB TFT
2. DE polarity is active high
3. H and V syncs are active high
4. Established CRT timings will be used
5. Dithering will not be enabled on the host

3.11. HOST +5V SUPPLY

The DFP host is required to source +5V on pin 8 of the DFP connector. The specifications for this source are the same as those defined in the VESA DDC Standard V3.0 (+5V +/- 5%, 50 mA minimum, 1.0 A maximum).

4. ELECTRICAL SPECIFICATIONS

4.1. TMDS SPECIFICATIONS

The DFP Standard uses the Transition Minimized Differential Signaling (TMDS) interface standard developed by Silicon Image. This interface transmits the video digitally to the monitor using 4 differential pairs. Refer to Chapter 5 (Electrical Layer Specification: Digital (TMDS) Video Transmission Overview) and Chapter 6 (Electrical Layer Specifications: TMDS Transmission Specifications) of the VESA Plug and Display (P&D) Standard V1.0 for more information about the electrical interface. At the time of release of the DFP Standard, a separate TMDS Standard was under development that included the contents of Chapters 5 and 6 of the P&D Standard.

The TMDS encoding information is not part of the VESA P&D Standard and must be licensed from Silicon Image. Contact Silicon Image for more information.

4.2. DDC2B ELECTRICAL SPECIFICATIONS

The DDC/EDID interface is used by the host to identify the monitor. Refer to the VESA DDC V3.0 and EDID V3.0 standards for more information.

5. MECHANICAL PHYSICAL LAYER: CONNECTOR

5.1 INTRODUCTION

The DFP connector is a two row shielded ribbon contact connector with contacts on .050" spacing. A 360° "Delta" shaped metal shell encloses the plug and receptacle contacts to provide EMI shielding and proper polarity when mated.

The following is a list of the known DFP compatible connectors at the time of the release of this standard.

1. 3M – Mini Delta Ribbon (MDR) Connector .050" series
   a. Receptacle : P/N 10220-55G3 VC or 10220-55H3 VC
   b. Plug: P/N 10120-6000 EC

2. AMP –
   a. Receptacle: P/N 917738-2
   b. Plug: P/N 2-175677-2

3. Molex –
   a. Receptacle: P/N 52515-2011
   b. Plug: P/N 52316-2011

NOTE: Contact connector manufacturer for compatible junction shells and panel mounting screws as required by the specific application.

5.2 MECHANICAL DRAWINGS

Figure 5.1 provides the features and dimensions of a DFP thru-hole board mount receptacle. This information is intended to aid the designer of the PCB layout when considering proper body clearance dimensions for a DFP receptacle.

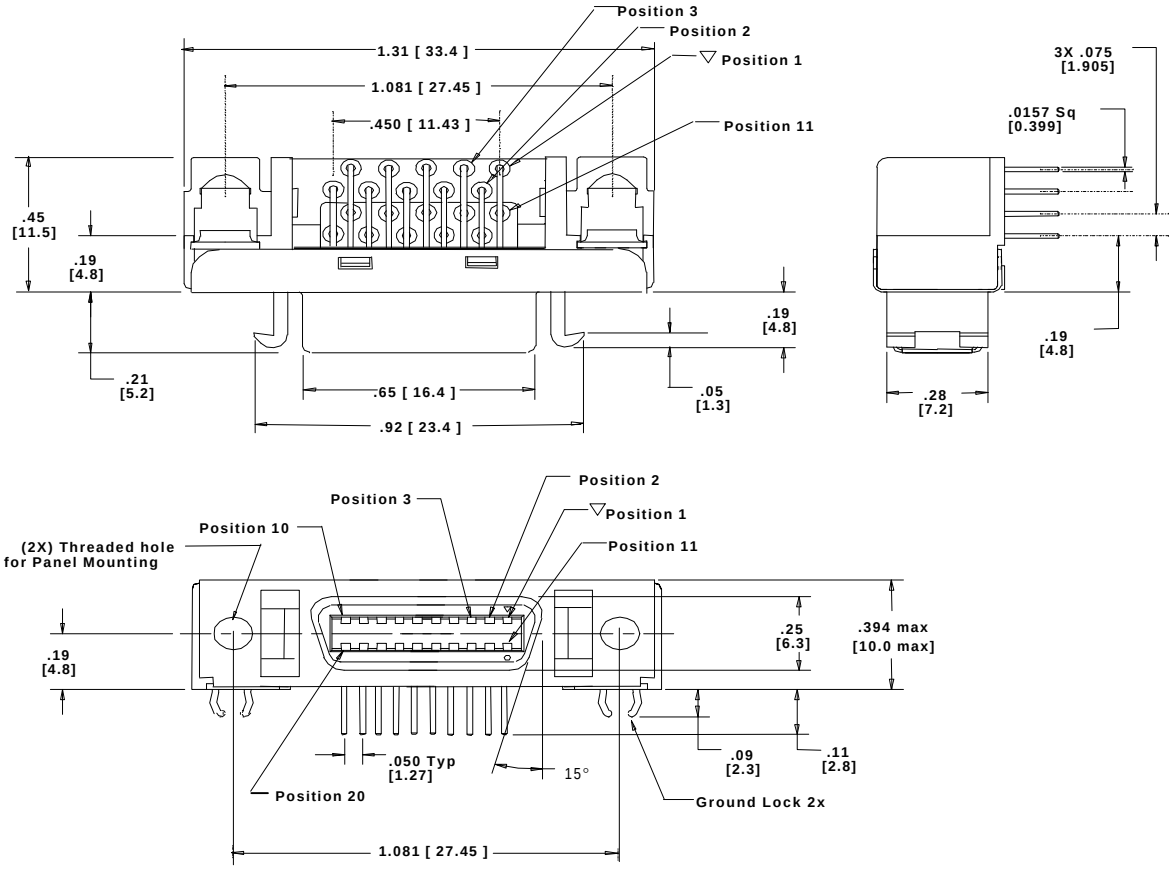
Figure 5.2 includes the features and dimensions of a typical PCB layout and panel cutout for a DFP receptacle. The PCB layout shows the solder tail and ground lock thru-hole placement relative to the PCB edge. The panel cutout dimensions are also provided for proper clearance of the face of the DFP receptacle .

NOTE 1: Most connector manufacturers have detailed drawings and specifications of board layout requirements and recommendations. The system designer should contact the connector manufacturer of choice for the latest specifications.

NOTE 2: The system designer will need to define the connector performance requirements with respect to environmental and electrical requirements as defined by the application.

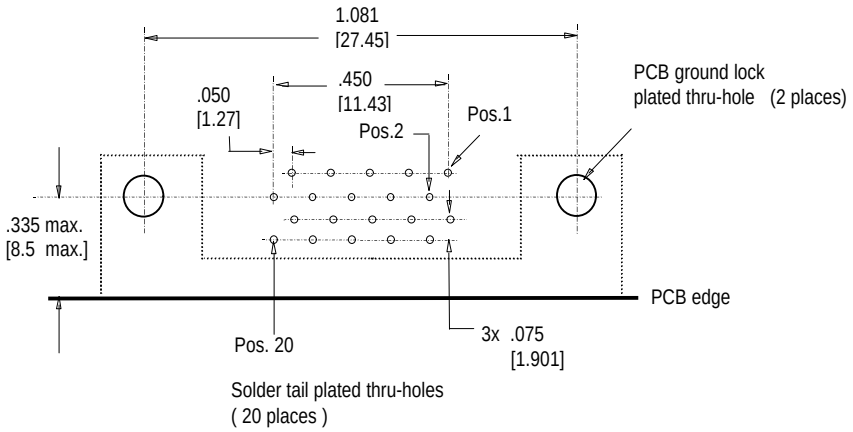
NOTE 3: The system designer will need to obtain additional information from the connector manufacturer to assure compatibility of a DFP plug and receptacle when specifying a connector system.

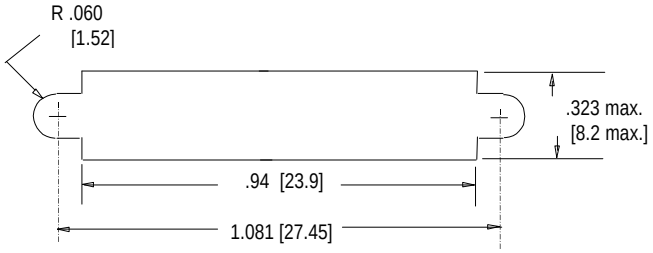
FIGURE 5-1. DFP RECEPTACLE – TYPICAL MATING INTERFACE DIMENSIONS AND FEATURES (inches [mm])



NOTE: Typical dimensions are shown, see connector manufacturer for detailed dimensions and tolerances.

FIGURE 5-2. DFP RECEPTACLE-TYPICAL BOARD LAYOUT AND PANEL CUTOUT DIMENSIONS (INCHES [MM])





NOTE: Typical dimensions are shown, see connector manufacturer for detailed dimensions and tolerances.

BIBLIOGRAPHY

This standard is supplemented by the following publications or their most current issue.

VESA Display Data Channel (DDC) Standard, Version 3.0, September 15, 1997

VESA Extended Display Identification (EDID) Standard, Version 3.0, November 13, 1997

VESA Plug and Display (P&D) Standard, Version 1.0, June 11, 1997

VESA Display Monitor Timing Specifications (DMTS), Version 1.7, December 18, 1996

APPENDIX A. ACRONYMS AND ABBREVIATIONS

This appendix defines acronyms and abbreviations commonly used in this standard, all VESA standards, and industry publications.

CRT	Cathode Ray Tube
DDC	(VESA) Display Data Channel
DDC2B	Simplest of the DDC modes defined in the VESA DDC standard
EDID	(VESA) Extended Display Identification Data
I^2C™	Trademark of Philips used to refer to Inter IC or I^2C bus
LCD	Liquid Crystal Display
MSB	Most Significant Bit
OSD	On Screen Display
P&D™	Trademark of VESA for Plug and Display standard
PanelLink™	Trademark of Silicon Image for their TMDS technology
RGB	Red, Green, Blue video signals
SCL	Serial Clock - I2C clocking signal
SDA	Serial Data - I2C data signal
TFT	Thin Film Transistor (LCD)
TMDS™	Transition Minimized Differential Signaling–Trademark of Silicon Image
TTL	Transistor-transistor Logic
VESA	Video Electronic Standards Association
VGA	Video Graphics Adapter