USB Chapter 7 Addendum

Draft 0.79 – October 5, 1999

Note on USB 2.0 Bit Rate: This specification draft calls out a data rate of 480Mb/s. This is the target rate for which the Electrical Working Group is designing and prototyping; this rate needs to be confirmed with completed validation of prototype IC's operating on test boards. Chapter 7 will roll to the 0.9 level after this prototype validation is completed.

High Speed Electrical Addendum to USB Specification Version 1.1, Chapter 7

This document describes the signaling and physical layer specifications for USB devices which support High Speed (HS) signaling mode.

Devices which only support Low Speed (LS) and/or Full Speed (FS) are not impacted by this Addendum.

The sections in this document are not numbered sequentially. Instead, the sections are numbered to match the associated sections in Chapter 7 of the USB Specification Revision 1.1. For example, in this Addendum there are no sections 7.1.1.1 or 7.1.1.2 because those sections in the Revision 1.1 specification are about FS and LS driver characteristics and the new HS electrical specification does not require any changes to those sections. This Addendum does contain a section 7.1.1.3 which is not in the Revision 1.1 specification, and that section covers the new topic of HS driver characteristics.

Unless noted otherwise, hubs and devices which operate in LS, FS, and/or HS modes must conform to all USB 1.1 specifications when in LS or FS modes and must conform to this addendum when operating in HS mode.

In those few cases where a HS capable device which is operating in LS or FS mode is required to operate differently from the way called out in the USB 1.1 specification, this addendum supercedes the existing specification.

A HS capable upstream facing port shall never operate in LS signaling mode. A HS capable downstream facing port must be able to operate in HS, FS, and LS modes.

To assure reliable operation at HS data rates, this specification assumes the use of cables which conform to USB 1.1 specifications, and additionally to those cable specifications called out herein.

7.1 High Speed Signaling Overview

A High Speed USB connection is made through a shielded, twisted pair cable which conforms to the cable specifications called out herein.

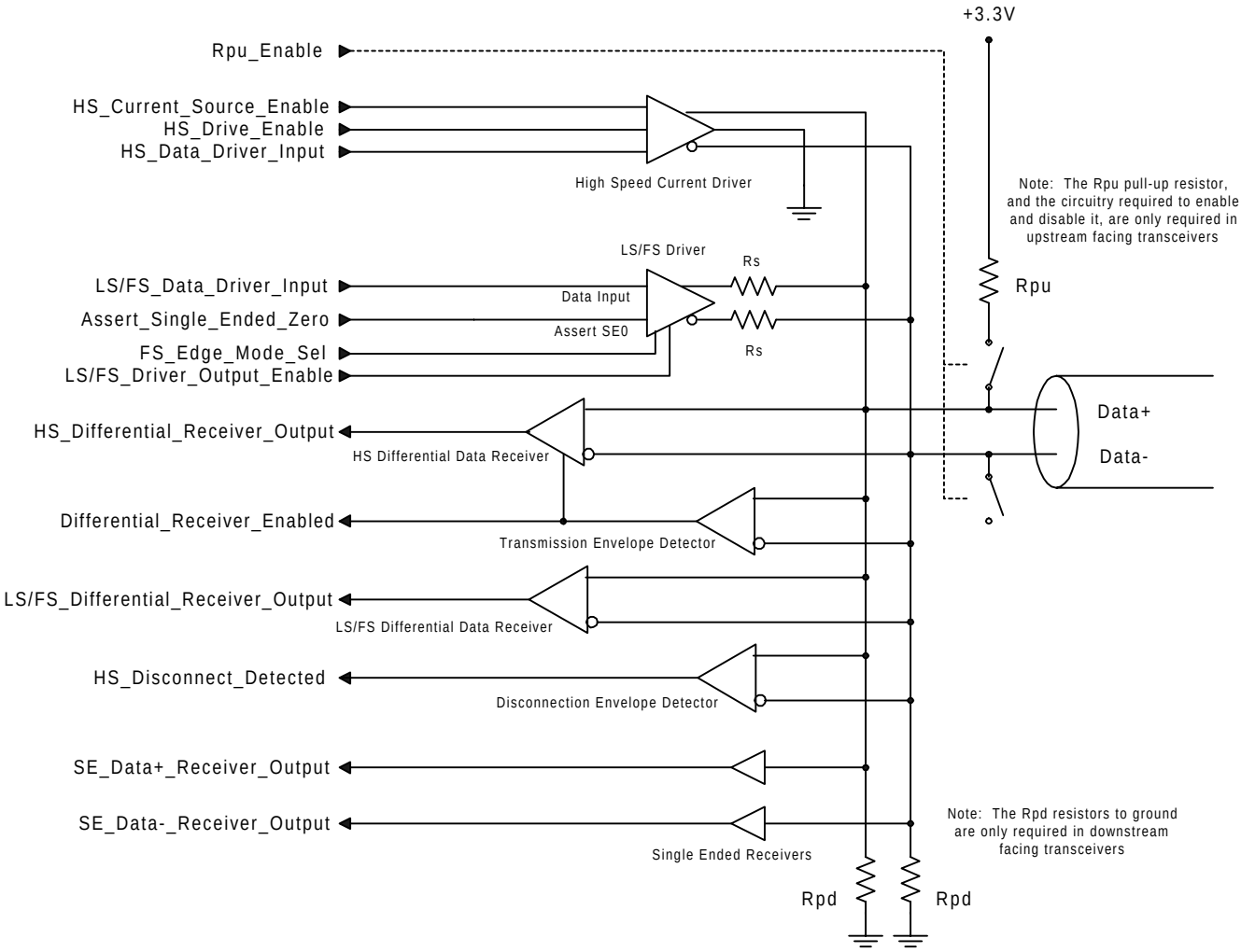

Figure 7.1 - Example HS Capable Transceiver Circuit

Figure 7.1 depicts an example implementation which largely utilizes USB 1.1 transceiver elements and adds the new elements required for HS operation.

High speed operation supports signaling at 480Mb/s. To achieve reliable signaling at this rate, the cable is terminated at each end with a resistance from each wire to ground. The value of this resistance (on each wire) is nominally set to 1/2 the specified differential impedance of the cable, or 45 Ohms. This presents a differential termination of 90 Ohms.

The quiescent state of a transceiver which is operating in HS mode is the terminated state with no signal applied to the Data+ and Data- lines. This state is achieved by using the LS/FS driver to assert a single ended zero, and to closely control the combined total of the driver output

impedance and the R_S resistance (to 45 Ohms, nominal). The recommended practice is to make the driver impedance as low as possible, and to let R_S contribute as much of the 45 Ohms as possible. This will generally lead to the best termination accuracy with the least parasitic loading.

In order to transmit in HS mode, a transceiver activates an internal current source which is derived from its positive supply voltage and directs this current into one of the two data lines via a high speed current steering switch.

The dynamic switching of this current into the Data+ or Data- line follows the NRZI data encoding scheme described in the USB 1.1 specification, including the bit stuffing behavior. To signal a J the current is directed into the Data+ line, and to signal a K the current is directed into the Data- line. The SYNC field and the EOP delimiters have been modified for HS mode.

The magnitude of the current source and the value of the termination resistors are controlled to specified tolerances, and together they determine the actual voltage drive levels. The DC resistance from Data+ or Data- to the device ground is required to be 45 Ohms +/- 10% when measured without a load, and the differential output voltage measured across the lines (in either the J or K state) must be +/- 400mV +/- 10% when terminated with precision 45 Ohm resistors to ground.

The differential voltage developed across the lines is used for three purposes:

- A differential receiver at the receiving end of the cable receives the differential data signal
- A differential envelope detector at the receiving end of the cable determines when the differential signal on the line is below the minimum receivable level and "squelches" the receive circuitry to prevent unintended noise from entering the receive logic
- In the case of a downstream facing hub port which is actively transmitting, a differential envelope detector monitors whether the differential voltage on the lines significantly exceeds the maximum signaling levels. This is used to detect device disconnection. In the absence of the far end terminations, the differential voltage will nominally double (as compared to when a HS device is present) when the current is not switched for a period exceeding the round-trip delay.

When used in a downstream facing port, a HS capable transceiver must be able to operate in LS, FS, or HS signaling modes. When used in an upstream facing port, a transceiver must be capable of operating in FS or HS mode. An upstream facing HS capable transceiver may not operate in LS signaling mode. Therefore a 1.5k pull-up on the Data- line is not allowed, since a HS capable transceiver must never signal LS operation to the hub port to which it's attached.

Table 7.1 describes the functional elements of the example HS capable transceiver shown in Figure 7.1.

Table 7.1 - Description of functional elements in example shown in Figure 7.1

Element	Description
LS/FS Driver	The LS/FS driver is used for LS and FS transmission. It is required to meet all specifications called out in USB 1.1 for LS and FS operation, with one exception. The exception is that in HS capable transceivers the impedance of each output, including the contribution of R_S, must be 45 Ohms +/- 10%. When the transceiver is operating in HS mode, this driver must assert a SE0. Because of the tightened output impedance requirement described above, asserting a SE0 provides a well-controlled HS termination on each data line of 45 Ohms to ground. This is equivalent to a 90 Ohm differential termination.
LS/FS Differential Receiver	The LS/FS differential receiver is used for receiving LS and FS data, and is required to meet all specifications called out in USB 1.1.
Single Ended Receivers	The single ended receivers are required to meet all specifications called out in USB 1.1.
HS Current Driver	The HS current driver is used for HS data transmission. A current source derived from a positive supply is switched into either the Data+ or Data- lines to signal a J or a K, respectively. The nominal value of the current source is 17.78mA. When this current is applied to a data line with a 45 Ohm termination to ground at each end, the nominal high level voltage is +400mV. The nominal differential HS voltage (Data+ - Data-) is thus 400mV for a J, and -400mV for a K. The current source must meet the required accuracy starting with the first symbol of a packet. One means of achieving this is to leave the current source on continuously when a transceiver is operating in HS mode. If this approach is used, the current can be directed to the port ground when the transceiver is not transmitting (the example design in Figure 7.1 shows a control line called HS_Current_Source_Enable to turn the current on, and another called HS_Drive_Enable to direct the current into the data lines.) The penalty of this approach is the 17.78mA of standing current for every such enabled transceiver in the system. The preferred design is to fully turn the current source off when the transceiver is not transmitting.
HS Differential Data Receiver	The HS differential data receiver is used to receive HS data, which has a nominal differential amplitude of +/- 400mV. This receiver must have the ability to be disabled by the Transmission Envelope Detector, as indicated in Figure 7.1. This is a requirement because the quiescent state of a HS link is with the receivers at each end active and with the data lines held at ground. In this condition, the receivers are susceptible to noise or spurious signals, and a means of "squelching" is required. It is left to transceiver designers to choose between incorporating separate HS and LS/FS receivers, as shown in Figure 7.1, or combining both functions into a single receiver.
Transmission Envelope Detector	This envelope detector is used to disable the HS receiver when the amplitude of the differential signal falls below the minimum required level for data reception. It must have a response time which is sufficient to enable or disable reception within 4 bit times of when the signal goes above or below the squelch threshold, respectively.

Table 7.1 (continued) - Description of functional elements in example shown in Figure 7.1

Disconnection Envelope Detector	This envelope detector is used to detect when the amplitude of the differential signal exceeds the maximum allowable data signaling levels. This will occur when a downstream facing transceiver transmits a continuous string of J's or K's for more than the round trip time of the cable and device termination resistors are not present. Because such a string of J's or K's is required as part of the uSOF EOP, the Disconnection Envelope Detector is used for detecting disconnection of HS devices.
Pull-up Resistor (R_{PU})	This resistor is required only in upstream facing transceivers, and is used to indicate signaling speed capability. A HS capable device is required to initially attach as a FS device, and must transition to HS as described in this specification. Once operating in HS, the 1.5k Ohm resistor must be electrically removed from the circuit. In Figure 7.1, a control line called R_{PU}_Enable is indicated for this purpose. The preferred embodiment is to attach matched switching devices to both the Data+ and Data- lines so as to keep the lines' parasitics balanced, even though a pull-up resistor will never be used on the Data- line of an upstream facing HS capable transceiver.
Pull-down Resistors (R_{PD})	These resistors are required only in downstream facing transceivers, and must conform to USB 1.1 specifications.

7.1.1.3 HS Driver Characteristics

A HS USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance of 90 Ohms +/- 15% and a maximum one-way delay of 26ns. Data+ and Data- circuit board traces should also meet this impedance specification. The differential output impedance of a HS capable driver is 90 Ohms +/- 10%. When either the Data+ or Data- lines are driven high, V_{HSOH} (the HS mode high-level output voltage driven on a data line with a 45 Ohm load to GND) must be 400mV +/- 10%. On a line which is not driven high (either because the transceiver is not transmitting or because the opposite line is being driven high) V_{HSOL} (the HS mode low-level output voltage driven on a data line with a 45 Ohm load to GND) must be 0V +/- 5mV.

***Note**: Unless indicated otherwise, all voltage measurements are to be made with respect to the local circuit ground.*

***Note:** This addendum requires that a HS capable transceiver operating in FS or LS mode will have a driver impedance of 45 Ohms, +/- 10%. This addendum supercedes the USB 1.1 specification for driver output impedance, which allows a range of 28 to 44 Ohms. However, that specification remains in effect for devices which do not support HS mode.*

On downstream facing ports, R_{PD} resistors (15k +/- 5%) must be connected from Data+ and Data- to ground.

When a HS capable transceiver operating in LS or FS mode transitions to HS mode, a number of configuration changes occur. These changes are described for the design shown in the Figure 7.1 example implementation, and for the signals described in Table 7.1.

- The 1.5k Ohm pull-up resistor, R_{PU}, which was used to indicate FS mode (in the case of an upstream facing transceiver) is electronically removed from the circuit. This is achieved by setting R_{PU}_Enable low.

- To provide the Data+ and Data- terminations to ground, the Assert_Single_Ended_Zero and the LS/FS_Driver_Output_Enable bits are high.

As described in the overview, the quiescent state of a transceiver operating in HS mode is with the LS/FS driver held in its Single Ended Zero state (so as to provide the required terminations), and with the HS current source in a state in which the source is active, but the current is being directed into the device ground rather than through the current steering switch which is used for data transmission. Steering the current to ground is accomplished by setting the HS_Drive_Enable low.

***Note**: As mentioned above, the implementation of current sources with fast turn on is optional. Such implementations will turn the current on and off directly with the HS_Drive_Enable signal, and will not direct a standing current to ground when in the quiescent state.*

In CMOS implementations, the driver impedance (Z_{OUT}) will typically be realized by the combination of the driver's output impedance (Z_{DRV}) and R_S. To optimally control Z_{OUT} and to minimize parasitics, it is preferred the driver impedance be minimized (under 5 Ohms) and the balance of the 45 Ohms should be contributed by the R_S component.

When a transceiver operating in HS mode begins transmitting, the transmit current is redirected from the device ground to the current steering switch. This switch in turn directs the current to either the Data+ or Data- data line. A J is asserted by directing the current to the Data+ line, a K by directing it to the Data- line.

When each of the data lines is terminated with a 45 Ohm resistor to the device ground, the effective load resistance on each side is 22.5 Ohms. Therefore, the line into which the drive current is being directed rises to 17.78 ma * 22.5 Ohms, or 400mV (nominal). The other line remains at the device ground voltage. When the current is directed to the opposite line, these voltages are reversed.

7.1.2 HS Signaling Eye Patterns, Rise and Fall Times

The following specifications apply to HS mode signaling. The USB 1.1 specifications are unchanged for LS/FS signaling.

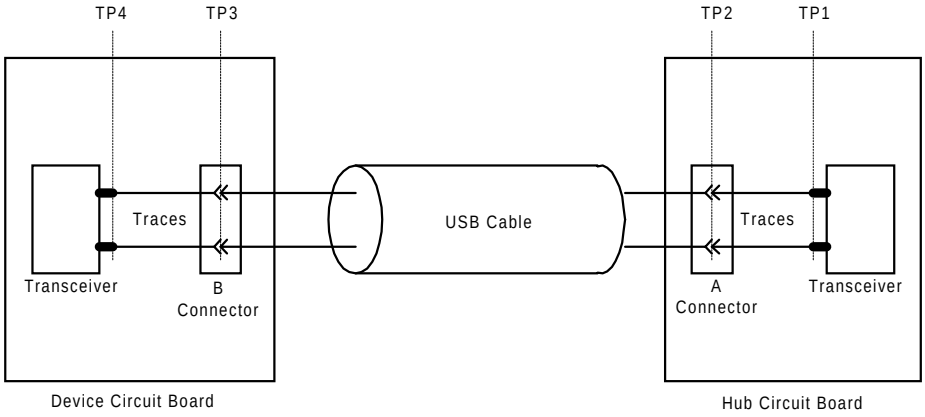

Figure 7.2 - Measurement Planes

Figure 7.2 defines four test planes which will be referenced in this section. TP1 and TP4 are the points where the transceiver IC pins are soldered to the circuit boards. TP2 is at the mated pins of the A connector, and TP3 is at the mated pins of the B connector (or where the cable is attached to the circuit board if there is no B connector). The following differential eye pattern templates specify transmit waveform and receive sensitivity requirements at various points and under various conditions. Conformance to Template 1 and Template 6 are recommended guidelines for designers. Conformance to Templates 2, 3, 4, and 5 are required for USB 2.0 hubs and devices.

Template 1: Transmit waveform requirements for hub transceiver measured at TP1
Transmit waveform requirements for device transceiver measured at TP4

Template 2: Transmit waveform requirements for hub transceiver measured at TP2
Transmit waveform requirements for device transceiver measured at TP3
(applies only to the case when the device does not have a captive cable)

Template 3: Transmit waveform requirements for device transceiver measured at TP2
(applies only to the case when the device has a captive cable)

Template 4: Receiver sensitivity requirements for device transceiver measured at TP2
(applies only to the case when the device has a captive cable)

Template 5: Receiver sensitivity requirements for device transceiver measured at TP3
(applies only to the case when the device does not have a captive cable)
Receiver sensitivity requirements for hub transceiver measured at TP2

Template 6: Receiver sensitivity requirements for device transceiver measured at TP4
Receiver sensitivity requirements for hub transceiver measured at TP1

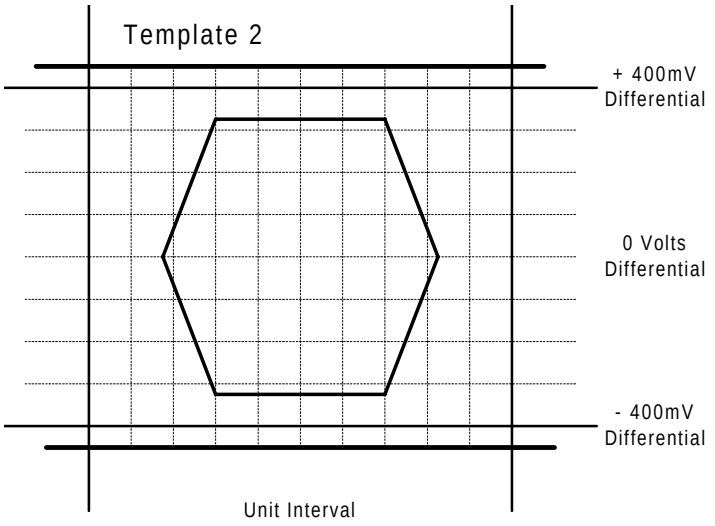

Figure 7.3 – Transmit Eye Patterns

*(**Note:** Similar diagrams for Templates 1 and 3 under development)*

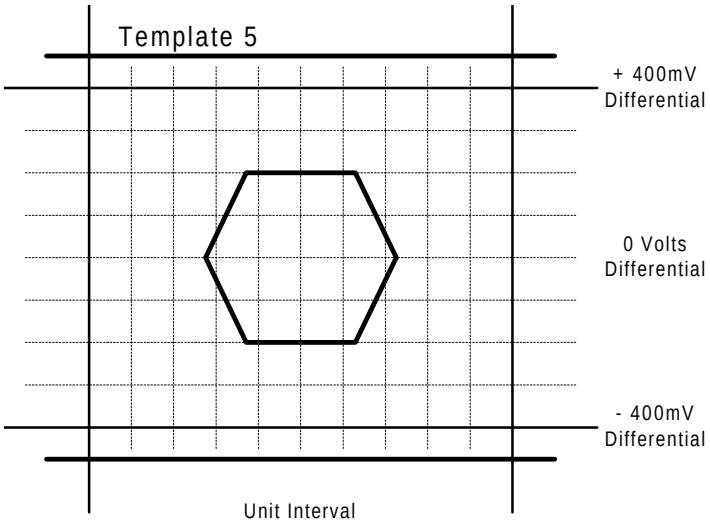

Figure 7.4 – Receiver Sensitivity Eye Patterns

*(**Note:** Similar diagrams for Templates 4 and 6 are under development)*

Transmit eye patterns specify the minimum and maximum limits, as well as limits on timing jitter, within which a transmitter must drive signals at each of the specified test planes.

Receive eye patterns specify the minimum and maximum limits, as well as limits on timing jitter, within which a receiver must reliably recover data.

***Note**: It has been suggested that a BER be specified for "reliable data recovery"*

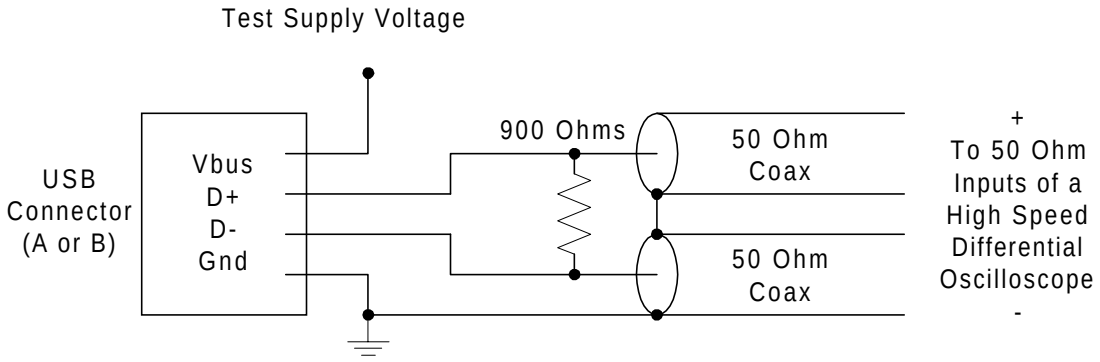

Figure 7.5 – 50 Ohm Measurement Fixture

In addition to the specified eye pattern limits, a transmitter must also meet minimum and maximum differential rise and fall time specifications. Figure 7.5 shows a recommended test fixture for performing these measurements.

For a hub, the 10% to 90% differential rise and fall times of HS signaling must be (Min rise, fall time) <= (T_{HR}, T_{HF}) <= (Max rise, fall time) when measured at the A receptacle with the fixture shown above.

For a device with a captive cable assembly, the 25% to 75% differential rise and fall times of HS signaling must be (Min rise, fall time) <= (T_{HR}, T_{HF}) <= (Max rise, fall time) when measured at the A plug of the captive cable with the fixture shown above.

For a device with a B connector, the 10% to 90% differential rise and fall times of HS signaling must be (Min rise, fall time) <= (T_{HR}, T_{HF}) <= (Max rise, fall time) when measured at the B receptacle with the fixture shown above.

7.1.2.1 HS Driver Usage

In this section there is reference to a situation in which HS operation is "disallowed". This topic is discussed in depth in the Hub chapter of this addendum. In brief, a HS capable hub's downstream facing ports are "HS disallowed" if the hub is unable to establish a HS connection on its upstream facing port. For example, this would be the case for the downstream facing ports of a HS capable hub when the hub is connected to a USB 1.1 host controller.

If a transceiver is not HS capable, or if HS operation is disallowed for the transceiver, its usage is governed by the rules described in the USB 1.1 Specification.

Usage rules for HS capable transceivers which are not HS disallowed:

- An upstream facing transceiver must not support LS signaling. This has always been the case for hubs, but is now a requirement for HS capable functions as well.
- A downstream facing transceiver must support HS, FS, and LS signaling and data rates
- A transceiver must operate at the highest signaling speed which is supported by the transceiver at the other end of its USB cable, and the data rate will be the same as is normally associated with the signaling mode (1.5 Mb/s for LS, 12Mb/s for FS, 480Mb/s for HS)

7.1.3 Cable Skew for HS

The data line skew introduced by the USB cable must be less than 100ps.

Note: *This addendum requires that the data line skew introduced by the USB cable must be less than 100ps. This addendum supercedes the USB 1.1 specification, which allowed a maximum cable skew of 400ps.*

7.1.4 HS Receiver Characteristics

A HS capable transceiver receiver must conform to the USB 1.1 Receiver Characteristics specification when receiving in LS or FS modes.

When receiving in HS mode, the differential receiver must be able to reliably receive signals which conform to the specified Receiver Eye Pattern templates shown in section 7.1.2. The receiver must disable reception when the differential signal amplitude falls below a threshold within the range of 100mV to 150mV. (This means that signals with less than 100mV differential amplitude are required to be disabled, and that signals with greater than 150mV differential amplitude are required to be enabled.) Detection must be done with a differential "Envelope Detection" device, such as the one shown in Figure 7.1. This mechanism must enable reception within 4 symbol times after the start of an incoming packet, and must disable reception within 4 symbol times after the lines return to their quiescent levels following the EOP delimiter.

In the case of a downstream facing port, a HS capable transceiver must indicate device disconnection if the signal amplitude on the data lines exceeds a differential voltage threshold within the range of 500mV to 600mV. (This means that signals with less than 500mV differential amplitude must not cause indication of disconnection, and that signals with greater than 600mV differential amplitude are required to indicate disconnection.) When no downstream device is attached, the disconnect detection circuitry in the downstream facing transceiver must detect the over-voltage condition in response to a single uSOF EOP delimiter. The output of the Disconnect Detection Envelope detector will be used as described in Section 7.1.7.1.

7.1.5 HS Device Speed Identification

The USB 2.0 Reset and HS Detection mechanisms defined in these sections follow the USB 1.1 behavior model. When reset is complete, the link must be operating in its appropriate signaling mode (LS, FS, or HS as governed by the preceding usage rules), and the speed indication bits in the port status register will correctly report this mode. SW need only initiate the assertion of reset and read the port register upon notification of reset completion.

HS capable devices initially attach as FS devices, using the techniques described in the USB 1.1 specification. This means that for HS capable upstream facing ports, R_{PU} (1.5k +/- 5%) must be connected from Data+ to the 3.3V supply (as shown in the Addendum Figure 7.1) through a switch which can be opened under SW control.

After the initial attachment, HS capable transceivers engage in a low level protocol to establish a HS link and to indicate HS operation in the appropriate port status register. This protocol is described in Addendum section 7.1.7.3 (Reset Signaling).

7.1.6 HS Input Characteristics

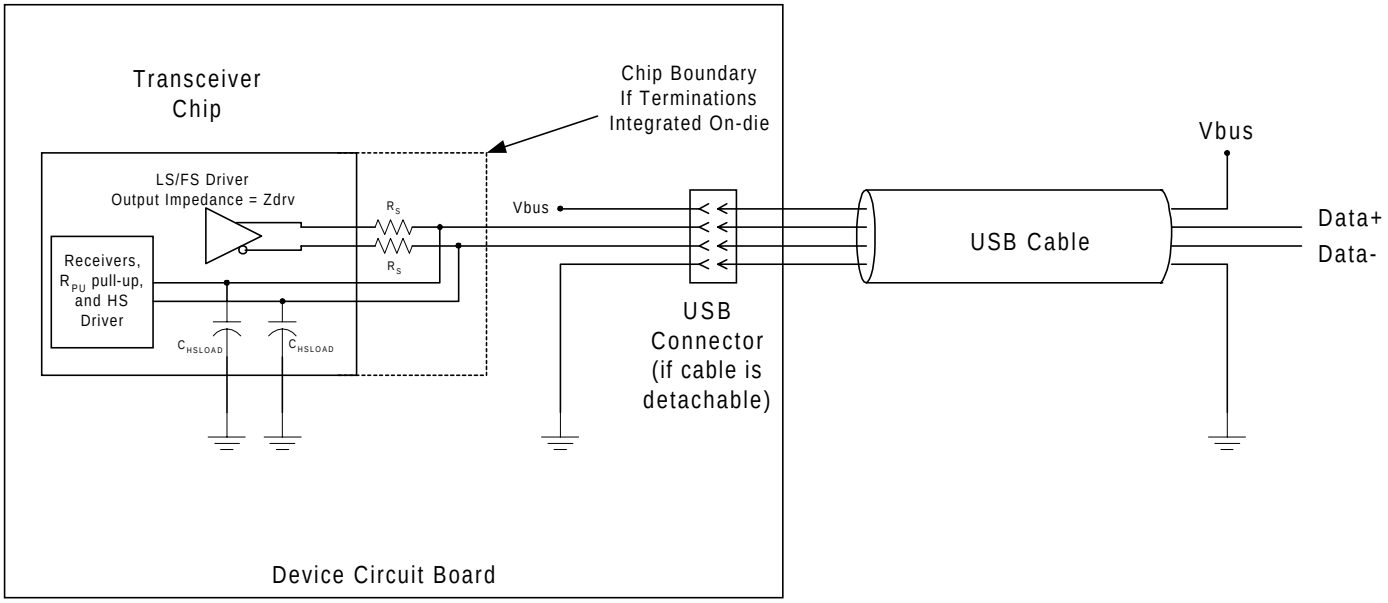

Figure 7.6 – Diagram for HS Loading Equivalent Circuit

Figure 7.6 shows the simple equivalent loading circuit of a USB device operating in HS receive mode.

In addition to meeting the input characteristic requirements called out in the USB 1.1 specification, it is a guideline that a HS capable port should meet Specification 1 (the loading of the transceiver component itself) and it is required that a HS capable port must meet Specification 2 (the loading of the port) as described below.

Specification 1 - HS loading for HS capable transceiver measured in isolation

When characterizing a transceiver chip as an isolated component, the measurement can be performed effectively at the chip boundary shown above, with no additional USB connectors or cables. Parasitic capacitance of the test fixture can be corrected by measuring the capacitance of the fixture itself, and subtracting this reading from the reading taken with the transceiver inserted. If the terminations are off-chip, discrete R_S resistors should be in place during the measurements, and measurements should be taken on the "connector side" of the resistors. The transceiver should be in the HS receive mode during testing.

Resistance and capacitance measurements are taken from each of the data lines to ground while the other line is left open.

Resistance to Ground on each line: 45 Ohms +/- 10%
Capacitance to Ground on each line: <= (C_{HSLOAD})pF

***Note**: A limit of 10pF has been proposed for C_{HSLOAD}. The proposal is to allow a maximum of 5pF for the transceiver die itself, and an additional 5pF for the package.*

Specification 2 – One of the following two specifications, depending on whether device has a captive cable

HS loading specifications for HS capable hubs, and for devices with a B connector

This measurement is performed with a differential TDR, and governs the maximum allowable transmission line discontinuities of the B connector, the circuit board traces, the transceiver package and its leads, and the transceiver circuit itself.

***Note**: The discontinuity specification is under development.*

HS loading specifications for HS capable devices with a captive cable:

This measurement is performed with a differential TDR, and governs the maximum allowable transmission line discontinuities of the A connector, the cable, the connection of the cable to the device circuit board, the circuit board traces, the transceiver package and its leads, and the transceiver circuit itself.

***Note**: The discontinuity specification is under development.*

7.1.7 Signaling Voltage Levels

The HS signaling voltage specifications in Table 7.2 must be met when measuring at the connector closest to the transceiver, using precision 45 Ohm load resistors to the device ground as reference loads. All voltage measurements are taken with respect to the local device ground.

Table 7.2 - Signaling Voltages

Bus state	Signaling Levels
HS Quiescent state	-5mV <= Data+ <= 5mV; -5mV <= Data- <= 5mV
HS J state	360mV <= Data+ <= 440mV; -5mV <= Data- <= 5mV
HS K state	-5mV <= Data+ <= 5mV; 360mV <= Data- <= 440mV
Squelch threshold	The incoming signal must be disabled when its differential amplitude falls below 100mV, and enabled when its differential amplitude exceeds 150mV
HS disconnect on downstream facing port	A downstream facing transceiver must indicate disconnection when the it senses a differential amplitude on the Data+ and Data- line of more than 600mv, and it must not signal disconnection when the voltage is less than 500mV
Start of HS packet	The transmission of a HS packet is initiated by the transition from the HS quiescent state to the HS SYNC pattern, as defined in section 7.1.10
End of HS packet	The HS EOP field is the pattern described in section 7.1.13.2, followed by the HS quiescent state
HS reset	A hub resets a HS capable device by asserting an extended single-ended zero, as described in section 7.1.7.3

7.1.7.1 Connect and Disconnect Signaling

HS capable upstream facing and downstream facing ports must support the USB 1.1 section 7.1.7.1 specifications for FS and LS Connect and Disconnect Signaling.

The means to detect and transition to HS operation are described in Addendum section 7.1.7.3 (Reset Signaling).

A downstream facing port operating in HS mode detects disconnection by sensing the increase in the differential signal amplitude across the Data+ and Data- lines that occurs when the device terminations are removed. As shown in Figure 7.1, the "Disconnection Envelope Detector" output goes high when the downstream facing transceiver transmits and positive reflections from the open line arrive in a phase which is additive with the transceiver driver signal. To assure that this additive effect occurs reliably and is of sufficient duration to be detected, the uSOF EOP delimiter is lengthened, as discussed in Addendum section 7.1.13.2.

Signals with differential amplitudes >= 600mV must reliably activate the Disconnection Envelope Detector. Signals with differential amplitudes <= 500mV must never activate the Disconnection Envelope Detector.

The hub must sample the Disconnection Envelope Detector output at a time which coincides with the transmission of the 40th bit of the uSOF EOP pattern. The detector's output should be ignored at all other times.

7.1.7.2 Data Signaling

HS data transmission within a packet is done with differential signals. The quiescent state of the data lines between packets is both lines at GND.

The start of a packet (SOP) in HS mode is signaled by driving the Data+ and Data- lines from the HS quiescent state to the K state. This K is the first symbol of the SYNC pattern (NRZI sequence KJKJKJKJ KJKJKJKJ KJKJKJKJ KJKJKJKK) as described in Section 7.1.10.

The first symbol in the HS EOP (end of a packet) delimiter is a transition from the last symbol prior to the EOP. This opposite symbol becomes the first symbol in the EOP pattern (NRZ 011111111 with bit stuffing disabled) as described in Section 7.1.13.2. Upon completion of the EOP pattern, the transmitter returns to the quiescent state.

The fact that the first symbol in the EOP pattern forces a transition simplifies the process of determining precisely which is the last bit in the packet prior to the EOP delimiter.

7.1.7.3 Reset Signaling

A HS capable device must be capable of being reset while in HS or FS operation. A HS capable hub must be capable of performing reset and speed detection for both HS capable and non-HS capable devices.

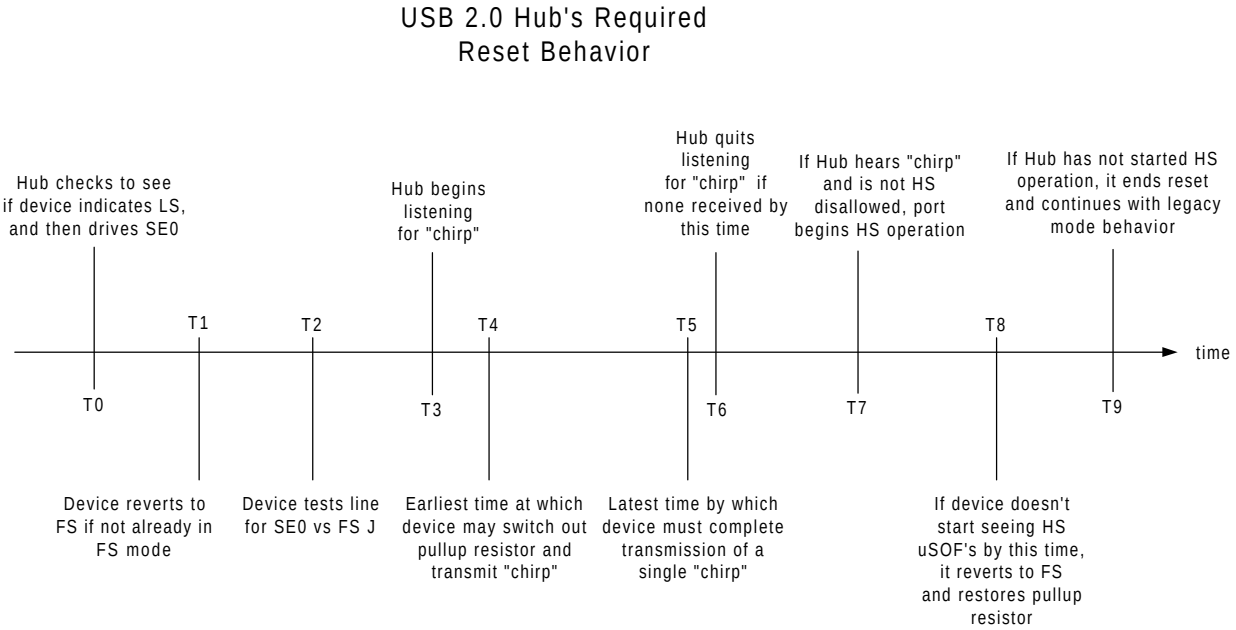

Figure 7.7 - Hub and Device Reset Behavior

A HS capable hub begins the reset process by checking the state of the lines (to determine whether a device is present and indicating LS) and then driving SE0. (Note that the following hub actions will be perceived by a non-HS capable device as a long SE0, and these actions will reset such a device just as a USB 1.1 hub would reset it.) The time at which SE0 is asserted is shown in Figure 7.7 as T0. If the device indicates LS capability, the hub simply holds the assertion of SE0 until T9, doesn't perform any of the following "listening" behaviors, and reports the port speed as LS.

If the hub port does not detect a LS device, it may be attached to a FS device, a HS capable device which is operating in FS mode, a HS capable device operating in HS mode, or no device at all. To differentiate between these possibilities, starting at T3 the hub begins listening for a HS "chirp" from the device.

In response to the assertion of a continuous SE0, at T1 a HS device reverts to FS mode (if not already in FS) by disconnecting its HS terminations and reconnecting the D+ pull-up resistor. 2.5us later, at T2, the device tests the line to determine whether a SE0 or FS J is present. (If the line is at a FS J, the device follows the Suspend process as described in Section 7.1.7.4.)

Upon detecting a SE0 at T2 the device continues with the Reset process, and at a time no sooner than T4 a HS capable device must switch off its Data+ pull-up resistor and restore its HS terminations, and transmit a "chirp" which ends no later than T5. This chirp is defined to be a continuous HS K with a duration of at least 8us.

If a hub detects the HS "chirp" before T6 and is not HS disallowed, it begins HS operation no later than T7. A hub detects a chirp if it sees a continuous HS K at its input for at least 2us. (The 8us assertion and 2us detection requirements make HS detection reliable in the presence of occasional noise events of sub-microsecond duration.) The speed of the link is reported as HS. If the hub fails to detect the "chirp", or if it is HS disallowed, it must remain in SE0 at least until T9. The speed of the link is reported as FS.

If the device begins receiving HS uSOF's before T8, it must continue to operate in HS mode. If it does not begin receiving HS uSOF's by T8, it must revert to FS operation.

Note that by this process, a USB 2.0 hub which resets a port to which nothing is attached will initially report that there is a FS device attached, and immediately thereafter it will detect a disconnection.

Table 7.3 - Reset Timing Values

Timing Parameter	Description	Value
T0	Hub asserts SE0 on the data lines	0 (reference)
T1	Device reverts to FS mode (if not already in FS mode) by connecting D+ pull-up and removing HS terminations	3ms
T2	Device tests for SE0 on the wire (FS J would indicate Suspend rather than Reset)	2.5us after device reverts to FS
T3	Hub begins listening for HS "chirp" from device	4.75ms
T4	Earliest time at which device may disconnect Data+ pull-up resistor, restore HS terminations, and begin transmission of HS "chirp"	5ms
T5	Latest time by which device must complete transmission of HS "chirp"	6ms
T6	Hub stops listening for HS "chirp"	6.25ms
T7	Time by which hub must begin HS operation if HS "chirp" was received	T7 < (End of HS "chirp" + 1ms)
T8	Time at which device restores Data+ pull-up resistor and reverts to FS operation if no HS uSOF's have been received	(End of HS "chirp" + 3ms) < T8 < (End of HS "chirp" + 3.5ms)
T9	Earliest time at which hub may end reset if no HS "chirp" was detected	10ms

7.1.7.4 Suspending

All devices, including HS capable devices, must support the Suspend state. Devices can go into Suspend from any powered state. They begin the transition to the Suspend state after they see a constant Idle state on their upstream facing port for more than 3.0ms. The device must actually be suspended, drawing only Suspend current from the bus, after no more than 10ms of inactivity on all of its ports.

A HS capable hub Suspends an attached device exactly as described in the USB 1.1 specification.

A device operating in HS mode must begin the transition to the Suspend state when, for a time greater than 3.0ms, the downstream facing port to which it is attached ceases transmission and disconnects its HS terminations to ground. This is equivalent to the host's behavior in the FS idle state. From the perspective of a device operating in HS mode, a Reset and a Suspend are initially indistinguishable, so the first part of the device response is the same as for a Reset. This is discussed in Section 7.1.7.3. The device's first step in this process, after the hub has been in the FS idle state for 3ms, is to revert to FS by disconnecting its termination resistors and reconnecting its D+ pull-up resistor. 2.5us after reverting to FS, the device must sample the state of the line. If the state is a FS J, the device continues with the Suspend process. (Had the state been SE0, that would have indicated that the downstream facing port was driving SE0, and the device would have gone into Reset as described in 7.1.7.3.)

7.1.7.4.1 Global Suspend

A HS capable device or hub must support Global Suspend as described in USB 1.1.

7.1.7.4.2 Selective Suspend

USB 2.0 hubs must support the same selective suspend functionality as required by USB 1.1.

7.1.7.5 Resume

If a hub port and device were not operating in HS mode at the time they were suspended, resume behavior is unchanged from USB 1.1.

This section covers resume behavior required for the case in which the hub port and device were operating in HS prior to suspend. Since at the end of resume both port and device "remember" that they were previously operating in HS, they can immediately transition back to HS operation without arbitration within T_{RHSMAX}. Thus after the assertion of the extended K, the device signaling Resume drives SE0 and then transitions directly to the HS quiescent state (both Data lines driven to ground).

In a host directed resume, both the hub and device will transition to HS shortly after the host drives the bus to SE0 from K. T_{RHSMAX} must be no longer than one microframe. Downstream facing hub ports must drive Data+ and Data- to GND continuously as they transition from FS SE0 to the HS quiescent state.

It is required that the host begin sending uSOF's within 3ms (to prevent the HS tree from suspending).

7.1.8 Data Encoding/Decoding

HS USB uses the same NRZI encoding and decoding mechanisms as LS/FS modes.

7.1.9 Bit Stuffing

HS USB uses the same bit stuffing mechanisms as LS/FS modes, with the exception of the intentional bit stuff errors used in the HS EOP as described in Section 7.1.13.2.

7.1.10 SYNC Pattern

The SYNC pattern used for HS transmission is required to be 15 KJ pairs followed by 2 K's, for a total of 32 symbols. Hubs are allowed to drop up to 4 bits from the start of the SYNC pattern when repeating packets. Hubs must not corrupt any repeated bits of the SYNC field, however. Thus after being repeated by 5 hubs, a packet's SYNC field may be as short as 12 bits.

7.1.11 Data Signaling Rate

The data signaling rate when operating in HS mode must be 480Mb/s, with a bit rate accuracy of +/- 500ppm. This accuracy must be maintained over allowable operating temperatures, supply voltages, aging effects.

7.1.12 Frame Interval and Frame Interval Adjustment

For USB2.0 the master clock in the system is the host-controller clock; synchronizing to other references will not be supported.

7.1.13.1 HS Data Source Jitter (HS data originating from a port)

HS data within a single packet must be transmitted with no more jitter than is allowed by the eye patterns defined in section 7.1.2.

Additionally, the delay through a hub repeater may vary over a total range of +/- 3 bit times from packet to packet.

7.1.13.2 HS EOP

For HS packets other than uSOF's the EOP delimiter is required to be an NRZ byte of 01111111 without bit stuffing. For example, if the last symbol prior to the EOP field is a J, this would lead to an EOP of KKKKKKKK.

For HS uSOF's the EOP delimiter is required to be 5 NRZ bytes without bit stuffing, consisting of 01111111 11111111 11111111 11111111 11111111. Thus if the last bit prior to the EOP field is a J, this would lead to 40 K's on the wire, at the end of which the transmitter returns to the quiescent state.

A hub is allowed to add up to 4 random bits to the end of the EOP field when repeating a packet. Thus after 5 repeaters, a packet can have up to 20 random bits following the EOP field. A hub must not corrupt any of the 8 (or 40, in the case of a uSOF) required bits of the EOP field, however.

7.1.14 Hub Signaling Timings (HS data transmitted through a Hub repeater section)

When a hub acts as a repeater for HS data, the delay of the hub must not exceed 36 bit times plus 4ns (the trace lengths allowed for the hub circuit board). This delay is measured from the last bit of the SYNC field at the input connector to the last bit of the SYNC field at the output connector.

A HS hub repeater must digitally resynchronize the buffered data, so there is no allowance for cumulative jitter (within a single packet) as a HS packet passes through multiple repeater stages. Within a single packet, the jitter must not exceed the eye pattern templates defined in section 7.1.2.

Because the data synchronization process in a hub repeater may be implemented at a sub-harmonic of the actual bit rate, the propagation delay of a hub repeater is allowed to vary by up to +/- 3 bit times from packet to packet. (This allows for some uncertainty as to when an incoming packet arrives at the hub with respect to the phase of the synchronization clock.)

7.1.15 Receiver Data Jitter

A HS capable receiver must reliably recover data which meets the receiver eye pattern templates called out in Section 7.1.2 and the jitter budgets called out in Section 7.1.13.1.

***Note**: It has been suggested that a BER be specified for "reliable data recovery"*

7.1.16 Cable Delay

The cable delay specification is the same as called out in USB 1.1.

7.1.17 Cable Attenuation

Cables must not exceed the loss figures shown in Table 7.4.

Table 7.4 - Maximum Allowable Cable Loss

Frequency (MHz)	Attenuation (maximum) dB/cable
0 < Frequency <= .064	.08
.064 < Frequency <= .256	.11
.256 < Frequency <=.512	.13
.512 < Frequency <=.772	.15
.772 < Frequency <= 1.000	.20
1.000 < Frequency <= 4.000	.39
4.000 < Frequency <= 8.000	.57
8.000 < Frequency <= 12.000	.67
12.000 < Frequency <= 24.000	.95
24.000 < Frequency <= 48.000	1.35
48.000 < Frequency <= 96.000	1.9
96.000 < Frequency <= 200.00	3.2
200.000 < Frequency <= 400.00	5.8

7.1.18 Bus Turn Around Time and Inter-packet Delay

HS inter-packet delays are measured from time when the line returns to a squelch level at the end of one packet to when the line leaves the squelch level at the start of the next packet.

Hosts and devices are required to allow an inter-packet delay of at least 8 bit times, measured at their A or B connectors respectively. Additionally, if a host is transmitting two packets in a row, the minimum allowable inter-packet gap is 88 bit times, measured at the host's A connector.

If a function is expected to provide a response to a host transmission, the maximum inter-packet delay for a function or hub with a detachable cable is 176 bit times, measured at the B connector. If the device has a captive cable, the maximum inter-packet delay is 176 bit times plus 52ns (2 times the max cable length).

The maximum inter-packet delay for a host response is 176 bit times, measured at the A connector.

There is no maximum inter-packet delay between packets in unrelated transactions.

7.1.19 Maximum End-to-end Signal Delay

As in the LS/FS modes, a HS device expecting a response to a transmission will invalidate the transaction if the inter-packet gap exceeds the maximum allowable time.

In HS mode, the worst case round trip signal delay model is the sum of the following components:

12 max length cable delays (6 in each direction)	= 312ns
10 max delay hubs (5 in each direction)	= 40ns + 360 bit times
1 max device response time	= 1ns + 176 bit times
Maximum response time	**= 353ns + 536 bit times**

7.1.20 Test mode support (new section, not an extension to a USB 1.1 section)

To facilitate compliance testing, HS capable hubs and devices must support the following test modes. Since the host controller is a (root) hub, this proposal applies seamlessly to host controller testing.

- Test SEO_NAK: Upon command, a hub or device must enter the HS receive mode and remain in that mode until the specified action is taken. This enables the testing of output impedance, low level output voltage, and loading characteristics. In addition, while in this mode a device must respond to a IN token packet with a NAK handshake (only if the packet CRC is determined to be correct) within the normal allowed device response time. This enables testing of the device squelch level circuitry, and additionally provides a general purpose stimulus/response test for basic functional testing.
- Test J: Upon command, a hub or device must enter the HS J state and remain in that state until the specified action is taken. This enables the testing of the high output drive level on the Data+ line.
- Test K: Upon command, a hub or device must enter the HS K state and remain in that state until the specified action is taken. This enables the testing of the high output drive level on the Data- line.
- Test PRBS: Upon command, a hub or device must continuously transmit a specified (TBD) data pattern until the specified action is taken. This enables the testing of rise and fall times, eye patterns, jitter, and any other dynamic waveform specifications.
- Test Force_Enable: Upon command, a downstream facing hub port must be enabled in HS mode, even if there is no device attached. Packets arriving at the hub's upstream facing port must be repeated on the port which is in this test mode. This enables testing of the hub's disconnect detection; the disconnect detect bit can be polled while varying the loading on the port, allowing the disconnect detection threshold voltage to be measured.

For an upstream facing port, the exit action is to power cycle the device. For a downstream facing port, the exit action is issuance of the ClearPortFeature(TEST_MODE) command.

For device/hub upstream facing port:

A new command called SetFeature(TEST_MODE) is defined in Section 9.4.9. This command is used to enter the selected test mode. To exit the test mode, the device must be power cycled.

For hub downstream facing port:

Two new commands called SetPortFeature(TEST_MODE) and ClearPortFeature(TEST_MODE) are defined to enter and exit this test mode, respectively. These commands are defined in Section 11.22.2.10.

All high-speed capable devices/hubs must support the respective commands. (Since these are unsupported commands in non-HS devices, they will return a STALL). The command is implemented on successful completion of the transfer, after the ACK of the status stage.

7.2 Power Distribution

There are no changes to the USB 1.1 power distribution specifications in USB 2.0.

7.3 Physical Layer

***Note**: This section is a set of tables enumerating all the HS specifications. Creation of these tables is deferred until the previous sections have been completed and ratified.*