

SECTION 10

HARDWARE DESIGN TECHNIQUES

- Low Voltage Interfaces
- Grounding in Mixed Signal Systems
- Digital Isolation Techniques
- Power Supply Noise Reduction and Filtering
- Dealing with High Speed Logic

SECTION 10

HARDWARE DESIGN TECHNIQUES

Walt Kester

LOW VOLTAGE INTERFACES

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For the past 30 years, the standard V_{DD} for digital circuits has been 5V. This voltage level was used because bipolar transistor technology required 5V to allow headroom for proper operation. However, in the late 1980s, Complimentary Metal Oxide Semiconductor (CMOS) became the standard for digital IC design. This process did not necessarily require the same voltage levels as TTL circuits, but the industry adopted the 5V TTL standard logic threshold levels to maintain backward compatibility with older systems (Reference 1).

The current revolution in supply voltage reduction has been driven by demand for faster and smaller products at lower costs. This push has caused silicon geometries to drop from $2\mu\text{m}$ in the early 1980s to $0.25\mu\text{m}$ that is used in today's latest microprocessor and IC designs. As feature sizes have become increasingly smaller, the voltage for optimum device performance has also dropped below the 5V level. This is illustrated in the current microprocessors for PCs, where the optimum core operating voltage is programmed externally using voltage identification (VID) pins, and can be as low as 1.3V.

The strong interest in lower voltage DSPs is clearly visible in the shifting sales percentages for 5V and 3.3V parts. Sales growth for 3.3V DSPs has increased at more than twice the rate of the rest of the DSP market (30% for all DSPs versus more than 70% for 3.3V devices). This trend will continue as the high volume/high growth portable markets demand signal processors that contain all of the traits of the lower voltage DSPs.

On the one hand, the lower voltage ICs operate at lower power, allow smaller chip areas, and higher speeds. On the other hand, the lower voltage ICs must often interface to other ICs which operate at larger V_{DD} supply voltages thereby causing interface compatibility problems. Although lower operating voltages mean smaller signal swings, and hence less switching noise, noise margins are lower for low supply voltage ICs.

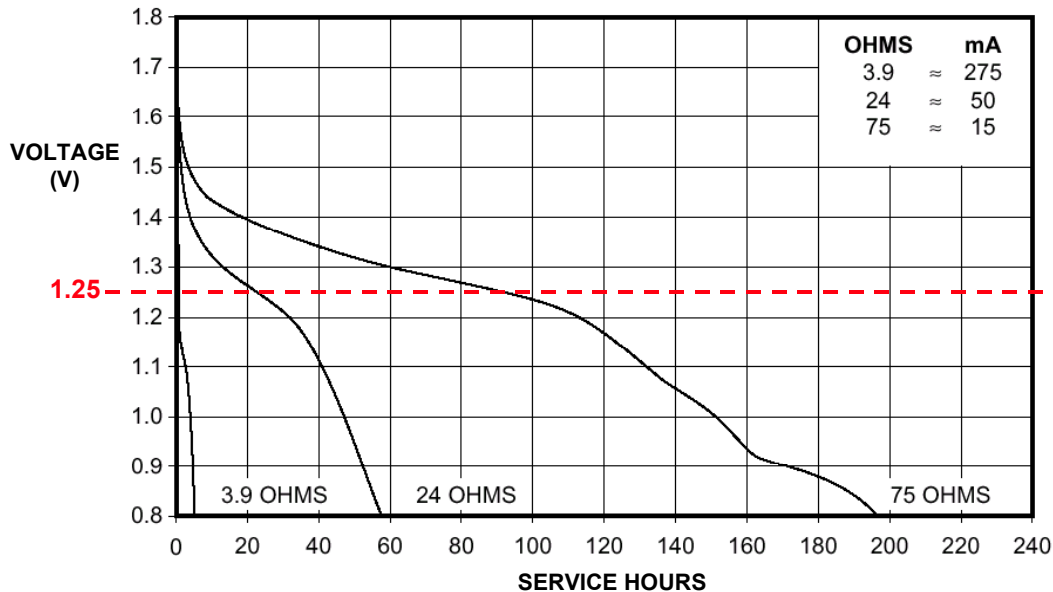
The popularity of 2.5V devices can be partially explained by their ability to operate from two AA alkaline cells. Figure 10.2 shows the typical discharge characteristics for a AA cell under various load conditions (Reference 2). Note that at a load current of 15mA, the voltage remains above +1.25V (2.5V for two cells in series) for nearly 100 hours. Therefore, an IC that can operate effectively at low currents with a supply voltage of $2.5V \pm 10\%$ (2.25V - 2.75V) is very useful in portable designs. Also, DSPs that have low mA/MIPS ratings and can integrate peripherals onto a single chip, such as the ADSP-218x L or M-series, are useful in portable applications.

LOW VOLTAGE MIXED-SIGNAL ICs

- Lower Power for Portable Applications
- 2.5V ICs Can Operate on Two “AA” Alkaline Cells
- Faster CMOS Processes, Smaller Geometries, Lower Breakdown Voltages
- Multiple Voltages in System: +5V, +3.3V, +2.5V, +1.8V
DSP Core Voltage (VID), Analog Supply Voltage
- Interfaces Required Between Multiple Logic Types
- Lower Voltage Swings Produce Less Switching Noise
- Lower Noise Margins
- Less Headroom in Analog Circuits Decreases Signal Swings and Increases Sensitivity to Noise (But that’s the subject of an entire seminar!)

Figure 10.1

DURACELL MN1500 “AA” ALKALINE BATTERY DISCHARGE CHARACTERISTICS



Courtesy: Duracell, Inc., Berkshire Corporate Park, Bethel, CT 06801
<http://www.duracell.com>

Figure 10.2

In order to understand the compatibility issues relating to interfacing ICs operated at different V_{DD} supplies, it is useful to first look at the structure of a typical CMOS logic stage as shown in Figure 10.3.

TYPICAL CMOS IC OUTPUT DRIVER CONFIGURATION

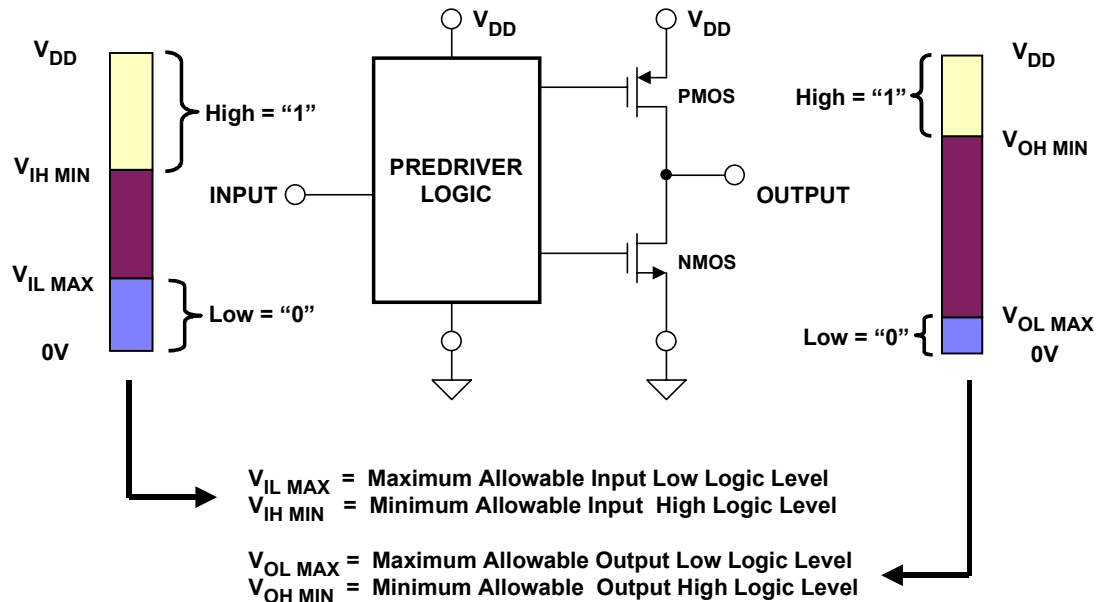


Figure 10.3

Note that the output driver stage consists of a PMOS and an NMOS transistor. When the output is high, the PMOS transistor connects the output to the $+V_{DD}$ supply through its low on-resistance (R_{ON}), and the NMOS transistor is off. When the output is low, the NMOS transistor connects the output to ground through its on-resistance, and the PMOS transistor is off. The R_{ON} of a CMOS output stage can vary between 5Ω and 50Ω depending on the size of the transistors, which in turn, determines the output current drive capability.

A typical logic IC has its power supplies and grounds separated between the output drivers and the rest of the circuitry (including the pre-driver). This is done to maintain a clean power supply, which reduces the effect of noise and ground bounce on the I/O levels. This is increasingly important, since added tolerance and compliance are critical in I/O driver specifications, especially at low voltages.

Figure 10.3 also shows “bars” which define the minimum and maximum required input and output voltages to produce a valid high or low logic level. Note that for CMOS logic, the actual output logic levels are determined by the drive current and the R_{ON} of the transistors. For light loads, the output logic levels are very close to $0V$ and $+V_{DD}$. The input logic thresholds, on the other hand, are determined by the input circuit of the IC.

There are three sections in the “input” bar. The bottom section shows the input range that is interpreted as a logic low. In the case of 5V TTL, this range would be

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between 0V and 0.8V. The middle section shows the input voltage range where it is interpreted as neither a logic low nor a logic high. The upper section shows where an input is interpreted as a logic high. In the case of 5V TTL, this would be between 2V and 5V.

Similarly, there are three sections in the “output” bar. The bottom range shows the allowable voltage for a logic low output. In the case of 5V TTL, the IC must output a voltage between 0V and 0.4V. The middle section shows the voltage range that is not a valid high or low - the device should never transmit a voltage level in this region except when transitioning from one level to the other. The upper section shows the allowable voltage range for a logic high output signal. For 5V TTL, this voltage is between 2.4V and 5V. The chart does not reflect a 10% overshoot/undershoot also allowed on the inputs of the logic standard.

A summary of the existing logic standards using these definitions is shown in Figure 10.4. Note that the input thresholds of classic CMOS logic (series-4000, for example) are defined as $0.3V_{DD}$ and $0.7V_{DD}$. However, most CMOS logic circuits in use today are compatible with TTL and LVTTTL levels which are the dominant 5V and 3.3V operating standards for DSPs. Note that 5V TTL and 3.3V LVTTTL input and output threshold voltages are identical. The difference is the upper range for the allowable high levels.

LOW VOLTAGE LOGIC LEVEL STANDARDS

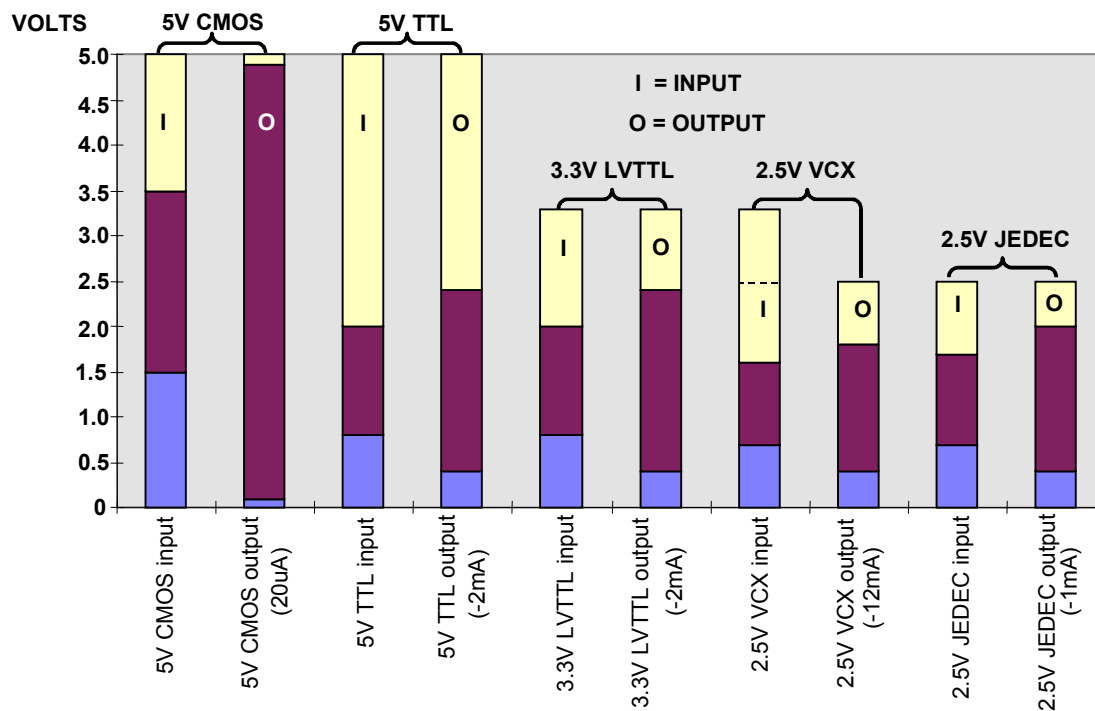


Figure 10.4

The international standards bureau JEDEC (Joint Electron Device Engineering Council) has created a 2.5V standard (JEDEC standard 8-5) which will most likely become the minimum requirement for 2.5V operation (Reference 3). However, there is no current (2000) dominant 2.5V standard for IC transmission and reception, because few manufacturers are making products that operate at this voltage. There is one proposed 2.5V standard created by a consortium of IC manufacturers, titled the Low Voltage Logic Alliance. Their specification provides a guideline for semiconductor operation between 1.8V and 3.6V. A standard covering this voltage range is useful because it ensures present and future compatibility. As an example, the 74VCX164245, a bus translator/transceiver from Fairchild Semiconductor, is designed to be operated anywhere between 1.8V - 3.6V and has different input and output characteristics depending upon the supplied V_{DD} . This standard, named VCX, was formed by Motorola, Toshiba and Fairchild Semiconductor. It currently consists primarily of bus transceivers, translators, FIFOs and other building block logic. There are also a wide range of other low voltage standards, such as GTL (Gunning Transceiver Logic), BTL (Backplane Transceiver Logic), and PECL (PseudoECL Logic). However, most of these standards are aimed at application specific markets and not for general purpose semiconductor systems.

The VCX devices can be operated on a very wide range of voltage levels (1.8V - 3.6V). The I/O characteristics of this standard are dependent upon the V_{DD} voltage and the load on each pin. In Figure 10.4, one voltage (2.5V) was chosen to show the general I/O behavior of a VCX device. Each of the device's output voltages is listed for a specific current. As the current requirements increase, the output high voltage decreases while the output low voltage increases. Please refer to the appropriate data sheets for more specific I/O information.

From this chart, it is possible to visualize some of the possible problems in connecting together two ICs operating on different standards. One example would be connecting a 5V CMOS device to a 3.3V LVTTL IC. The 5V CMOS high level is too high for the LVTTL to handle ($> 3.3V$). This could cause permanent damage to the LVTTL chip. Another possible problem would be a system with a 2.5V JEDEC IC driving a 5V CMOS device. The logic high level from the 2.5V device is not high enough for it to register as a logic high on the 5V CMOS input ($V_{IH\ MIN} = 3.5V$). These examples illustrate two possible types of logic level incompatibilities - either a device being driven with too high a voltage or a device not driving a voltage high enough for it to register a valid high logic level with the receiving IC. These interfacing problems introduce two important concepts: *voltage tolerance* and *voltage compliance*.

VOLTAGE TOLERANCE AND VOLTAGE COMPLIANCE

A device that is *voltage tolerant* can withstand a voltage greater than its V_{DD} on its I/O pins. For example, if a device has a V_{DD} of 2.5V and can accept inputs equal to 3.3V and can withstand 3.3V on its outputs, the 2.5V device is called 3.3V tolerant. The meaning of *input* voltage tolerance is fairly obvious, but the meaning of *output* voltage tolerance requires some explanation. The output of a 2.5V CMOS driver in the high state appears like a small resistor (R_{ON} of the PMOS FET) connected to 2.5V. Obviously, connecting its output directly to 3.3V is likely to destroy the device due to excessive current. However, if the 2.5V device has a three-state output which is connected to a bus which is also driven by a 3.3V IC, then the meaning becomes

clearer. Even though the 2.5V IC is in the off (third-state) condition, the 3.3V IC can drive the bus voltage higher than 2.5V, potentially causing damage to the 2.5V IC output.

A device which is *voltage compliant* can receive signals from and transmit signals to a device which is operated at a voltage greater than its own V_{DD} . For example, if a device has a 2.5V V_{DD} and can transmit and receive signals to and from a 3.3V device, the 2.5V device is said to be 3.3V compliant.

The interface between the 5V CMOS and 3.3V LVTTL parts illustrates a lack of voltage tolerance; the LVTTL IC input is overdriven by the 5V CMOS device output. The interface between the 2.5V JEDEC and the 5V CMOS part demonstrates a lack of voltage compliance; the output high level of the JEDEC IC does not comply to the input level requirement of a the 5V CMOS device.

LOGIC VOLTAGE TOLERANCE AND COMPATIBILITY DEFINITIONS

■ Voltage Tolerance:

- ◆ A device that is *Voltage Tolerant* can *withstand* a voltage greater than its V_{DD} on its input and output pins. If a device has a V_{DD} of 2.5V and can accept inputs of 3.3V ($\pm 10\%$), the 2.5V device is 3.3V tolerant on its input. Input and output tolerance should be examined and specified separately.

■ Voltage Compliance:

- ◆ A device that is *Voltage Compliant* can *transmit and receive* signals to and from logic which is operated at a voltage greater than its own V_{DD} . If a device has a 2.5V V_{DD} and can properly transmit signals to and from 3.3V logic, the 2.5V device is 3.3V compliant. Input and output compliance should be examined and specified separately.

Figure 10.5

INTERFACING 5V TO 3.3V SYSTEMS USING NMOS FET BUS SWITCHES

When combining ICs that operate on different voltage standards, one is often forced to add additional discrete elements to ensure voltage tolerance and compliance. In order to achieve voltage tolerance between 5V and 3.3V logic, for instance, a bus switch voltage translator, or QuickSwitch™ can be used (Reference 4, 5). The bus switch limits the voltage applied to an IC. This is done to avoid applying a larger input high voltage than the receiving device can tolerate.

As an example, it is possible to place a bus switch between a 5V CMOS and 3.3V LVTTL IC, and the two devices can then transmit data properly as shown in Figure 10.6. The bus switch is basically an NMOS FET. If 4.3V is placed on the gate of the FET, the maximum passable signal is 3.3V (approximately 1V less than the gate

voltage). If both input and output are below 3.3V, the NMOS FET acts as a low resistance ($R_{ON} \approx 5\Omega$). As the input approaches 3.3V, the FET on-resistance increases, thereby limiting the signal output. The QuickSwitch contains 10 bi-directional FETs with a gate drive enable as shown in Figure 10.6. The V_{CC} of the QuickSwitch sets the high level for the gate drive.

One way of creating a 4.3V supply on a 5V/3.3V system board is to place a diode between the 5V supply and V_{CC} on the QuickSwitch. In Figure 10.6, the 4.3V is generated by a silicon diode in series with a Schottky diode connected to the 3.3V supply. With 10% tolerances on both 5V and 3.3V supplies, this method produces a more stable gate bias voltage. Some bus switches are designed to operate on either 3.3V or 5V directly and generate the internal gate bias level internally.

A QuickSwitch removes voltage tolerance concerns in this mixed logic design. One convenient feature of bus switches is that they are bi-directional; this allows the designer to place a bus translator between two ICs and not have to create additional routing logic for input and output signals.

+3.3V / +5V BIDIRECTIONAL INTERFACE USING NMOS FET ACHIEVES VOLTAGE TOLERANCE

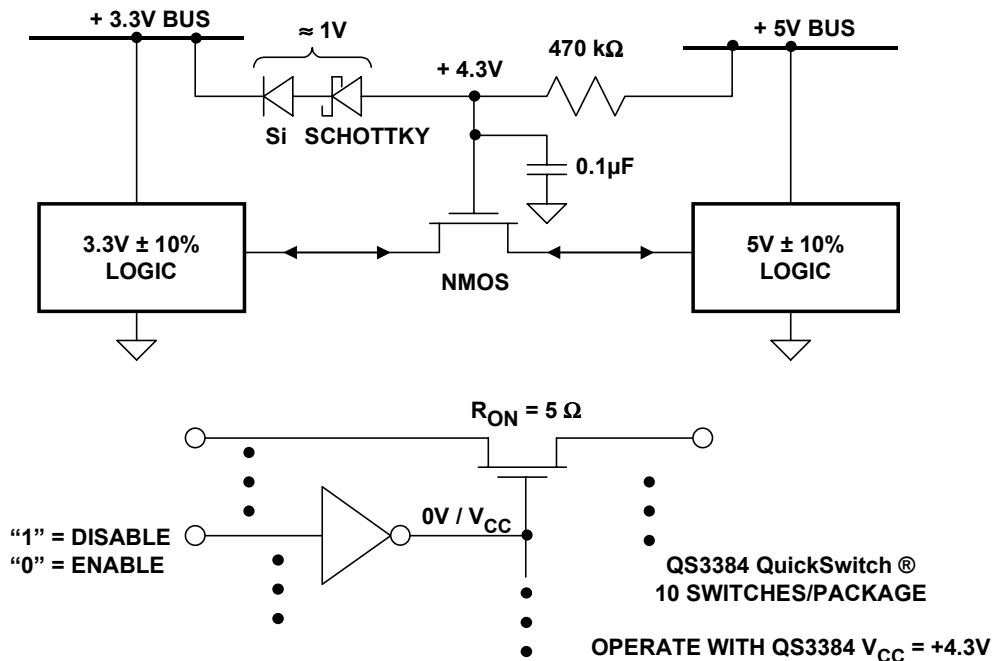
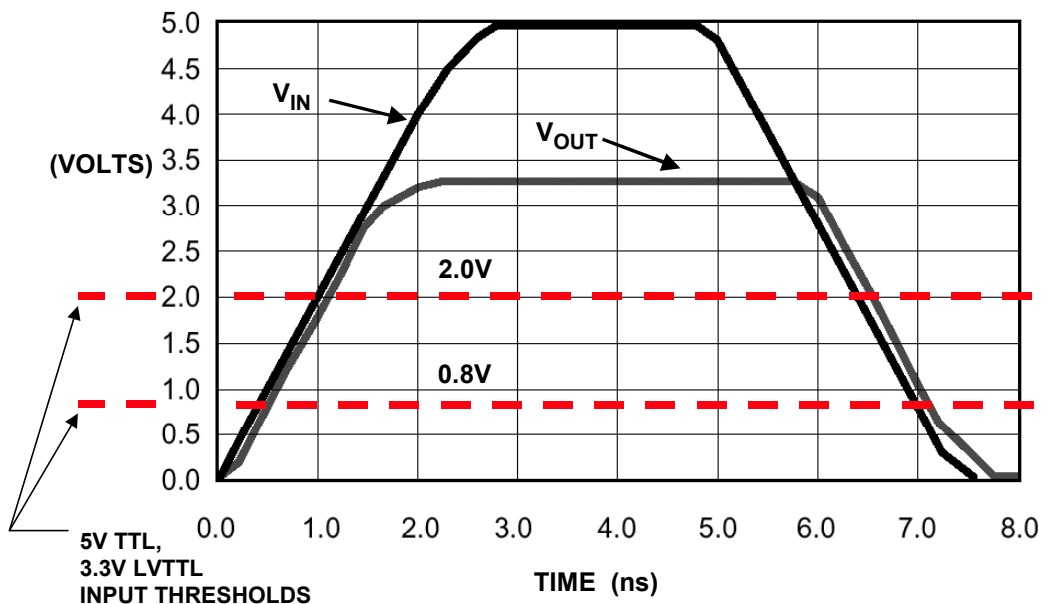


Figure 10.6

A bus switch increases the total power dissipation along with the total area required to layout a system. Since voltage bus switches are typically CMOS circuits, they have very low power dissipation ratings. An average value for added continuous power dissipation is 5mW per package (10 switches), and this is independent of the frequency of signals which pass through the circuit. Bus switches typically have 8 - 20 I/O pins per package and take up approximately 25 to 50mm² of board space.

One concern when adding interface logic into a circuit is a possible increase in propagation delay. Added propagation delay can create many timing problems in a design. QuickSwitches have very low propagation delay values ($< 0.25\text{ns}$) as shown in Figure 10.7.

QS3384 QuickSwitch® TRANSIENT RESPONSE WITH +4.3V SUPPLY



Courtesy: Integrated Device Technology (IDT), Inc., 2975 Stender Way, Santa Clara, CA 95054
<http://www.idt.com>

Figure 10.7

INTERNALLY CREATED VOLTAGE TOLERANCE / COMPLIANCE

The requirement for low power, high performance ICs has triggered a race among manufacturers to design devices operating at and below 2.5V that are also TTL/CMOS compatible. Figure 10.8 is a block diagram of a logic circuit that allows the logic core to operate at a reduced voltage, while the output driver operates at a standard supply voltage level of 3.3V, for example.

The technique followed by many IC manufacturers is to provide a secondary I/O ring, i.e., the I/O drivers in a 2.5V IC are driven by a 3.3V power supply, hence the device can be TTL compatible and meet the specification for V_{OH} and V_{OL} . The 3.3V external power supply is *required* for the part to be 3.3V tolerant. This causes the added complexity of two power supplies for the chip which have to be maintained in all future plug-in generations of the IC.

A more flexible technique (used in the ADSP-218xM series DSPs) is to provide a separate I/O ring with an external voltage with the option of setting that voltage equal to the core's operating voltage, if desired. This design can provide tolerance to 3.3V with the external voltage set to 2.5V, or 3.3V tolerance and compliance to 3.3V with the external voltage set to 3.3V. There are vendors today that use this option partially, i.e., the VCX devices are 3.3V tolerant at 2.5V internal and external voltages, but do not have the option of 3.3V compliance. Other existing designs and patents that address this issue do not support complete tolerance and compliance and the low standby current specification. This approach is complicated, since the circuits must meet the noise and power requirements with the external voltages at 3.3V or 2.5V.

CMOS IC WITH SECONDARY I/O RING

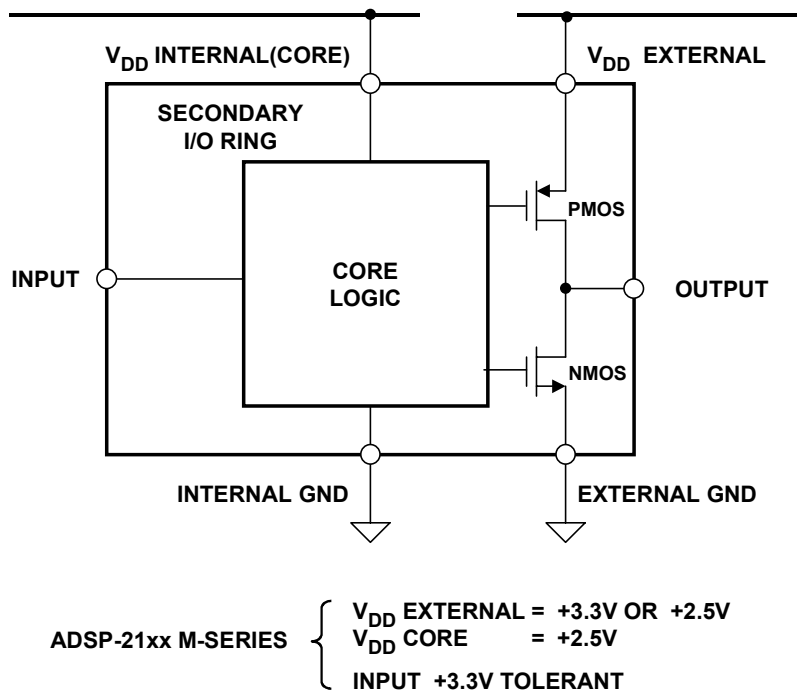


Figure 10.8

There are several issues to consider in a dual-supply logic IC design:

- *Power-Up Sequencing:* If two power supplies are required to give an IC additional tolerance / compliance, what is the power-up sequence? Is it a requirement that the power supplies are switched on simultaneously or can the device only have a voltage supplied on the core or only on the I/O ring?

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- *Process Support and Electro-Static Discharge (ESD) Protection:* The transistors created in the IC's fabrication process must be able to both withstand and drive high voltages. The high voltage transistors create additional fabrication costs since they require more processing steps to build in high voltage tolerance. Designs with standard transistors require additional circuitry. The I/O drivers must also provide ESD protection for the device. Most current designs limit the overvoltage to below one diode drop (0.7V) above the power supply. Protection for larger overvoltage requires more diodes in series.
- *Internal High Voltage Generation:* The PMOS transistors need to be placed in a substrate well which is tied to the highest on-chip voltage to prevent lateral diodes from turning on and drawing excessive current. This high voltage can either be generated on chip using charge pumps or from an external supply. This requirement can make the design complex, since one cannot efficiently use charge pumps to generate higher voltages and also achieve low standby current.
- *Chip Area:* Die size is a primary factor in reducing costs and increasing yields. Tolerance and compliance circuitry may require either more or larger I/O devices to achieve the desired performance levels.
- *Testing:* Since the core and the I/O can be at different voltages, testing the device for all possible combinations of voltages can be complicated, adding to the total cost of the IC.

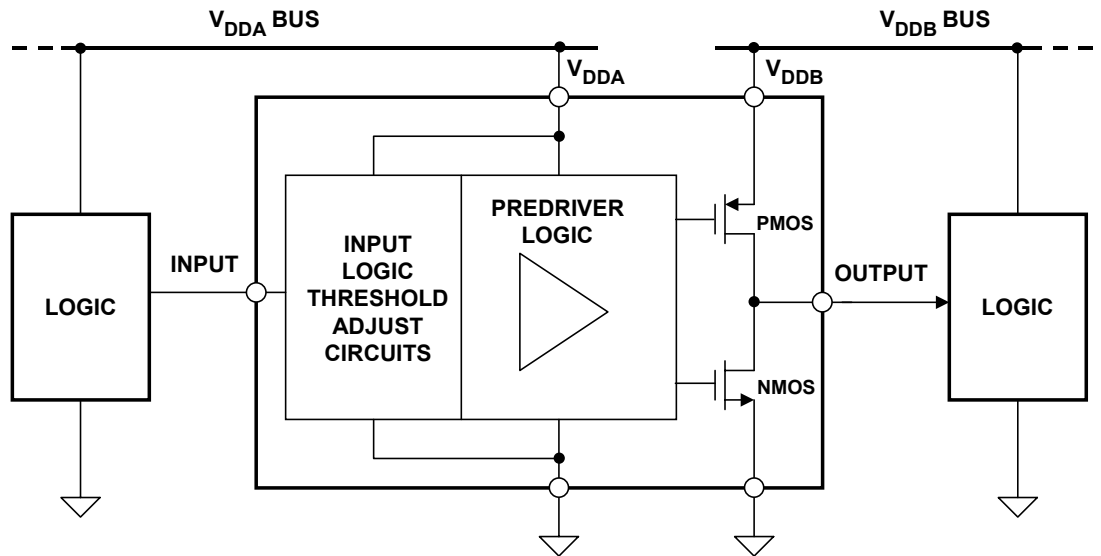
3.3V / 2.5V INTERFACES

The Fairchild 74VCX164245-series are low voltage 16-bit dual supply logic translators/transceivers with three-state outputs. A simplified block diagram is shown in Figure 10.9. These devices use the VCX low voltage standard previously discussed. The output driver circuit is supplied from the V_{DDB} power supply bus, ensuring V_{DDB} compliant and tolerant outputs. The input circuit is supplied from the V_{DDA} supply, and the input logic threshold adjust circuits optimize the input logic thresholds for the particular value of V_{DDA} . Figure 10.10 shows the VCX voltage standards for 3.3V, 2.5V, and 1.8V supply voltages. Note that the input voltage is 3.3V tolerant for all three supply voltages.

These devices dissipate about 2mW per input/output and are packaged in a 48-lead TSSOP with a 2.5V supply. Propagation delay is about 3.2ns.

Figure 10.11 shows two possibilities for a 3.3V to 2.5V logic interface. The top diagram (A) shows a direct connection. This will work provided the 2.5V IC is 3.3V tolerant on its input. If the 2.5V IC is not 3.3V tolerant, the VCX translator can be used as shown in Figure 10.11B.

LOGIC TRANSLATING TRANSCEIVER (FAIRCHILD 74VCX164245)



- 74VCX164245 CHARACTERISTICS:**
- Power Dissipation = 2mW / Input or Output
 - 16-bits per 48-lead TSSOP 100mm² package
 - 3.2ns Propagation Delay at +2.5V

Figure 10.9

VOLTAGE COMPLIANCE FOR VCX STANDARD (FAIRCHILD 74VCX164245 TRANSLATOR)

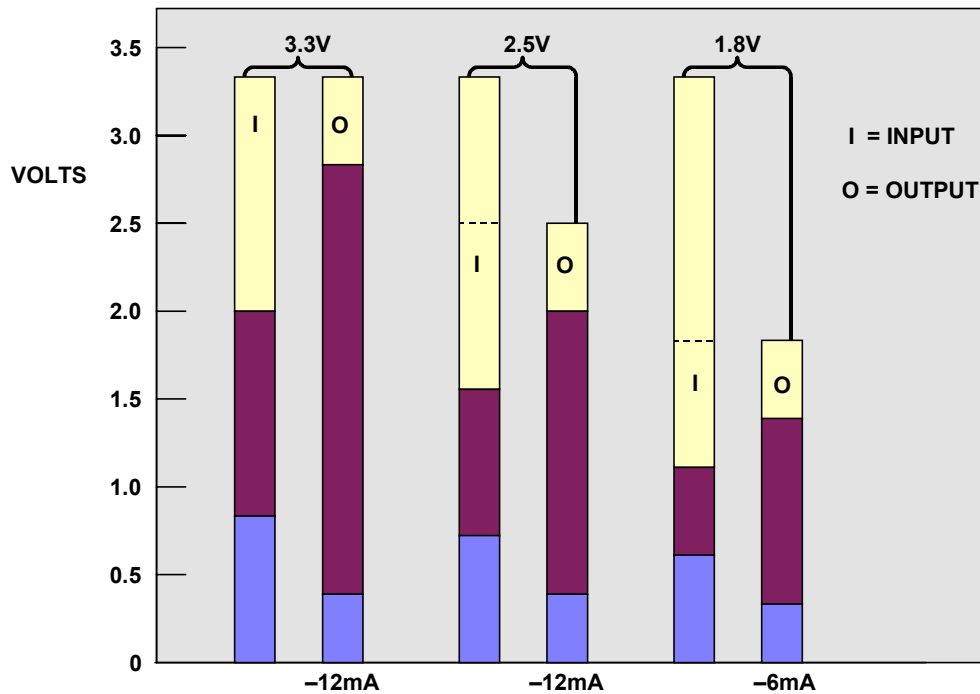


Figure 10.10

+3.3V TO +2.5V INTERFACE

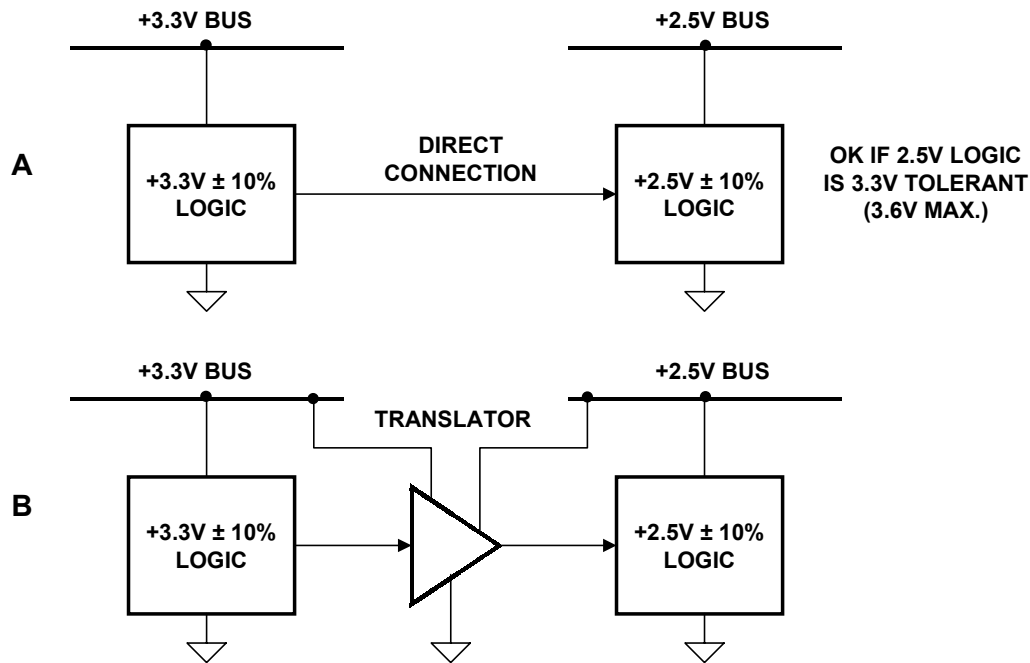


Figure 10.11

Figure 10.12A shows a direct connection between 2.5V and 3.3V logic. In order for this to work, the 2.5V output must be at least 2V minimum. With no loading on the 2.5V output, the 3.3V IC input is connected directly to +2.5V through the on-resistance of the PMOS transistor driver. This provides 0.5V noise margin for the nominal supply voltage of 2.5V. However, the 10% tolerance on the 2.5V bus allows it to drop to a minimum of 2.25V, and the noise margin is reduced to 0.25V. This may still work in a relatively quiet environment, but could be marginal if there is noise on the supply voltages.

Adding a 1.6kΩ pull-up resistor as shown in Figure 10.12B ensures the 2.5V output will not drop below 2.5V due to the input current of the 3.3V device, but the degraded noise margin still exists for a 2.25V supply. With a 50% duty cycle, the resistor adds about 3.4mW power dissipation per output.

A more reliable interface between 2.5V and 3.3V logic is shown in Figure 10.12C, where a VCX translator is used. This solves all noise margin problems associated with (A) and (B) and requires about 2mW per output.

+2.5V TO +3.3V INTERFACE

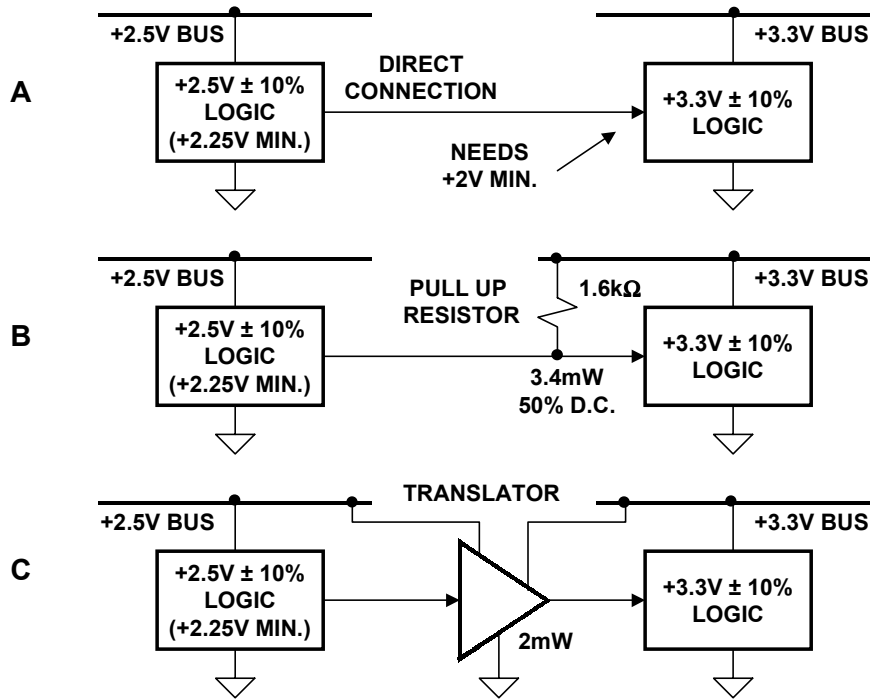


Figure 10.12

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GROUNDING IN MIXED SIGNAL SYSTEMS

Walt Kester, James Bryant, Mike Byrne

Today's signal processing systems generally require mixed-signal devices such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) as well as fast digital signal processors (DSPs). Requirements for processing analog signals having wide dynamic ranges increases the importance of high performance ADCs and DACs. Maintaining wide dynamic range with low noise in hostile digital environments is dependent upon using good high-speed circuit design techniques including proper signal routing, decoupling, and grounding.

In the past, "high precision, low-speed" circuits have generally been viewed differently than so-called "high-speed" circuits. With respect to ADCs and DACs, the sampling (or update) frequency has generally been used as the distinguishing speed criteria. However, the following two examples show that in practice, most of today's signal processing ICs are really "high-speed," and must therefore be treated as such in order to maintain high performance. This is certainly true of DSPs, and also true of ADCs and DACs.

All sampling ADCs (ADCs with an internal sample-and-hold circuit) suitable for signal processing applications operate with relatively high speed clocks with fast rise and fall times (generally a few nanoseconds) and must be treated as high speed devices, even though throughput rates may appear low. For example, the 12-bit AD7892 successive approximation (SAR) ADC operates on an 8MHz internal clock, while the sampling rate is only 600kSPS.

Sigma-delta (Σ - Δ) ADCs also require high speed clocks because of their high oversampling ratios. The AD7722 16-bit ADC has an output data rate (effective sampling rate) of 195kSPS, but actually samples the input signal at 12.5MSPS (64-times oversampling). Even high resolution, so-called "low frequency" Σ - Δ industrial measurement ADCs (having throughputs of 10Hz to 7.5kHz) operate on 5MHz or higher clocks and offer resolution to 24-bits (for example, the Analog Devices AD7730 and AD7731).

To further complicate the issue, mixed-signal ICs have both analog and digital ports, and because of this, much confusion has resulted with respect to proper grounding techniques. In addition, some mixed-signal ICs have relatively low digital currents, while others have high digital currents. In many cases, these two types must be treated differently with respect to optimum grounding.

Digital and analog design engineers tend to view mixed-signal devices from different perspectives, and the purpose of this section is to develop a general grounding philosophy that will work for most mixed signal devices, without having to know the specific details of their internal circuits.

GROUND AND POWER PLANES

The importance of maintaining a low impedance large area ground plane is critical to all analog circuits today. The ground plane not only acts as a low impedance return path for decoupling high frequency currents (caused by fast digital logic) but

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also minimizes EMI/RFI emissions. Because of the shielding action of the ground plane, the circuit's susceptibility to external EMI/RFI is also reduced.

Ground planes also allow the transmission of high speed digital or analog signals using transmission line techniques (microstrip or stripline) where controlled impedances are required.

The use of "buss wire" is totally unacceptable as a "ground" because of its impedance at the equivalent frequency of most logic transitions. For instance, #22 gauge wire has about 20nH/inch inductance. A transient current having a slew rate of 10mA/ns created by a logic signal would develop an unwanted voltage drop of 200mV at this frequency flowing through 1 inch of this wire:

$$\Delta v = L \frac{\Delta i}{\Delta t} = 20\text{nH} \times \frac{10\text{mA}}{\text{ns}} = 200\text{mV}.$$

For a signal having a 2V peak-to-peak range, this translates into an error of about 200mV, or 10% (approximate 3.5-bit accuracy). Even in all-digital circuits, this error would result in considerable degradation of logic noise margins.

Figure 10.13 shows an illustration of a situation where the digital return current modulates the analog return current (top figure). The ground return wire inductance and resistance is shared between the analog and digital circuits, and this is what causes the interaction and resulting error. A possible solution is to make the digital return current path flow directly to the GND REF as shown in the bottom figure. This is the fundamental concept of a "star," or single-point ground system. Implementing the true single-point ground in a system which contains multiple high frequency return paths is difficult because the physical length of the individual return current wires will introduce parasitic resistance and inductance which can make obtaining a low impedance high frequency ground difficult. In practice, the current returns must consist of large area ground planes for low impedance to high frequency currents. Without a low-impedance ground plane, it is therefore almost impossible to avoid these shared impedances, especially at high frequencies.

All integrated circuit ground pins should be soldered directly to the low-impedance ground plane to minimize series inductance and resistance. The use of traditional IC sockets is not recommended with high-speed devices. The extra inductance and capacitance of even "low profile" sockets may corrupt the device performance by introducing unwanted shared paths. If sockets must be used with DIP packages, as in prototyping, individual "pin sockets" or "cage jacks" may be acceptable. Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6). They have spring-loaded gold contacts which make good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade their performance.

Power supply pins should be decoupled directly to the ground plane using low inductance ceramic surface mount capacitors. If through-hole mounted ceramic capacitors must be used, their leads should be less than 1mm. The ceramic capacitors should be located as close as possible to the IC power pins. Ferrite beads may be also required for additional decoupling.

DIGITAL CURRENTS FLOWING IN ANALOG RETURN PATH CREATE ERROR VOLTAGES

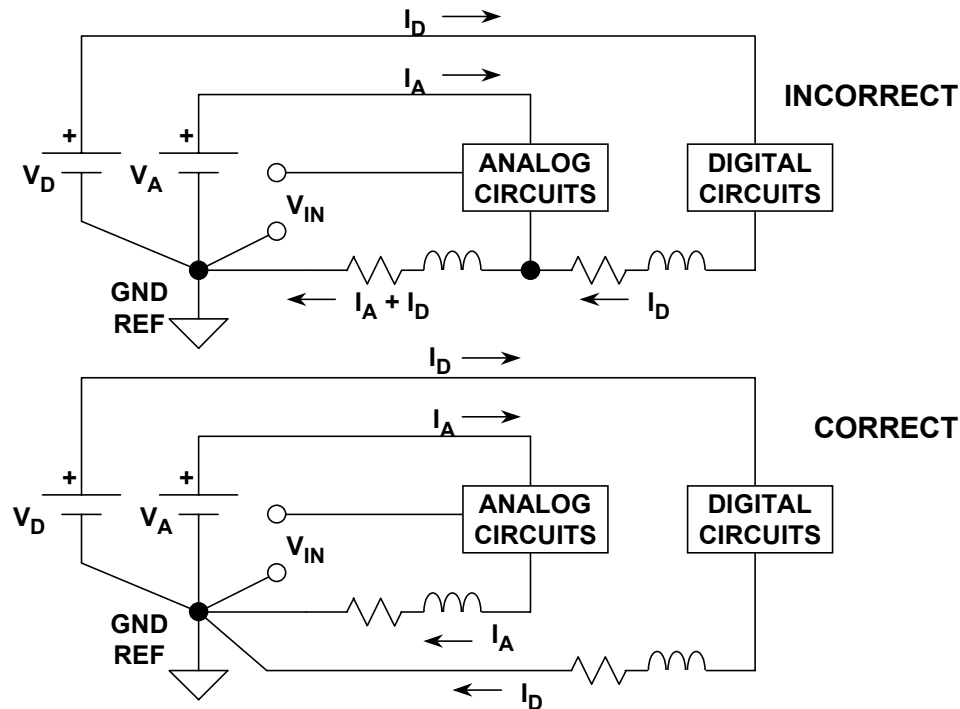


Figure 10.13

DOUBLE-SIDED VS. MULTILAYER PRINTED CIRCUIT BOARDS

Each PCB in the system should have at least one complete layer dedicated to the ground plane. Ideally, a double-sided board should have one side completely dedicated to ground and the other side for interconnections. In practice, this is not possible, since some of the ground plane will certainly have to be removed to allow for signal and power crossovers, vias, and through-holes. Nevertheless, as much area as possible should be preserved, and at least 75% should remain. After completing an initial layout, the ground layer should be checked carefully to make sure there are no isolated ground "islands," because IC ground pins located in a ground "island" have no current return path to the ground plane. Also, the ground plane should be checked for "skinny" connections between adjacent large areas which may significantly reduce the effectiveness of the ground plane. Needless to say, auto-routing board layout techniques will generally lead to a layout disaster on a mixed-signal board, so manual intervention is highly recommended.

Systems that are densely packed with surface mount ICs will have a large number of interconnections; therefore multilayer boards are mandatory. This allows at least one complete layer to be dedicated to ground. A simple 4-layer board would have internal ground and power plane layers with the outer two layers used for

interconnections between the surface mount components. Placing the power and ground planes adjacent to each other provides additional inter-plane capacitance which helps high frequency decoupling of the power supply. In most systems, 4-layers are not enough, and additional layers are required for routing signals as well as power.

GROUND PLANES ARE MANDATORY!

- **Use Large Area Ground (and Power) Planes for Low Impedance Current Return Paths (Must Use at Least a Double-Sided Board!)**
- **Double-Sided Boards:**
 - ◆ **Avoid High-Density Interconnection Crossovers and Vias Which Reduce Ground Plane Area**
 - ◆ **Keep > 75% Board Area on One Side for Ground Plane**
- **Multilayer Boards: Mandatory for Dense Systems**
 - ◆ **Dedicate at Least One Layer for the Ground Plane**
 - ◆ **Dedicate at Least One Layer for the Power Plane**
- **Use at Least 30% to 40% of PCB Connector Pins for Ground**
- **Continue the Ground Plane on the Backplane Motherboard to Power Supply Return**

Figure 10.14

MULTICARD MIXED-SIGNAL SYSTEMS

The best way of minimizing ground impedance in a multocard system is to use a "motherboard" PCB as a backplane for interconnections between cards, thus providing a continuous ground plane to the backplane. The PCB connector should have at least 30-40% of its pins devoted to ground, and these pins should be connected to the ground plane on the backplane mother card. To complete the overall system grounding scheme there are two possibilities:

1. The backplane ground plane can be connected to chassis ground at numerous points, thereby diffusing the various ground current return paths. This is commonly referred to as a "multipoint" grounding system and is shown in Figure 10.15.
2. The ground plane can be connected to a single system "star ground" point (generally at the power supply).

MULTIPOINT GROUND CONCEPT

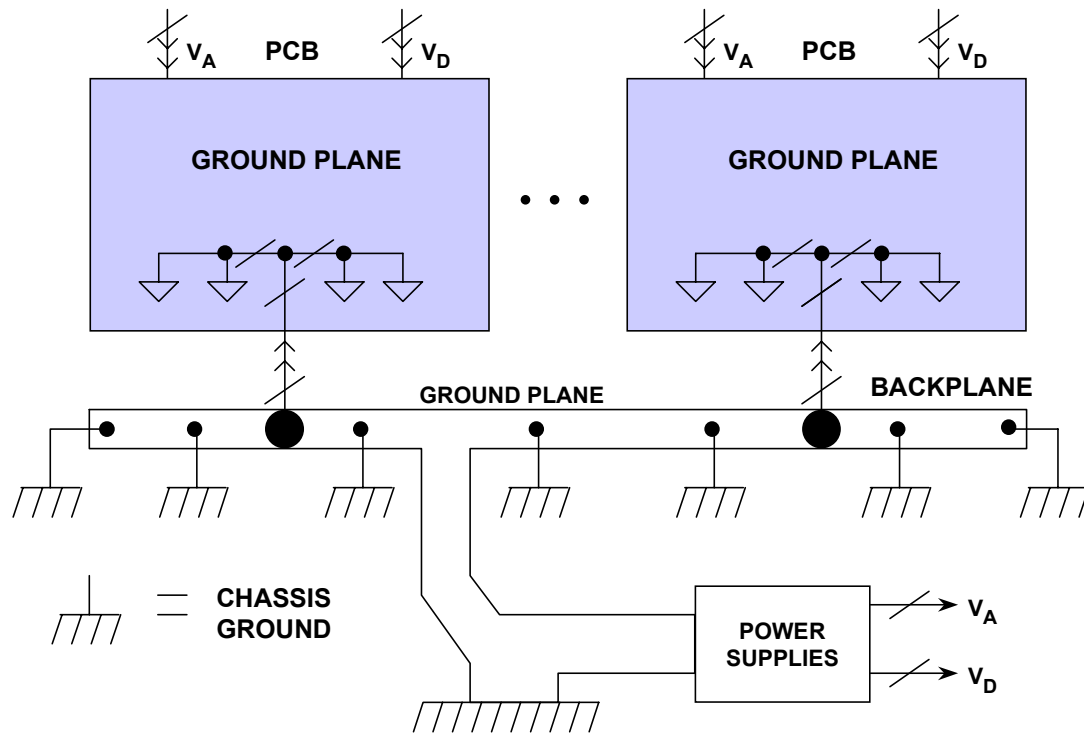


Figure 10.15

The first approach is most often used in all-digital systems, but can be used in mixed-signal systems provided the ground currents due to digital circuits are sufficiently low and diffused over a large area. The low ground impedance is maintained all the way through the PC boards, the backplane, and ultimately the chassis. However, it is critical that good electrical contact be made where the grounds are connected to the sheet metal chassis. This requires self-tapping sheet metal screws or "biting" washers. Special care must be taken where anodized aluminum is used for the chassis material, since its surface acts as an insulator.

The second approach ("star ground") is often used in high speed mixed-signal systems having separate analog and digital ground systems and warrants further discussion.

SEPARATING ANALOG AND DIGITAL GROUNDS

In mixed-signal systems with large amounts of digital circuitry, it is highly desirable to *physically* separate sensitive analog components from noisy digital components. It may also be beneficial to use separate ground planes for the analog and the digital circuitry. These planes should not overlap in order to minimize capacitive coupling between the two. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the

connector ground pins. The arrangement shown in Figure 10.16 illustrates that the two planes are kept separate all the way back to a common system "star" ground, generally located at the power supplies. The connections between the ground planes, the power supplies, and the "star" should be made up of multiple bus bars or wide copper braids for minimum resistance and inductance. The back-to-back Schottky diodes on each PCB are inserted to prevent accidental DC voltage from developing between the two ground systems when cards are plugged and unplugged. This voltage should be kept less than 300mV to prevent damage to ICs which have connections to both the analog and digital ground planes. Schottky diodes are preferable because of their low capacitance and low forward voltage drop. The low capacitance prevents AC coupling between the analog and digital ground planes. Schottky diodes begin to conduct at about 300mV, and several parallel diodes in parallel may be required if high currents are expected. In some cases, ferrite beads can be used instead of Schottky diodes, however they introduce DC ground loops which can be troublesome in precision systems.

SEPARATING ANALOG AND DIGITAL GROUND PLANES

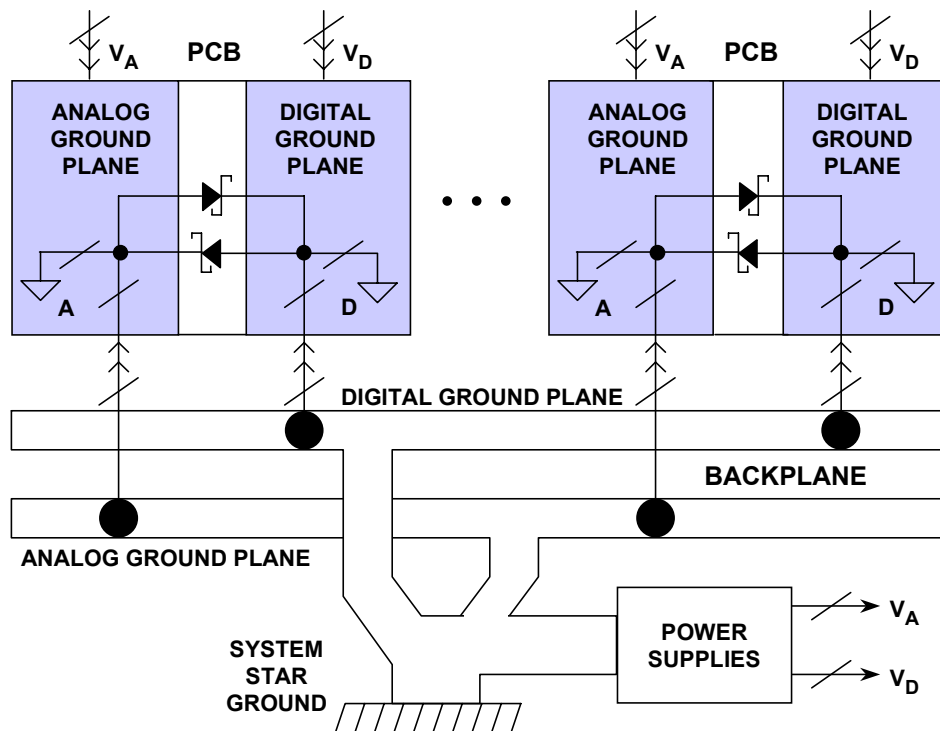


Figure 10.16

It is mandatory that the impedance of the ground planes be kept as low as possible, all the way back to the system star ground. DC or AC voltages of more than 300mV between the two ground planes can not only damage ICs but cause false triggering of logic gates and possible latching.

GROUNDING AND DECOUPLING MIXED-SIGNAL ICs WITH LOW DIGITAL CURRENTS

Sensitive analog components such as amplifiers and voltage references are always referenced and decoupled to the analog ground plane. *The ADCs and DACs (and other mixed-signal ICs) with low digital currents should generally be treated as analog components and also grounded and decoupled to the analog ground plane.* At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually has pins designated as *analog ground* (AGND) and *digital ground* (DGND). The diagram shown in Figure 10.17 will help to explain this seeming dilemma.

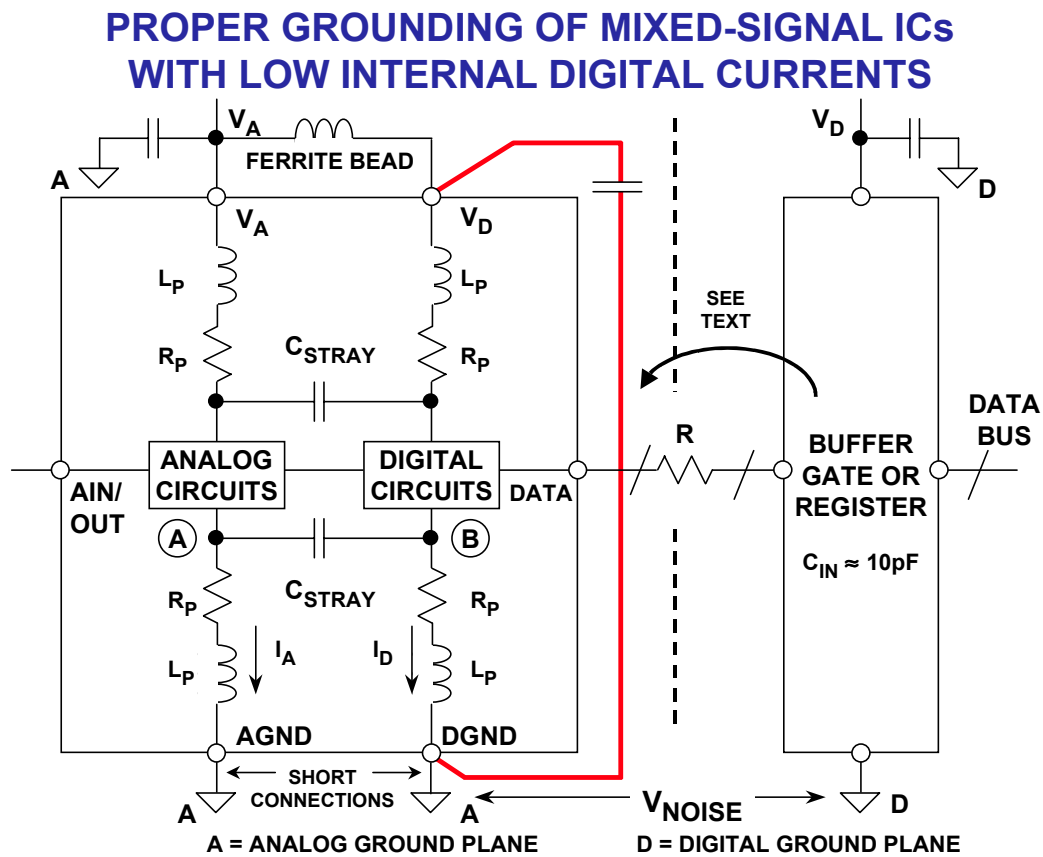


Figure 10.17

HARDWARE DESIGN TECHNIQUES

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 10.17 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the bond pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY} . In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance. *Note that connecting DGND to the digital ground plane applies V_{NOISE} across the AGND and DGND pins and invites disaster!*

The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system.

It is true that this arrangement may inject a small amount of digital noise onto the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter output does not drive a large fanout (they normally can't, by design). Minimizing the fanout on the converter's digital port will also keep the converter logic transitions relatively free from ringing and minimize digital switching currents, and thereby reducing any potential coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead as shown in Figure 10.17. The internal transient digital currents of the converter will flow in the small loop from V_D through the decoupling capacitor and to DGND (this path is shown with a heavy line on the diagram). The transient digital currents will therefore not appear on the external analog ground plane, but are confined to the loop. The V_D pin decoupling capacitor should be mounted as close to the converter as possible to minimize parasitic inductance. These decoupling capacitors should be low inductance ceramic types, typically between 0.01 μ F and 0.1 μ F.

TREAT THE ADC DIGITAL OUTPUTS WITH CARE

It is always a good idea (as shown in Figure 10.17) to place a buffer register adjacent to the converter to isolate the converter's digital lines from noise on the data bus. The register also serves to minimize loading on the digital outputs of the converter and acts as a Faraday shield between the digital outputs and the data bus. Even though many converters have three-state outputs/inputs, this isolation register still represents good design practice. In some cases it may be desirable to

add an additional buffer register on the analog ground plane next to the converter output to provide greater isolation.

The series resistors (labeled "R" in Figure 10.17) between the ADC output and the buffer register input help to minimize the digital transient currents which may affect converter performance. The resistors isolate the digital output drivers from the capacitance of the buffer register inputs. In addition, the RC network formed by the series resistor and the buffer register input capacitance acts as a lowpass filter to slow down the fast edges.

A typical CMOS gate combined with PCB trace and a through-hole will create a load of approximately 10pF. A logic output slew rate of 1V/ns will produce 10mA of dynamic current if there is no isolation resistor:

$$\Delta I = C \frac{\Delta v}{\Delta t} = 10\text{pF} \times \frac{1\text{V}}{\text{ns}} = 10\text{mA} .$$

A 500Ω series resistors will minimize this output current and result in a rise and fall time of approximately 11ns when driving the 10pF input capacitance of the register:

$$t_r = 2.2 \times \tau = 2.2 \times R \cdot C = 2.2 \times 500\Omega \times 10\text{pF} = 11\text{ns}.$$

TTL registers should be avoided, since they can appreciably add to the dynamic switching currents because of their higher input capacitance.

The buffer register and other digital circuits should be grounded and decoupled to the *digital* ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter. The analog ground plane will generally not be very noisy, but if the noise on the digital ground plane (relative to the analog ground plane) exceeds a few hundred millivolts, then steps should be taken to reduce the digital ground plane impedance, thereby maintaining the digital noise margins at an acceptable level. Under no circumstances should the voltage between the two ground planes exceed 300mV, or the ICs may be damaged.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane as shown in Figure 10.18. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

In some cases it may not be possible to connect V_D to the analog supply. Some of the newer, high speed ICs may have their analog circuits powered by +5V, but the digital interface powered by +3V to interface to 3V logic. In this case, the +3V pin of the IC should be decoupled directly to the analog ground plane. It is also advisable to connect a ferrite bead in series with the power trace that connects the pin to the +3V digital logic supply.

GROUNDING AND DECOUPLING POINTS

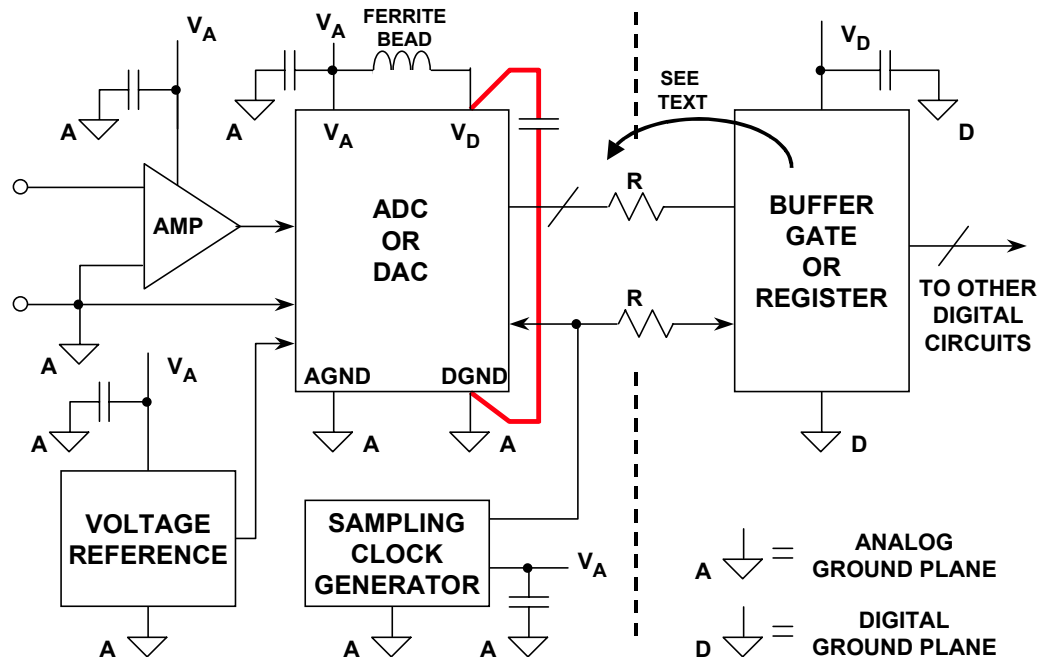


Figure 10.18

The sampling clock generation circuitry should be treated like analog circuitry and also be grounded and heavily-decoupled to the analog ground plane. Phase noise on the sampling clock produces degradation in system SNR as will be discussed shortly.

SAMPLING CLOCK CONSIDERATIONS

In a high performance sampled data system a low phase-noise crystal oscillator should be used to generate the ADC (or DAC) sampling clock because sampling clock jitter modulates the analog input/output signal and raises the noise and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.

The effect of sampling clock jitter on ADC Signal-to-Noise Ratio (SNR) is given approximately by the equation:

$$\text{SNR} = 20 \log_{10} \left[\frac{1}{2\pi f t_j} \right],$$

where SNR is the SNR of a perfect ADC of infinite resolution where the only source of noise is that caused by the RMS sampling clock jitter, t_j . Note that f in the above equation is the analog input frequency. Just working through a simple example, if $t_j = 50\text{ps}$ RMS, $f = 100\text{kHz}$, then $\text{SNR} = 90\text{dB}$, equivalent to about 15-bits dynamic range.

It should be noted that t_j in the above example is the root-sum-square (RSS) value of the external clock jitter *and* the internal ADC clock jitter (called aperture jitter). However, in most high performance ADCs, the internal aperture jitter is negligible compared to the jitter on the sampling clock.

Since degradation in SNR is primarily due to external clock jitter, steps must be taken to ensure the sampling clock is as noise-free as possible and has the lowest possible phase jitter. This requires that a crystal oscillator be used. There are several manufacturers of small crystal oscillators with low jitter (less than 5ps RMS) CMOS compatible outputs. (For example, MF Electronics, 10 Commerce Dr., New Rochelle, NY 10801, Tel. 914-576-6570.)

Ideally, the sampling clock crystal oscillator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multi-purpose system clock which is generated on the digital ground plane. It must then pass from its origin on the digital ground plane to the ADC on the analog ground plane. Ground noise between the two planes adds directly to the clock signal and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics. This can be remedied somewhat by transmitting the sampling clock signal as a differential signal using either a small RF transformer as shown in Figure 10.19 or a high speed differential driver and receiver IC. If an active differential driver and receiver are used, they should be ECL to minimize phase jitter. In a single +5V supply system, ECL logic can be connected between ground and +5V (PECL), and the outputs AC coupled into the ADC sampling clock input. In either case, the original master system clock must be generated from a low phase noise crystal oscillator.

SAMPLING CLOCK DISTRIBUTION FROM DIGITAL TO ANALOG GROUND PLANES

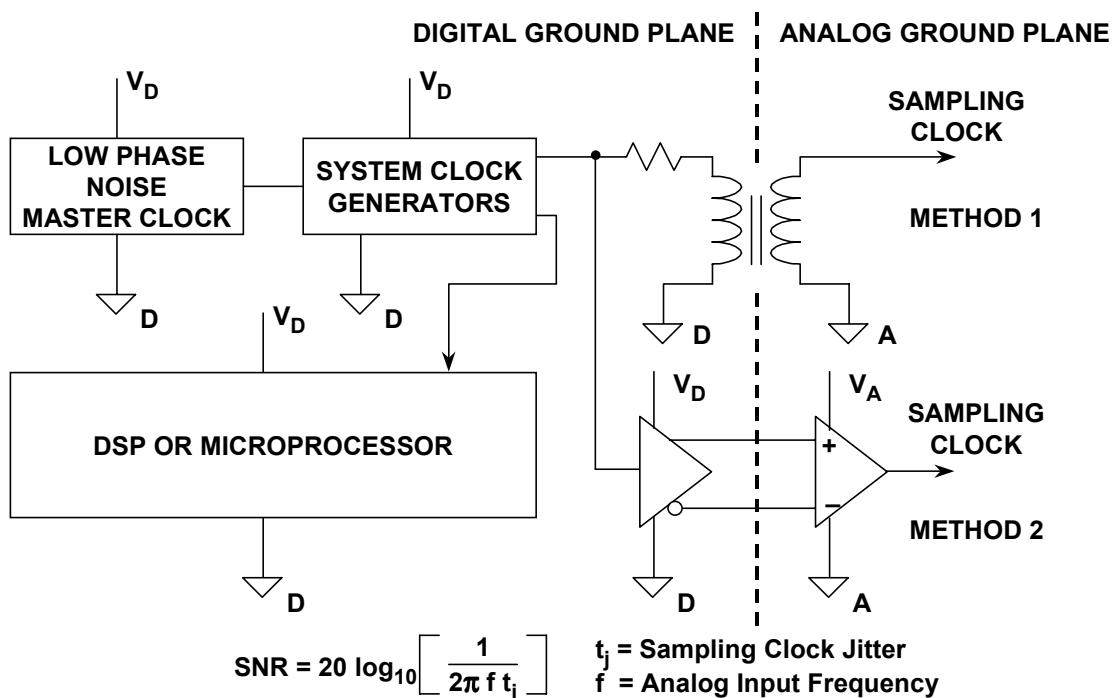


Figure 10.19

THE ORIGINS OF THE CONFUSION ABOUT MIXED-SIGNAL GROUNDING: APPLYING SINGLE-CARD GROUNDING CONCEPTS TO MULTICARD SYSTEMS

Most ADC, DAC, and other mixed-signal device data sheets discuss grounding relative to a single PCB, usually the manufacturer's own evaluation board. This has been a source of confusion when trying to apply these principles to multichip or multi-ADC/DAC systems. The recommendation is usually to split the PCB ground plane into an analog plane and a digital plane. It is then further recommended that the AGND and DGND pins of a converter be tied together and that the analog ground plane and digital ground planes be connected at that same point as shown in Figure 10.20. This essentially creates the system "star" ground at the mixed-signal device.

All noisy digital currents flow through the digital power supply to the digital ground plane and back to the digital supply; they are isolated from the sensitive analog portion of the board. The system star ground occurs where the analog and digital ground planes are joined together at the mixed signal device. While this approach will generally work in a simple system with a single PCB and single ADC/DAC, it is not optimum for multichip mixed-signal systems. In systems having several ADCs or DACs on different PCBs (or on the same PCB, for that matter), the analog and digital ground planes become connected at several points, creating the possibility of ground loops and making a single-point "star" ground system impossible. For these reasons, this grounding approach is not recommended for multichip systems, and

the approach previously discussed should be used for mixed signal ICs with low digital currents.

**GROUNDING MIXED SIGNAL ICs : SINGLE PC BOARD
(TYPICAL EVALUATION/TEST BOARD)**

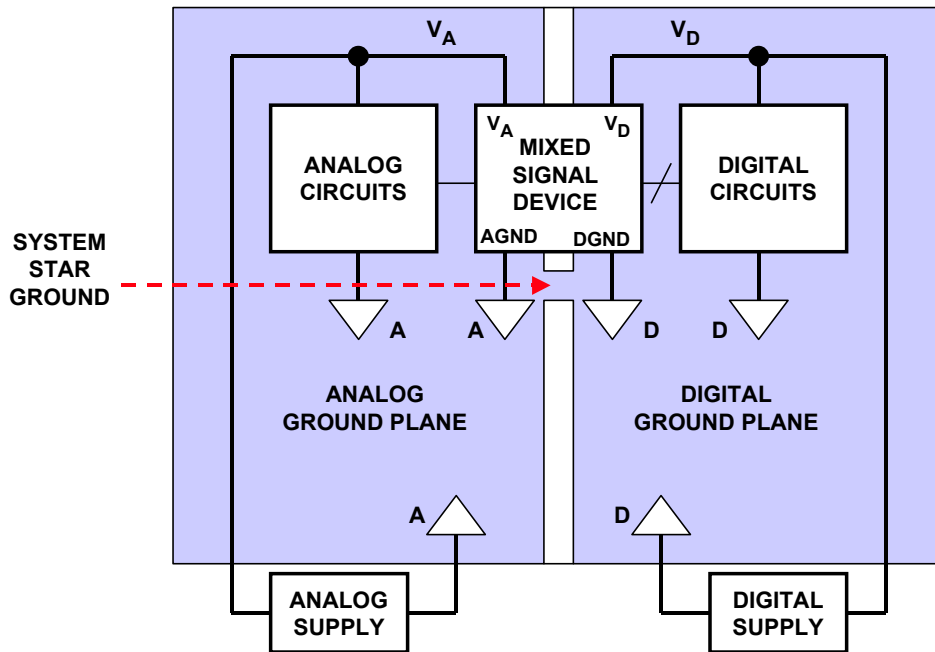


Figure 10.20

SUMMARY: GROUNDING MIXED SIGNAL DEVICES WITH LOW DIGITAL CURRENTS IN A MULTICARD SYSTEM

Figure 10.21 summarizes the approach previously described for grounding a mixed signal device which has low digital currents. The analog ground plane is not corrupted because the small digital transient currents flow in the small loop between V_D , the decoupling capacitor, and DGND (shown as a heavy line). The mixed signal device is for all intents and purposes treated as an analog component. The noise V_N between the ground planes reduces the noise margin at the digital interface but is generally not harmful if kept less than 300mV by using a low impedance digital ground plane all the way back to the system star ground.

However, mixed signal devices such as sigma-delta ADCs, codecs, and DSPs with on-chip analog functions are becoming more and more digitally intensive. Along with the additional digital circuitry come larger digital currents and noise. For example, a sigma-delta ADC or DAC contains a complex digital filter which adds considerably to the digital current in the device. The method previously discussed depends on the decoupling capacitor between V_D and DGND to keep the digital transient currents and isolated in a small loop. However, if the digital currents are

significant enough and have components at DC or low frequencies, the decoupling capacitor may have to be so large that it is impractical. Any digital current which flows outside the loop between V_D and DGND must flow through the analog ground plane. This may degrade performance, especially in high resolution systems.

GROUNDING MIXED SIGNAL ICs WITH LOW INTERNAL DIGITAL CURRENTS: MULTIPLE PC BOARDS

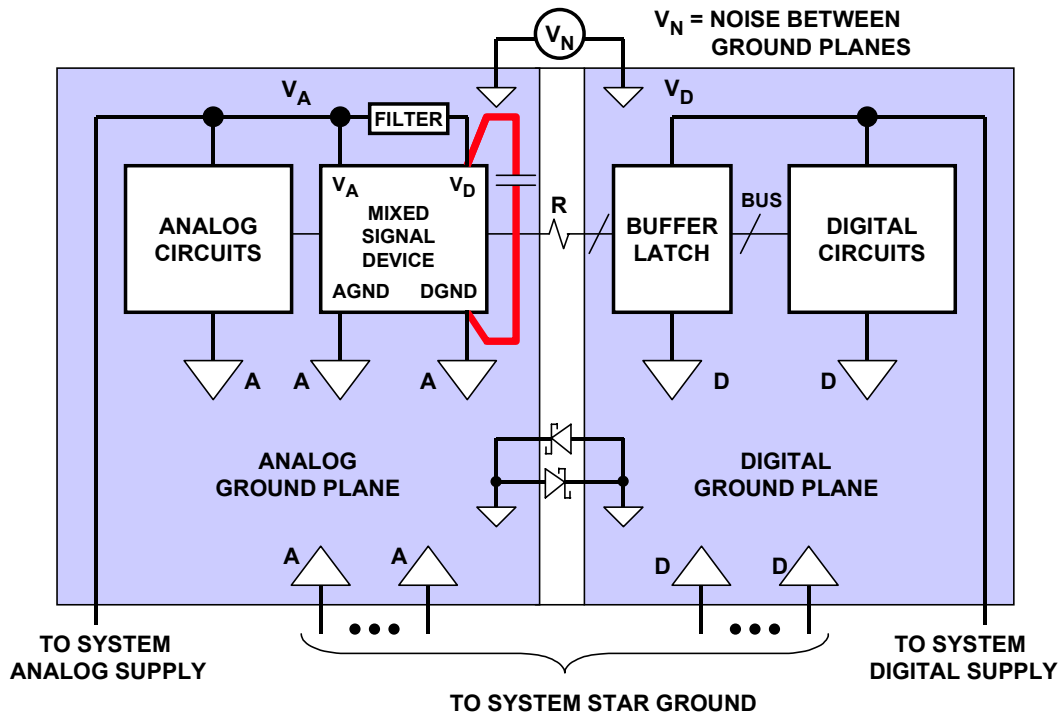


Figure 10.21

It is difficult to predict what level of digital current flowing into the analog ground plane will become unacceptable in a system. All we can do at this point is to suggest an alternative grounding method which may yield better performance.

SUMMARY: GROUNDING MIXED SIGNAL DEVICES WITH HIGH DIGITAL CURRENTS IN A MULTICARD SYSTEM

An alternative grounding method for a mixed signal device with high levels of digital currents is shown in Figure 10.22. The AGND of the mixed signal device is connected to the analog ground plane, and the DGND of the device is connected to the digital ground plane. The digital currents are isolated from the analog ground plane, but the noise between the two ground planes is applied directly between the AGND and DGND pins of the device. For this method to be successful, the analog and digital circuits within the mixed signal device must be well isolated. The noise between AGND and DGND pins must not be large enough to reduce internal noise margins or cause corruption of the internal analog circuits.

GROUNDING ALTERNATIVE FOR MIXED SIGNAL ICs WITH HIGH DIGITAL CURRENTS: MULTIPLE PC BOARDS

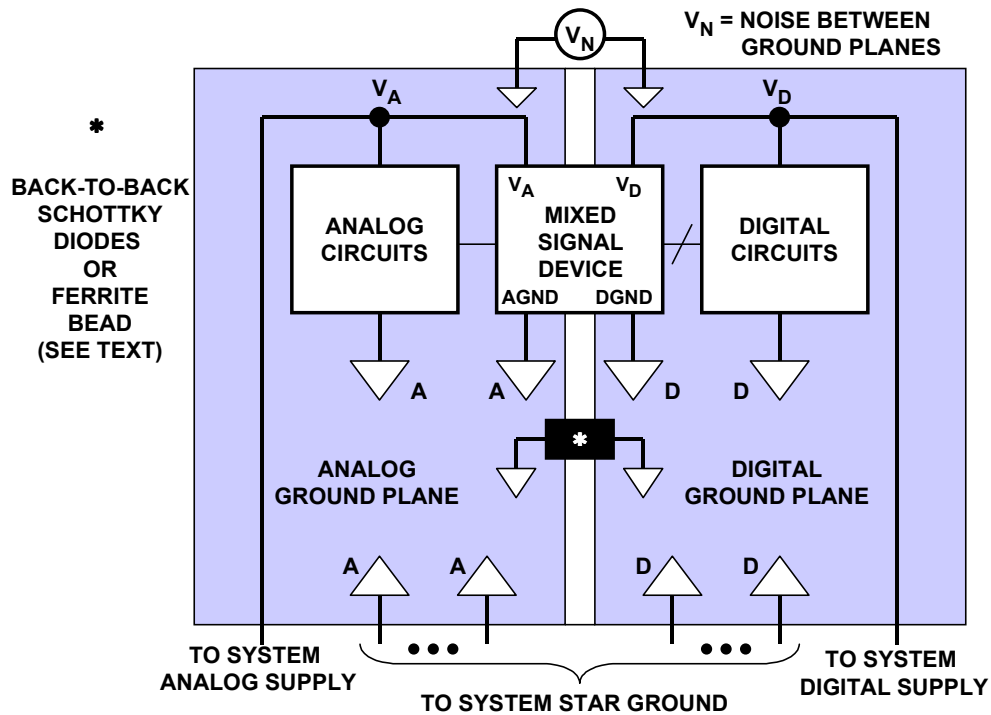


Figure 10.22

Figure 10.22 shows optional Schottky diodes (back-to-back) or a ferrite bead connecting the analog and digital ground planes. The Schottky diodes prevent large DC voltages or low frequency voltage spikes from developing across the two planes. These voltages can potentially damage the mixed signal IC if they exceed 300mV because they appear directly between the AGND and DGND pins. As an alternative to the back-to-back Schottky diodes, a ferrite bead provides a DC connection between the two planes but isolates them at frequencies above a few MHz where the ferrite bead becomes resistive. This protects the IC from DC voltages between AGND and DGND, but the DC connection provided by the ferrite bead can introduce unwanted DC ground loops and may not be suitable for high resolution systems.

GROUNDING DSPs WITH INTERNAL PHASE-LOCKED LOOPS

As if dealing with mixed-signal ICs with AGND and DGNDs wasn't enough, newer DSPs such as the ADSP-21160 SHARC with internal phase-locked-loops (PLLs) raise issues with respect to proper grounding. The ADSP-21160 PLL allows the internal core clock (determines the instruction cycle time) to operate at a user-selectable ratio of 2, 3, or 4 times the external clock frequency, CLKIN. The CLKIN rate is the rate at which the synchronous external ports operates. Although this allows using a lower frequency external clock, care must be taken with the power and ground connections to the internal PLL as shown in Figure 10.23.

GROUNDING DSPs WITH INTERNAL PHASE-LOCKED-LOOPS (PLLs)

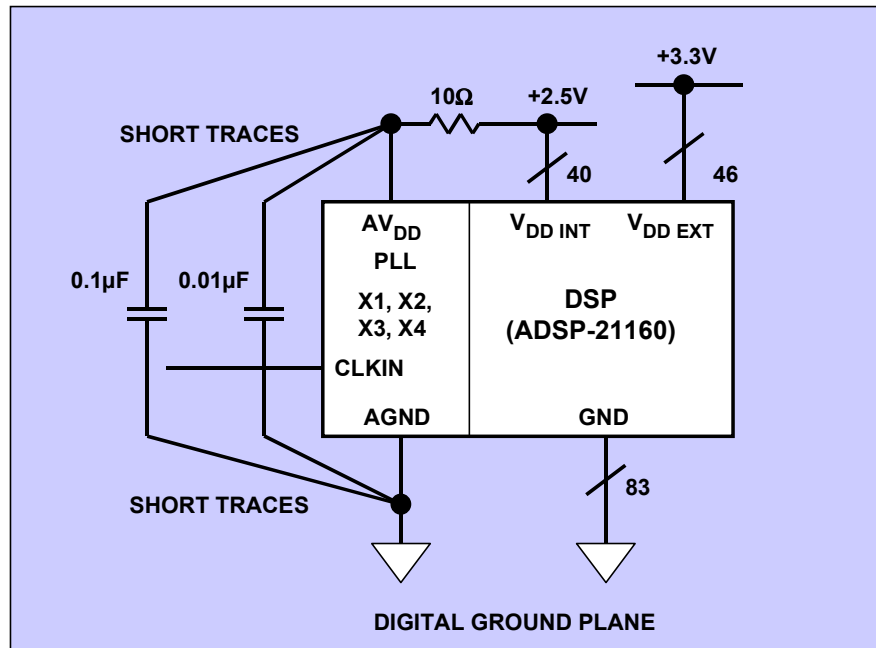


Figure 10.23

In order to prevent internal coupling between digital currents and the PLL, the power and ground connections to the PLL are brought out separately on pins labeled AV_{DD} and $AGND$, respectively. The AV_{DD} +2.5V supply should be derived from the $V_{DD INT}$ +2.5V supply using the filter network as shown. This ensures a relatively noise-free supply for the internal PLL. The $AGND$ pin of the PLL should be connected to the digital ground plane of the PC board using a short trace. The decoupling capacitors should be routed between the AV_{DD} pin and $AGND$ pin using short traces.

GROUNDING SUMMARY

There is no single grounding method which will guarantee optimum performance 100% of the time! This section has presented a number of possible options depending upon the characteristics of the particular mixed signal devices in question. It is helpful, however to provide for as many options as possible when laying out the initial PC board.

It is mandatory that at least one layer of the PC board be dedicated to ground plane! The initial board layout should provide for non-overlapping analog and digital ground planes, but pads and vias should be provided at several locations for the installation of back-to-back Schottky diodes or ferrite beads, if required. Pads and vias should also be provided so that the analog and digital ground planes can be connected together with jumpers if required.

The AGND pins of mixed-signal devices should in general always be connected to the analog ground plane. An exception to this are DSPs which have internal phase-locked-loops (PLLs), such as the ADSP-21160 SHARC. The ground pin for the PLL is labeled AGND, but should be connected directly to the digital ground plane for the DSP.

GROUNDING PHILOSOPHY SUMMARY

- **There is no single grounding method which is guaranteed to work 100% of the time!**
- **Different methods may or may not give the same levels of performance.**
- **At least one layer on each PC board MUST be dedicated to ground plane!**
- **Do initial layout with split analog and digital ground planes.**
- **Provide pads and vias on each PC board for back-to-back Schottky diodes and optional ferrite beads to connect the two planes.**
- **Provide "jumpers" so that DGND pins of mixed-signal devices can be connected to AGND pins (analog ground plane) or to digital ground plane. (AGND of PLLs in DSPs should be connected to digital ground plane).**
- **Provide pads and vias for "jumpers" so that analog and digital ground planes can be joined together at several points on each PC board.**
- **Follow recommendations on mixed signal device data sheet.**

Figure 10.24

SOME GENERAL PC BOARD LAYOUT GUIDELINES FOR MIXED-SIGNAL SYSTEMS

It is evident that noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems. If clock driver packages are used in clock distribution, only one frequency clock should be passed through a single package. Sharing drivers between clocks of different frequencies in the same package will produce excess jitter and crosstalk and degrade performance.

The ground plane can act as a shield where sensitive signals cross. Figure 10.25 shows a good layout for a data acquisition board where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

ANALOG AND DIGITAL CIRCUITS SHOULD BE PARTITIONED ON PCB LAYOUT

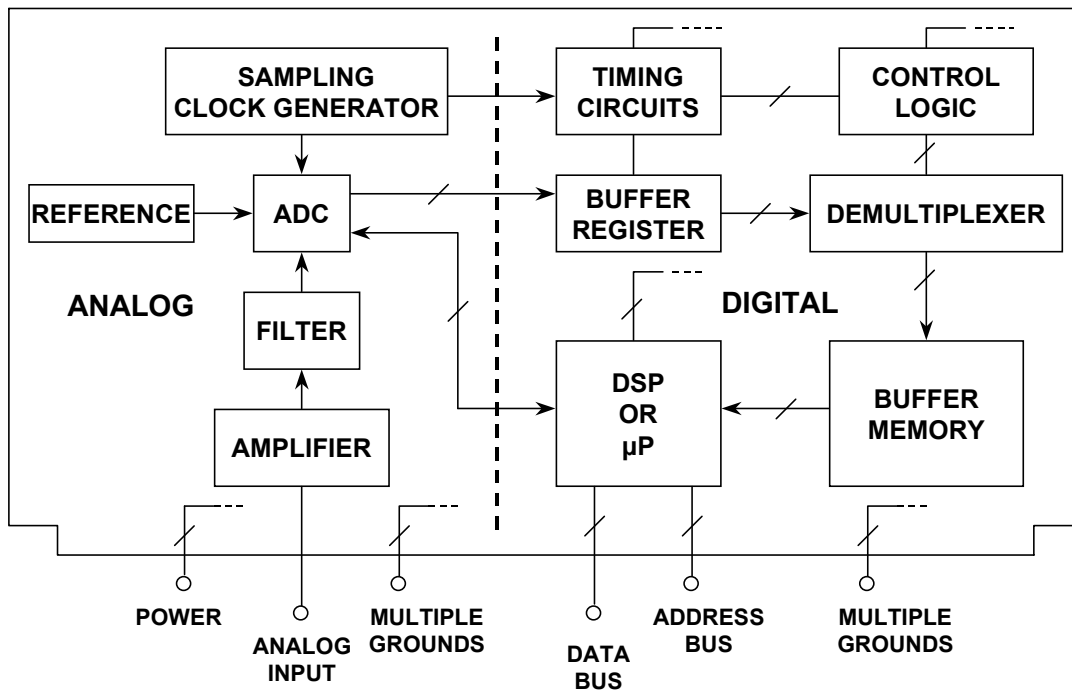


Figure 10.25

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run in parallel - it is therefore imperative to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10mΩ) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to allocate extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

Manufacturers of high performance mixed-signal ICs like Analog Devices offer evaluation boards to assist customers in their initial evaluations and layout. ADC evaluation boards generally contain an on-board low-jitter sampling clock oscillator, output registers, and appropriate power and signal connectors. They also may have additional support circuitry such as the ADC input buffer amplifier and external reference.

The layout of the evaluation board is optimized in terms of grounding, decoupling, and signal routing and can be used as a model when laying out the ADC PC board in the system. The actual evaluation board layout is usually available from the ADC manufacturer in the form of computer CAD files (Gerber files). In many cases, the layout of the various layers appears on the data sheet for the device.

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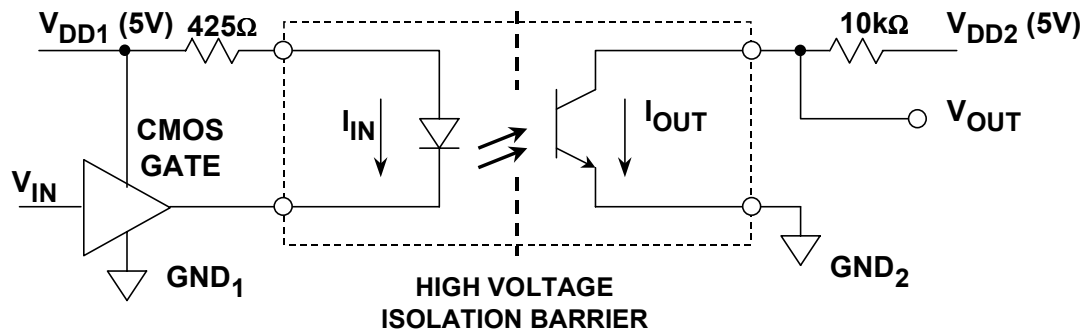
DIGITAL ISOLATION TECHNIQUES

Walt Kester

One way to break ground loops is to use isolation techniques. Analog isolation amplifiers find many applications where a high degree of isolation is required, such as in medical instrumentation. Digital isolation techniques offer a reliable method of transmitting digital signals over interfaces without introducing ground noise.

Optocouplers (also called optoisolators) are useful and available in a wide variety of styles and packages. A typical optocoupler based on an LED and a phototransistor is shown in Figure 10.26. A current of approximately 10mA is applied to an LED transmitter, and the light output is received by a phototransistor. The light produced by the LED is sufficient to saturate the phototransistor. Isolation of 5000V RMS to 7000V RMS is common. Although excellent for digital signals, optocouplers are too nonlinear for most analog applications. One should also realize that since the phototransistor is operated in a saturated mode, rise and fall-times can range from 10µs to 20µs in slower devices, thereby limiting applications at high speeds.

DIGITAL ISOLATION USING LED / PHOTOTRANSISTOR OPTOCOUPLEDERS



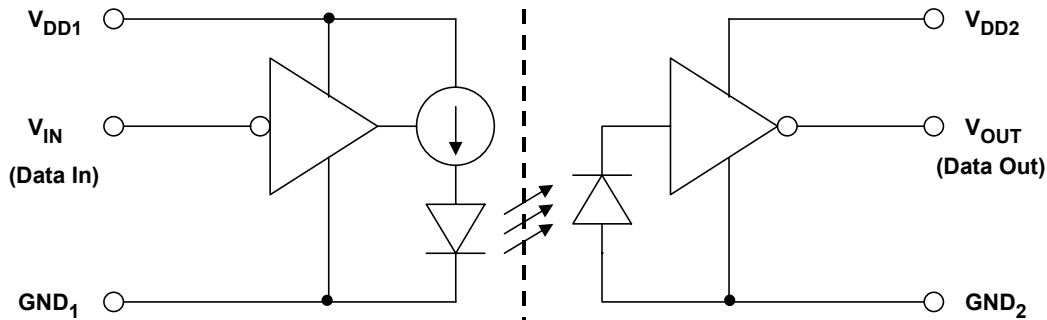
- Uses Light for Transmission Over a High Voltage Barrier
- The LED is the Transmitter, and the Phototransistor is the Receiver
- High Voltage Isolation: 5000V to 7000V RMS
- Non-Linear -- Best for Digital or Frequency Information
- Rise and Fall-times can be 10 to 20µs in Slower Devices
- Example: Siemens ILQ-1 Quad (<http://www.siemens.com>)

Figure 10.26

A faster optocoupler architecture is shown in Figure 10.27 and is based on an LED and a photodiode. The LED is again driven with a current of approximately 10mA. This produces a light output sufficient generate enough current in the receiving photodiode to develop a valid high logic level at the output of the transimpedance amplifier. Speed can vary widely between optocouplers, and the fastest ones have propagation delays of 20ns typical, and 40ns maximum, and can handle data rates

up to 25MBd for NRZ data. This corresponds to a maximum square wave operating frequency of 12.5MHz, and a minimum allowable passable pulse width of 40ns.

DIGITAL ISOLATION USING LED / PHOTODIODE OPTOCOUPPLERS



- +5V Supply Voltage
- 2500V RMS I/O Withstand Voltage
- Logic Signal Frequency: 12.5MHz Maximum
- 25MBd Maximum Data Rate
- 40ns Maximum Propagation Delay
- 9ns Typical Rise/Fall Time
- Example: Agilent HCPL-7720
(<http://www.semiconductor.agilent.com>)

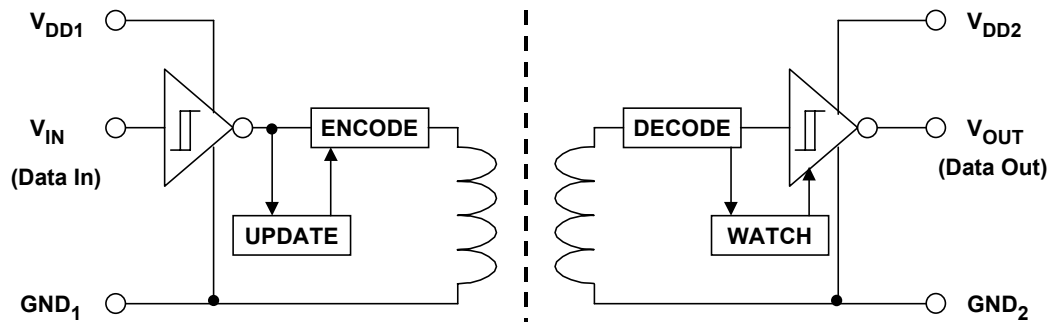
Figure 10.27

The ADuM1100A and ADuM1100B are digital isolators based on Analog Devices' *µm*Isolation™ (micromachined isolation) technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to the traditional optocouplers previously described.

Configured as pin-compatible replacements for existing high speed optocouplers, the ADuM1100A and ADuM1100B support data rates as high as 25MBd and 100MBd, respectively. A functional diagram of the devices is shown in Figure 10.28.

Both the ADuM1100A and ADuM1100B operate at either 3.3V or 5V supply voltages, have propagation delays < 10ns, edge asymmetry of < 2ns, and rise and fall-times < 2ns. They operate at very low power, less than 600µA of quiescent current (sum of both sides) and a dynamic current of less than 230µA per MBd of data rate. Unlike common transformer implementations, the parts provide DC correctness with a patented refresh feature which continuously updates the output signal.

ADuM1100A/ADuM1100B DIGITAL ISOLATORS



- +5V/+3.3V Supply Voltage
- 2500V RMS I/O Withstand Voltage
- 25MBd Maximum Data Rate (ADuM1100A)
- 100 MBd Maximum Data Rate (ADuM1100B)
- 10ns Maximum Propagation Delay
- 2ns Typical Rise/Fall Time
- Pin Compatible with Popular Optocouplers

Figure 10.28

The AD260/AD261 family of digital isolators isolates five digital control signals to/from high speed DSPs, microcontrollers, or microprocessors. The AD260 also has a 1.5W transformer for a 3.5kV RMS isolated external DC/DC power supply circuit.

Each line of the AD260 can handle digital signals up to 20MHz (40MBd) with a propagation delay of only 14ns which allows for extremely fast data transmission. Output waveform symmetry is maintained to within ± 1 ns of the input so the AD260 can be used to accurately isolate time-based pulse width modulator (PWM) signals.

A simplified schematic of one channel of the AD260/AD261 is shown in Figure 10.29. The data input is passed through a schmitt trigger circuit, through a latch, and a special transmitter circuit which differentiates the edges of the digital input signal and drives the primary winding of a proprietary transformer with a "set-high/set-low" signal. The secondary of the isolation transformer drives a receiver with the same "set-hi/set-low" data which regenerates the original logic waveform. An internal circuit operates in the background which interrogates all inputs about every $5\mu\text{s}$ and in the absence of logic transitions, sends appropriate "set-hi/set-low" data across the interface. Recovery time from a fault condition or at power-up is thus between $5\mu\text{s}$ and $10\mu\text{s}$.

The power transformer (available on the AD260) is designed to operate between 150kHz and 250kHz and will easily deliver more than 1W of isolated power when driven push-pull (5V) on the transmitter side. Different transformer taps, rectifier

and regulator schemes will provide combinations of $\pm 5V$, 15V, 24V, or even 30V or higher. The output voltage when driven with a low voltage-drop drive will be 37V p-p across the entire secondary with a 5V push-pull drive.

AD260/AD261 DIGITAL ISOLATORS

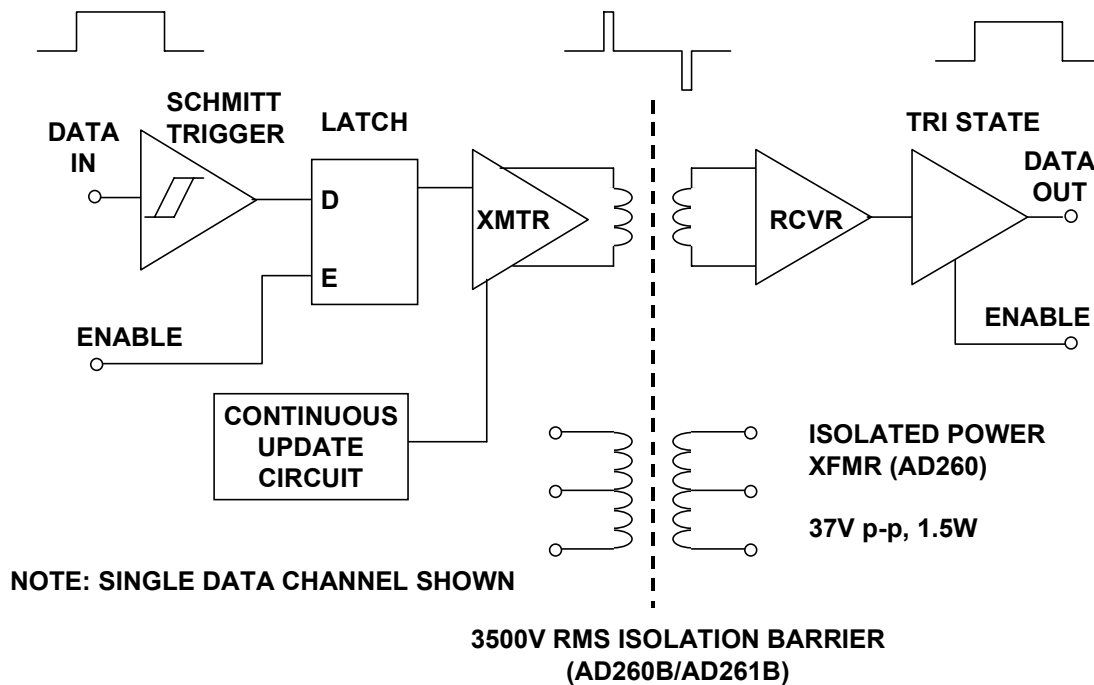


Figure 10.29

AD260/AD261 DIGITAL ISOLATOR KEY SPECIFICATIONS

- Isolation Test Voltage to 3500V RMS (AD260B/AD261B)
- Five Isolated Digital Lines Available in 6 Input/Output Configurations
- Logic Signal Frequency: 20MHz Max.
- Data Rate: 40MBd Max.
- Isolated Power Transformer: 37V p-p, 1.5W (AD260)
- Waveform Edge Transmission Symmetry: $\pm 1ns$
- Propagation Delay: 14ns
- Rise and Fall-Times < 5ns

Figure 10.30

POWER SUPPLY NOISE REDUCTION AND FILTERING

Walt Jung, Walt Kester, Bill Chestnut

Precision analog circuitry has traditionally been powered from well regulated, low noise linear power supplies. During the last decade however, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. Good reasons for the general popularity include their high efficiency, low temperature rise, small size, and light weight.

In spite of these benefits, switchers *do* have drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, resulting in both conducted and radiated noise, as well as unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20kHz to 1MHz, the spikes can contain frequency components extending to 100MHz or more. While specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the *peak* (or p-p) amplitudes of the switching spikes, at the output loading of your system.

The following section discusses filter techniques for rendering a switching regulator output *analog ready*, that is sufficiently quiet to power precision analog circuitry with relatively small loss of DC terminal voltage. The filter solutions presented are generally applicable to all power supply types incorporating switching element(s) in their energy path. This includes various DC-DC converters as well as popular 5V (PC type) supplies.

An understanding of the EMI process is necessary to understand the effects of supply noise on analog circuits and systems. Every interference problem has a *source*, a *path*, and a *receptor* [Reference 1]. In general, there are three methods for dealing with interference. First, source emissions can be minimized by proper layout, pulse-edge rise time control/reduction, filtering, and proper grounding. Second, radiation and conduction paths should be reduced through shielding and physical separation. Third, receptor immunity to interference can be improved, via supply and signal line filtering, impedance level control, impedance balancing, and utilizing differential techniques to reject undesired common-mode signals. This section focuses on reducing switching power supply noise with external post filters.

Tools useful for combating high frequency switcher noise are shown by Figure 10.31. They differ in electrical characteristics as well as their practicality towards noise reduction, and are listed roughly in an order of priorities. Of these tools, L and C are the most powerful filter elements, and are the most cost-effective, as well as small in size.

SWITCHING REGULATOR NOISE REDUCTION TOOLS

- Capacitors
- Inductors
- Ferrites
- Resistors
- Linear Post Regulation
- Proper Layout and Grounding Techniques
- PHYSICAL SEPARATION FROM SENSITIVE ANALOG CIRCUITS!!

Figure 10.31

Capacitors are probably the single most important filter component for switchers. There are many different types of capacitors, and an understanding of their individual characteristics is absolutely mandatory in the design of effective practical supply filters. There are generally three classes of capacitors useful in 10kHz-100MHz filters, broadly distinguished as the generic dielectric types; *electrolytic*, *organic*, *film*, and *ceramic*. These can in turn can be further sub-divided. A thumbnail sketch of capacitor characteristics is shown in the chart of Figure 10.32.

TYPES OF CAPACITORS

	Aluminum Electrolytic (General Purpose)	Aluminum Electrolytic (Switching Type)	Tantalum Electrolytic	OS-CON Electrolytic	Polyester (Stacked Film)	Ceramic (Multilayer)
Size	100 μ F	120 μ F	120 μ F	100 μ F	1 μ F	0.1 μ F
Rated Voltage	25 V	25 V	20 V	20 V	400 V	50 V
ESR	0.6 Ω @ 100 kHz	0.18 Ω @ 100 kHz	0.12 Ω @ 100 kHz	0.02 Ω @ 100 kHz	0.11 Ω @ 1 MHz	0.12 Ω @ 1 MHz
Operating Frequency (*)	\cong 100 kHz	\cong 500 kHz	\cong 1 MHz	\cong 1 MHz	\cong 10 MHz	\cong 1 GHz

(*) Upper frequency strongly size and package dependent

Figure 10.32

With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance characteristic switches from capacitive to inductive. This varies from as low as 10kHz in some electrolytics to as high as 100MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used. All capacitor types mentioned are available in surface mount packages, preferable for high speed uses.

The *electrolytic* family provides an excellent, cost-effective low-frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general purpose aluminum electrolytic* types, available in working voltages from below 10V up to about 500V, and in size from 1 to several thousand μF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without damage. They also have relatively high leakage currents (up to tens of μA , and strongly dependent upon design specifics).

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100V or less, with capacitance of up to 500 μF [Reference 3]. In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses [Reference 4]. This capacitor type competes directly with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte [Reference 5]. The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of low low-temperature ESR degradation.

Film capacitors are available in a very broad range of values and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10 μF /50V polyester capacitor (for example) is actually the size of your hand. Metalized (as opposed to foil) electrodes do help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest

HARDWARE DESIGN TECHNIQUES

voltage ratings (50V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as $10\text{m}\Omega$ or less, and the behavior of films generally is very high in terms of Q . In fact, this can cause problems of spurious resonance in filters, requiring damping components.

Film capacitors using a wound layer-type construction can be inductive. This can limit their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads [see References 4, 5, 6]. Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL [Reference 7].

Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to well above 10MHz. At the highest frequencies, only stacked film types should be considered. Some manufacturers are now supplying film types in leadless surface mount packages, which eliminates the lead length inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several μF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200V [see ceramic families of Reference 3]. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). NP0 types are limited to values of $0.1\mu\text{F}$ or less, with $0.01\mu\text{F}$ representing a more practical upper limit.

Multilayer ceramic “chip caps” are very popular for bypassing/ filtering at 10MHz or higher, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1GHz. For high frequency applications, a useful selection can be ensured by selecting a value which has a self-resonant frequency *above* the highest frequency of interest.

All capacitors have some finite ESR. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying “free” damping. For example, in most electrolytic types, a nominally flat broad series resonance region can be noted by the impedance vs. frequency plot. This occurs where $|Z|$ falls to a minimum level, nominally equal to the capacitor’s ESR at that frequency. This low Q resonance can generally cover a relatively wide frequency range of several octaves.

Contrasted to the very high Q sharp resonances of film and ceramic caps, the low Q behavior of electrolytics can be useful in controlling resonant peaks.

In most electrolytic capacitors, ESR degrades noticeably at low temperature, by as much as a factor of 4-6 times at -55°C vs. the room temperature value. For circuits where ESR is critical to performance, this can lead to problems. Some specific electrolytic types do address this problem, for example within the HFQ switching types, the -10°C ESR at 100kHz is no more than $2\times$ that at room temperature. The OSCON electrolytics have a ESR vs. temperature characteristic which is relatively flat.

As noted, all real capacitors have parasitic elements which limit their performance. The equivalent electrical network representing a real capacitor models both ESR and ESL as well as the basic capacitance, plus some shunt resistance (see Figure 10.33). In such a practical capacitor, at low frequencies the net impedance is almost purely capacitive. At intermediate frequencies, the net impedance is determined by ESR, for example about 0.12Ω to 0.4Ω at 125kHz, for several types. Above about 1MHz these capacitor types become inductive, with impedance dominated by the effect of ESL. All electrolytics will display impedance curves similar in general shape to that of Figure 10.34. The minimum impedance will vary with the ESR, and the inductive region will vary with ESL (which in turn is strongly affected by package style).

CAPACITOR EQUIVALENT CIRCUIT AND PULSE RESPONSE

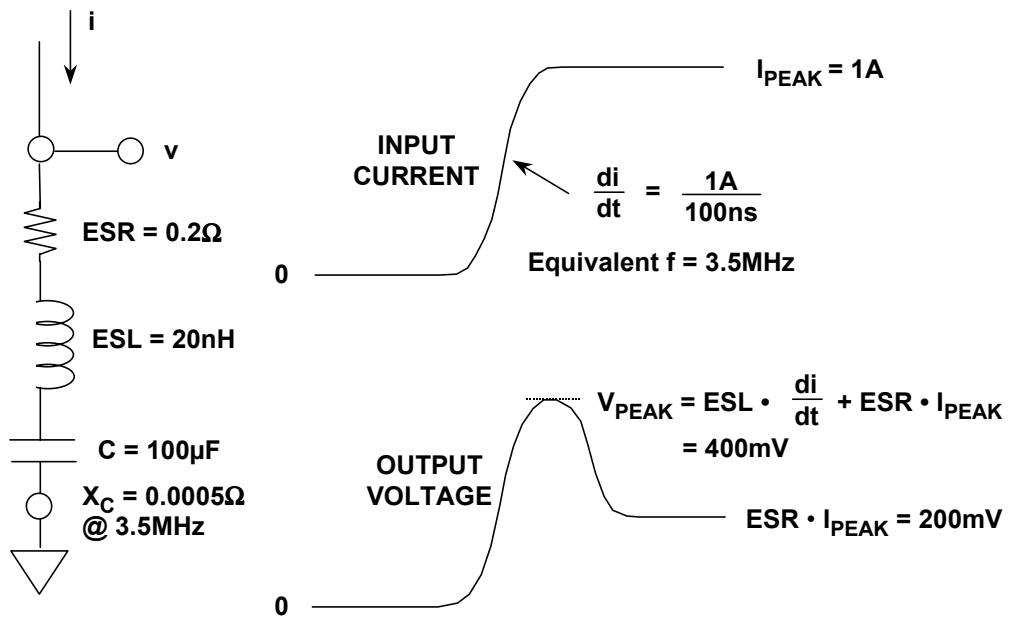


Figure 10.33

ELECTROLYTIC CAPACITOR IMPEDANCE VERSUS FREQUENCY

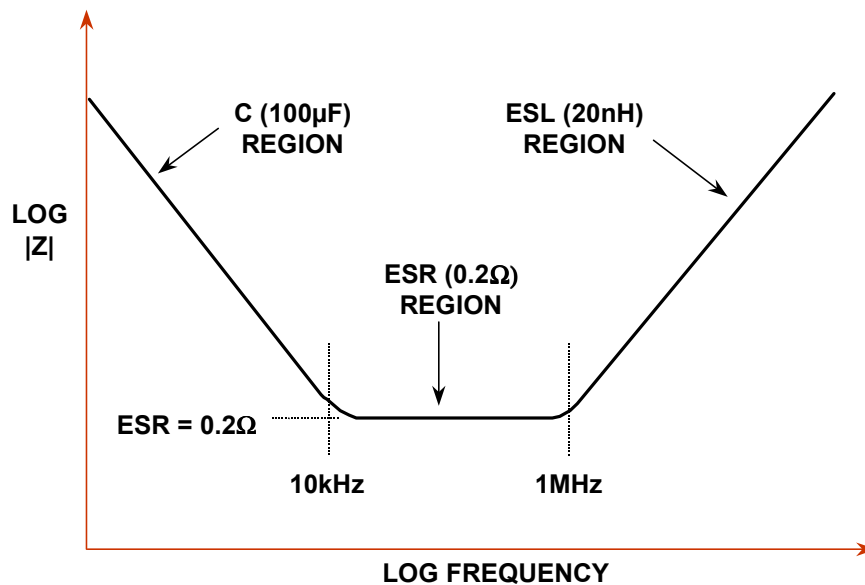


Figure 10.34

Regarding inductors, *Ferrites* (non-conductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are extremely useful in power supply filters [Reference 9]. At low frequencies (<100kHz), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100kHz, ferrites become resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, DC bias current, number of turns, size, shape, and temperature. Figure 10.35 summarizes a number of ferrite characteristics, and Figure 10.36 shows the impedance characteristic of several ferrite beads from Fair-Rite (<http://www.fair-rite.com>).

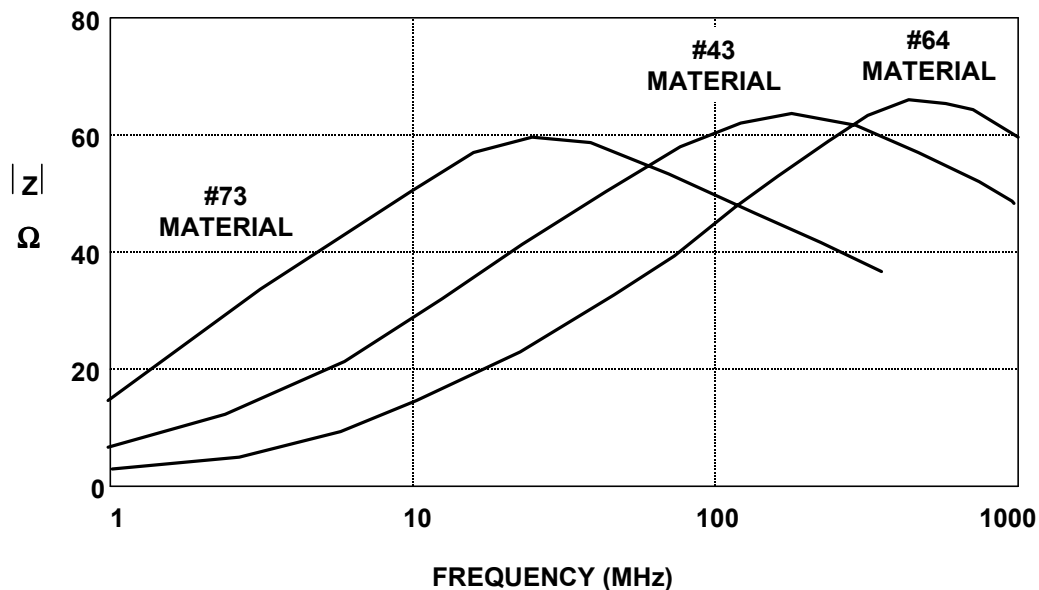
Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles (see References 10 and 11). A simple form is the *bead* of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the decoupled stage. Alternately, the *leaded ferrite bead* is the same bead, pre-mounted on a length of wire and used as a component (see Reference 11). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface mount beads are also available.

FERRITES SUITABLE FOR HIGH FREQUENCY FILTERS

- Ferrites Good for Frequencies Above 25kHz
- Many Sizes and Shapes Available Including Leaded "Resistor Style"
- Ferrite Impedance at High Frequencies Primarily Resistive -- Ideal for HF Filtering
- Low DC Loss: Resistance of Wire Passing Through Ferrite is Very Low
- High Saturation Current Versions Available
- Choice Depends Upon:
 - ◆ Source and Frequency of Interference
 - ◆ Impedance Required at Interference Frequency
 - ◆ Environmental: Temperature, AC and DC Field Strength, Size / Space Available
- Always Test the Design!

Figure 10.35

IMPEDANCE OF FERRITE BEADS



Courtesy: Fair-Rite Products Corp, Walkill, NY
 (<http://www.fair-rite.com>)

Figure 10.36

HARDWARE DESIGN TECHNIQUES

PSpice ferrite models for Fair-Rite materials are available, and allow ferrite impedance to be estimated [see Reference 12]. These models have been designed to match measured impedances rather than theoretical impedances.

A ferrite's impedance is dependent upon a number of inter-dependent variables, and is difficult to quantify analytically, thus selecting the proper ferrite is not straightforward. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. Second, the expected temperature range of the filter should be known, as ferrite impedance varies with temperature. Third, the peak DC current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with some experimentation with the actual filter connected to the supply output under system load conditions, should lead to a proper ferrite selection.

Using proper component selection, low and high frequency band filters can be designed to smooth a noisy switcher's DC output to produce an *analog ready* 5V supply. It is most practical to do this over two (and sometimes more) stages, each stage optimized for a range of frequencies. A basic stage can be used to carry all of the DC load current, and filter noise by 60dB or more up to a 1-10MHz range. This larger filter is used as a *card entry filter* providing broadband filtering for all power entering a PC card. Smaller, more simple local filter stages are also used to provide higher frequency decoupling right at the power pins of individual stages.

SWITCHING REGULATOR EXPERIMENTS

In order to better understand the challenge of filtering switching regulators, a series of experiments were conducted with a representative device, the ADP1148 synchronous buck regulator with a 9V input and a 3.3V/1A output.

In addition to observing typical input and output waveforms, the objective of these experiments was to reduce the output ripple to less than 10mV peak-to-peak, a value suitable for driving most analog circuits.

Measurements were made using a Tektronix wideband digitizing oscilloscope with the input bandwidth limited to 20MHz so that the ripple generated by the switching regulators could be more readily observed. In a system, power supply ripple frequencies above 20MHz are best filtered locally at each IC power pin with a low inductance ceramic capacitor and perhaps a series-connected ferrite bead.

Probing techniques are critical for accurate ripple measurements. A standard passive 10X probe was used with a "bayonet" probe tip adapter for making the ground connection as short as possible (see Figure 10.37). Use of the "ground clip lead" is not recommended in making this type of measurement because the lead length in the ground connection forms an unwanted inductive loop which picks up high frequency switching noise, thereby corrupting the signal being measured.

PROPER PROBING TECHNIQUES

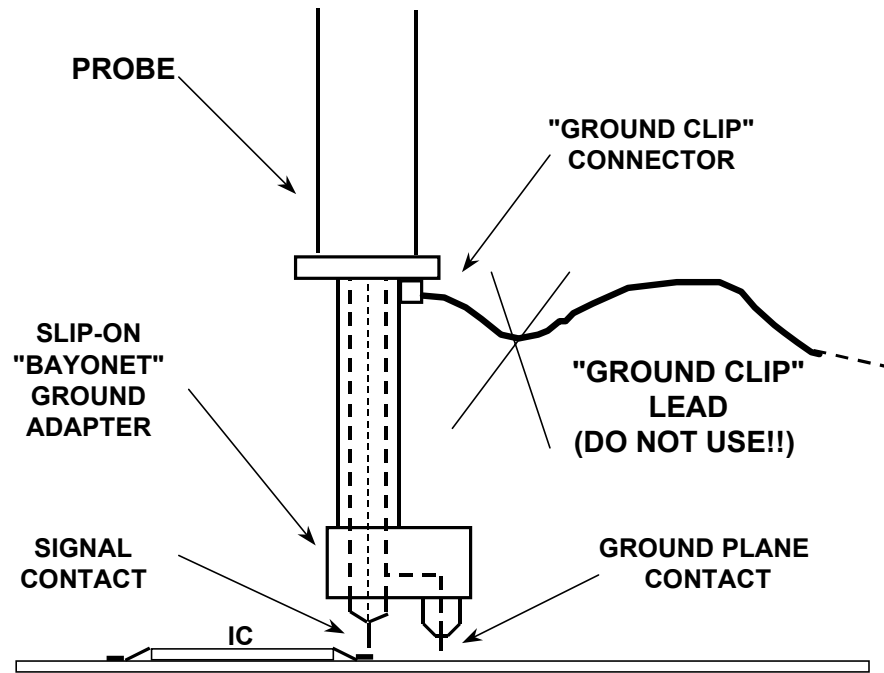


Figure 10.37

Note: Schematic representation of proper physical grounding is almost impossible. In all the following circuit schematics, the connections to ground are made to the ground plane using the shortest possible connecting path, regardless of how they are indicated in the actual circuit schematic diagram.

The circuit for the ADP1148 9V to 3.3V/1A buck regulator is shown in Figure 10.38. The output waveform of the ADP1148 buck regulator is shown in Figure 10.39. The fundamental switching frequency is approximately 150kHz, and the output ripple is approximately 40mV.

Adding an output filter consisting of a 50μH inductor and a 100μF leaded tantalum capacitor reduced the ripple to approximately 3mV as shown in Figure 10.40.

Linear regulators are often used following switching regulators for better regulation and lower noise. Low dropout (LDO) regulators such as the ADP3310 are desirable in these applications because they require only a small input-to-output series voltage to maintain regulation. This minimizes power dissipation in the pass device and may eliminate the need for a heat sink. Figure 10.41 shows the ADP1148 buck regulator configured for a 9V input and a 3.75V/1A output. The output drives an ADP3310 linear LDO regulator configured for 3.75V input and 3.3V/1A output. The input and output of the ADP3310 is shown in Figure 10.42. Notice that the regulator reduces the ripple from 40mV to approximately 5mV.

ADP1148 BUCK REGULATOR CIRCUIT

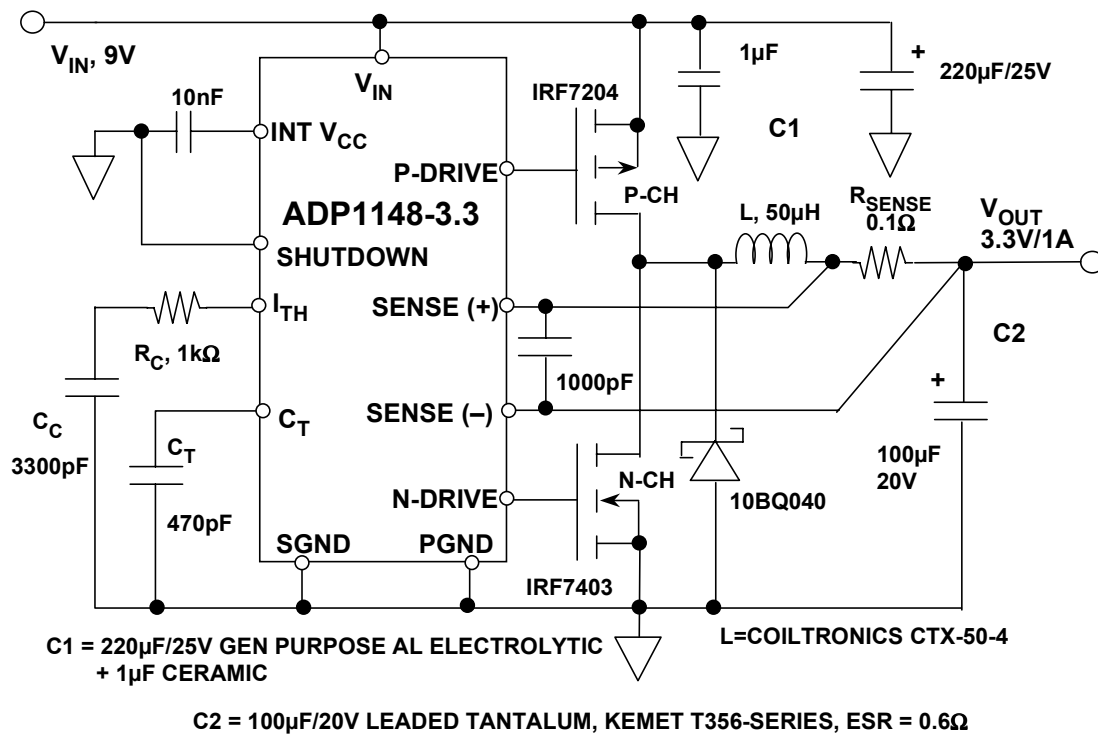


Figure 10.38

ADP1148 BUCK OUTPUT WAVEFORM

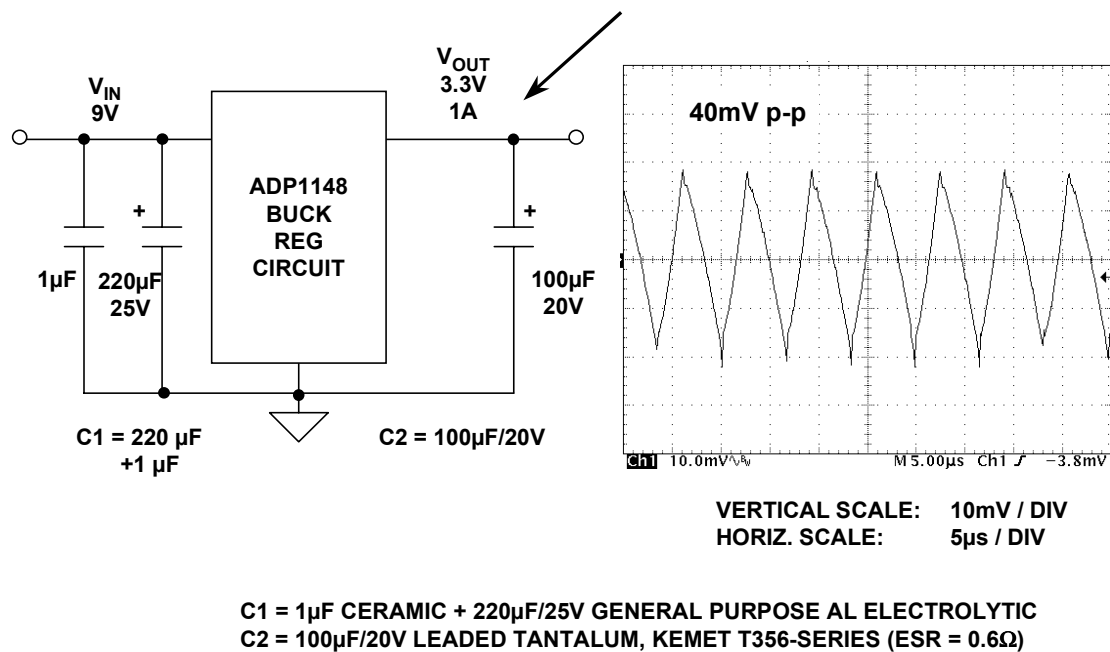
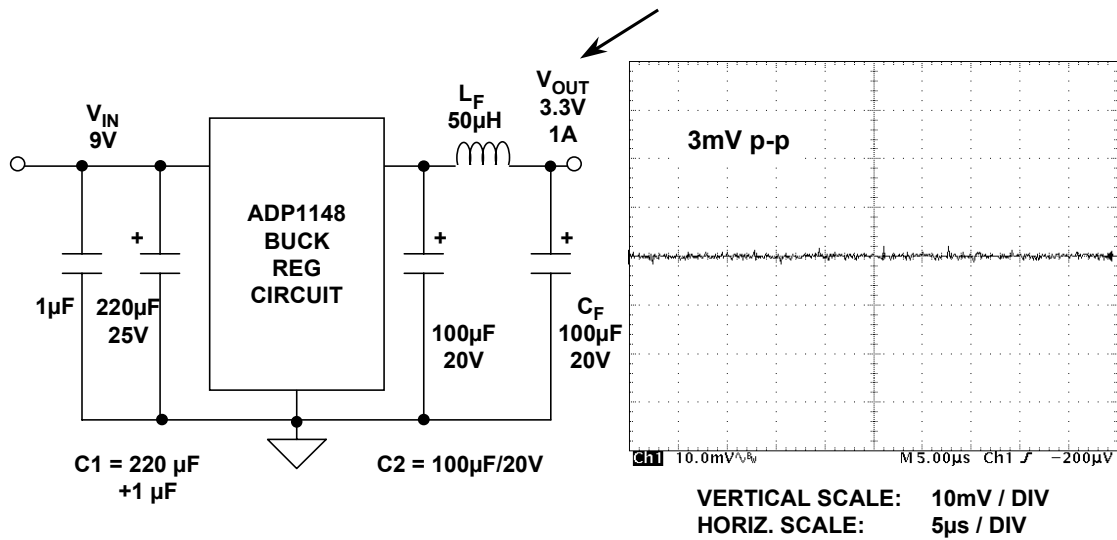


Figure 10.39

ADP1148 BUCK FILTERED OUTPUT



C1 = 1µF CERAMIC + 220µF/25V GENERAL PURPOSE AL ELECTROLYTIC
 C2 = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES (ESR = 0.6Ω)

OUTPUT FILTER

LF=COILTRONICS CTX-50-4

CF = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES

Figure 10.40

ADP1148 BUCK REGULATOR DRIVING ADP3310 LOW DROPOUT REGULATOR

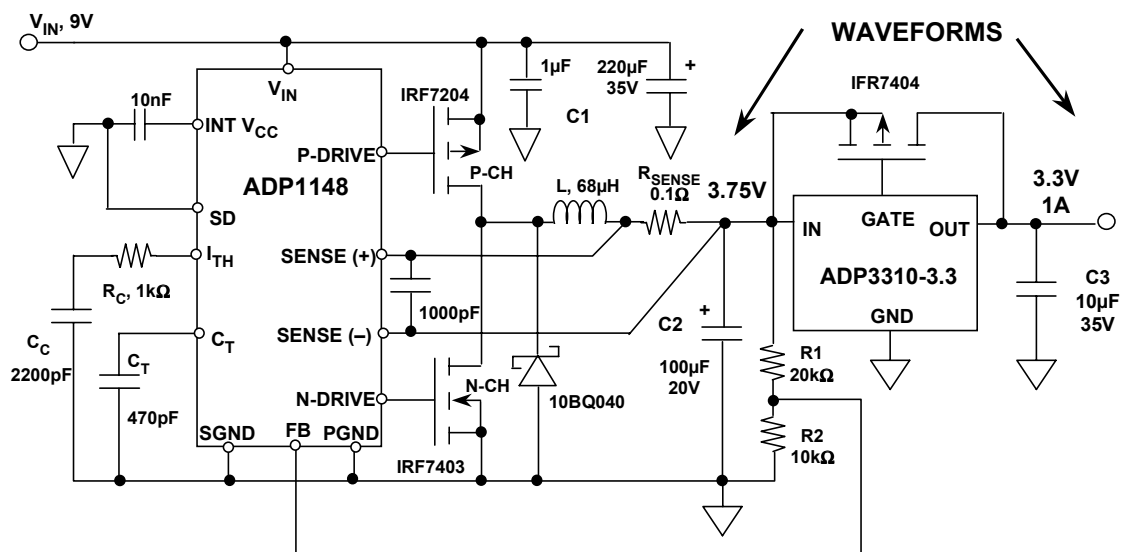


Figure 10.41

WAVEFORMS FOR ADP1148 BUCK REGULATOR DRIVING ADP3310 LOW DROPOUT REGULATOR

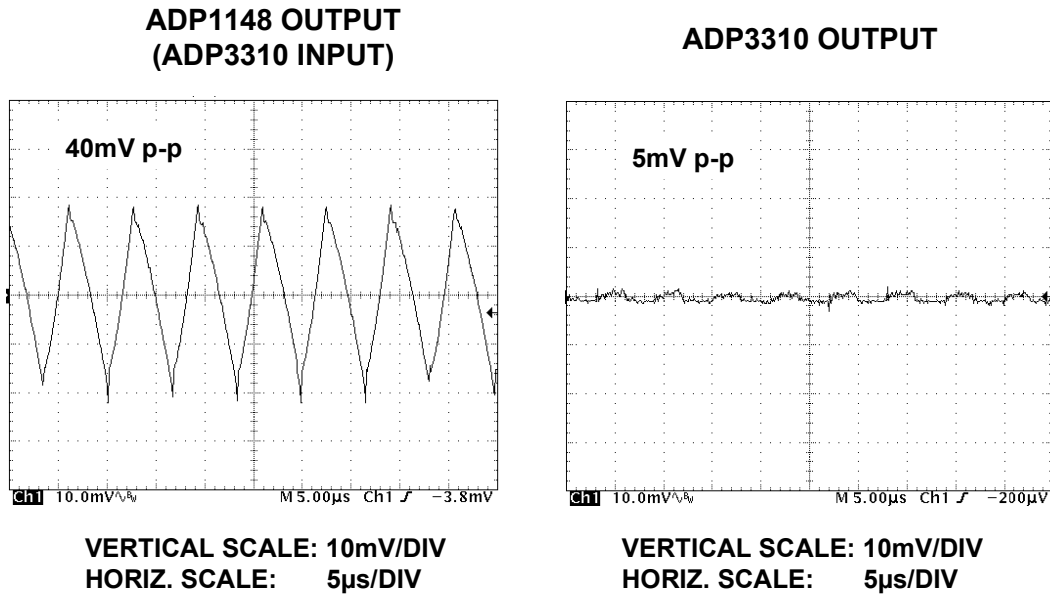


Figure 10.42

There are many tradeoffs in designing power supply filters. The success of any filter circuit is highly dependent upon a compact layout and the use of a large area ground plane. As has been stated earlier, all connections to the ground plane should be made as short as possible to minimize parasitic resistance and inductance.

Output ripple can be reduced by the addition of low ESL/ESR capacitors to the output. However, it may be more efficient to use an LC filter to accomplish the ripple reduction. In any case, proper component selection is critical. The inductor should not saturate under the maximum load current, and its DC resistance should be low enough as not to induce significant voltage drop. The capacitors should have low ESL and ESR and be rated to handle the required ripple current.

Low dropout linear post regulators provide both ripple reduction as well as better regulation and can be effective, provided the sacrifice in efficiency is not excessive.

Finally, it is difficult to predict the output ripple current analytically, and there is no substitute for a prototype using the real-world components. Once the filter is proven to provide the desired ripple attenuation (with some added safety margin), care must be taken that parts substitutions or vendor changes are not made in the final production units without first testing them in the circuit for equivalent performance.

SWITCHING SUPPLY FILTER SUMMARY

- Proper Layout and Grounding (using Ground Plane) Mandatory
- Low ESL/ESR Capacitors Give Best Results
- Parallel Capacitors Lower ESR/ESL and Increase Capacitance
- External LC Filters Very Effective in Reducing Ripple
- Linear Post Regulation Effective for Noise Reduction and Best Regulation
- Completely Analytical Approach Difficult, Prototyping is Required for Optimum Results
- Once Design is Finalized, Do Not Switch Vendors or Use Parts Substitutions Without First Verifying Their Performance in Circuit
- High Frequency Localized Decoupling at IC Power Pins is Still Required

Figure 10.43

LOCALIZED HIGH FREQUENCY POWER SUPPLY FILTERING

The LC filters described in the previous section are useful in filtering switching regulator outputs. However, it may be desirable to place similar filters on the individual PC boards where the power first enters the board. Of course, if the switching regulator is placed on the PC board, then the LC filter should be an integral part of the regulator design.

Localized high frequency filters may also be required at each IC power pin (see Figure 10.44). Surface mount ceramic capacitors are ideal choices because of their low ESL. It is important to make the connections to the power pin and the ground plane as short as possible. In the case of the ground connection, a via directly to the ground plane is the shortest path. Routing the capacitor ground connection to another ground pin on the IC is not recommended due to the added inductance of the trace. In some cases, a ferrite bead in series with the power connection may also be desirable.

LOCALIZED DECOUPLING TO GROUND PLANE USING SHORTEST PATH

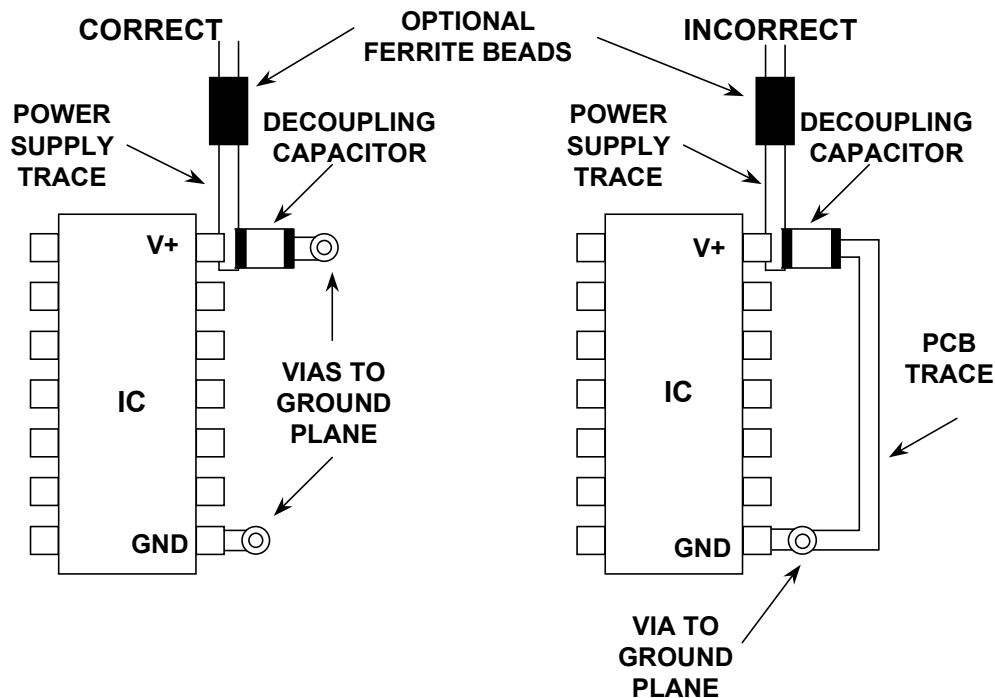


Figure 10.44

The following list summarizes the switching power supply filter layout/construction guidelines which will help ensure that the filter does the best possible job:

- (1) *Pick the highest electrical value and voltage rating for filter capacitors which is consistent with budget and space limits. This minimizes ESR, and maximizes filter performance. Pick chokes for low ΔL at the rated DC current, as well as low DCR.*
- (2) *Use short and wide PCB tracks to decrease voltage drops and minimize inductance. Make track widths at least 200 mils for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance.*
- (3) *Use short leads or better yet, leadless components, to minimize lead inductance. This minimizes the tendency to add excessive ESL and/or ESR. Surface mount packages are preferred. Make all connections to the ground plane as short as possible.*
- (4) *Use a large-area ground plane for minimum impedance.*
- (5) *Know what your components do over frequency, current and temperature variations! Make use of vendor component models for the simulation of prototype designs, and make sure that lab measurements correspond reasonably with the*

simulation. While simulation is not absolutely necessary, it does instill confidence in a design when correlation is achieved (see Reference 15).

HIGH DENSITY DSP LOCALIZED DECOUPLING CONSIDERATIONS

High pin-count DSP packages require special consideration with respect to localized decoupling due to their high digital transient currents. Typical decoupling arrangements are shown in Figure 10.45. The surface mount capacitors are placed on the top side of the PC board in Figure 10.45A. For the SHARC-family, eight 0.02 μ F ceramic capacitors are recommended. They should be placed as close to the package as possible. The connections to the V_{DD} pins should be as short as possible using wide traces. The connections to ground should be made directly to the ground plane with vias. A less desirable method is shown in Figure 10.45B, where the capacitors are mounted on the back side of the PC board underneath the footprint of the package. If the ground plane underneath the package footprint is perforated with many signal vias, the capacitor return transient current must flow to the outside ground plane, which may be poorly connected to the inside ground plane due to the vias.

**DECOUPLING HIGH PIN-COUNT DSPs
IN PQFP PACKAGES**

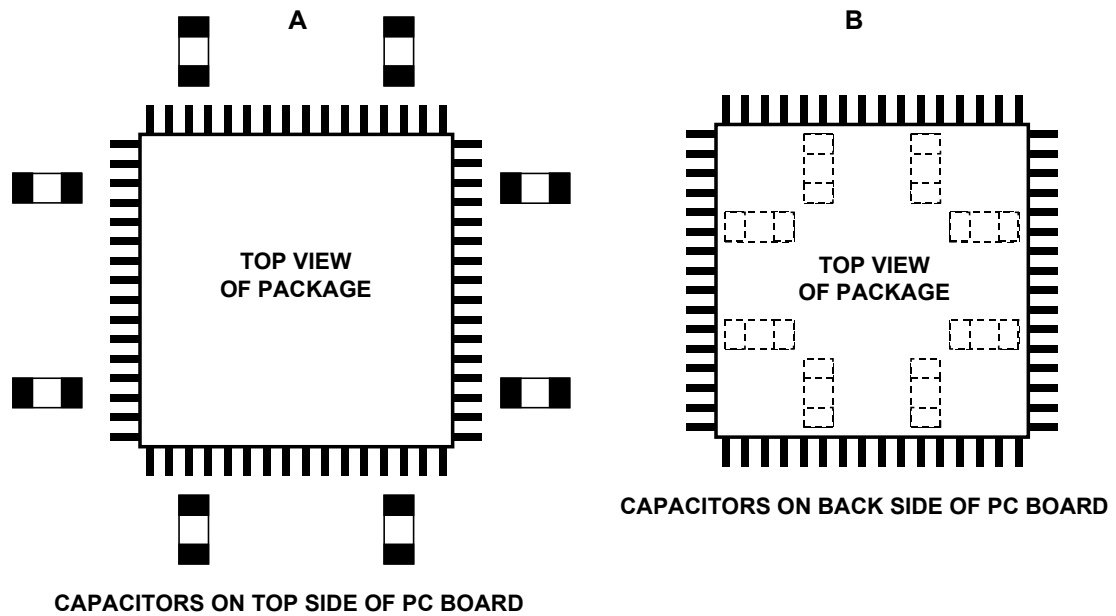


Figure 10.45

The PC board for a ball grid array (BGA) package is shown in Figure 10.46. Note that all connections to the balls must be made using vias to other layers of the board. The “dogbone” pattern shown is often used for the BGA packages. The shaded area indicates the location of the solder mask. As in the case of PQFP packages, the localized decoupling capacitors should be placed as close as possible to the package with short connections to the V_{DD} pins and direct connections to vias to the ground plane layer.

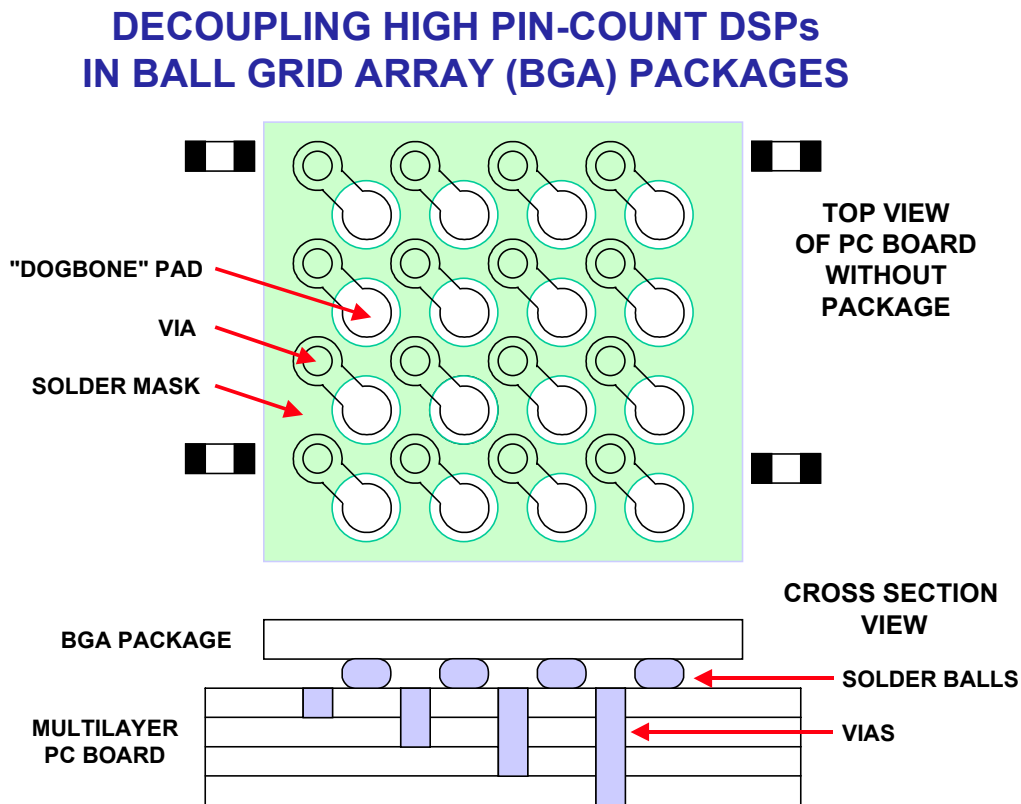


Figure 10.46

The ADSP-21160 400-ball BGA 27mm by 27mm package approximate power and ground assignments are shown in Figure 10.47. The ball pitch is 1.27mm. Approximately 84 balls are used in the center of the pattern for ground connections. The connections to the core voltage (40 balls) and the external voltage (46 balls) surround the ground balls. The remaining outer balls are used for the various signals.

The centrally located ground balls serve a dual function. Their primary function is to make a low impedance connection directly to the ground plane layer. Their secondary function is to conduct the package heat to the ground plane layer which also acts as a heat sink, since the device must dissipate about 2.5W under average operating conditions. The addition of an external heatsink as shown lowers the junction-to-ambient thermal resistance even further.

ADSP-21160 DSP 400-PIN PBGA PACKAGE BALL LOCATIONS

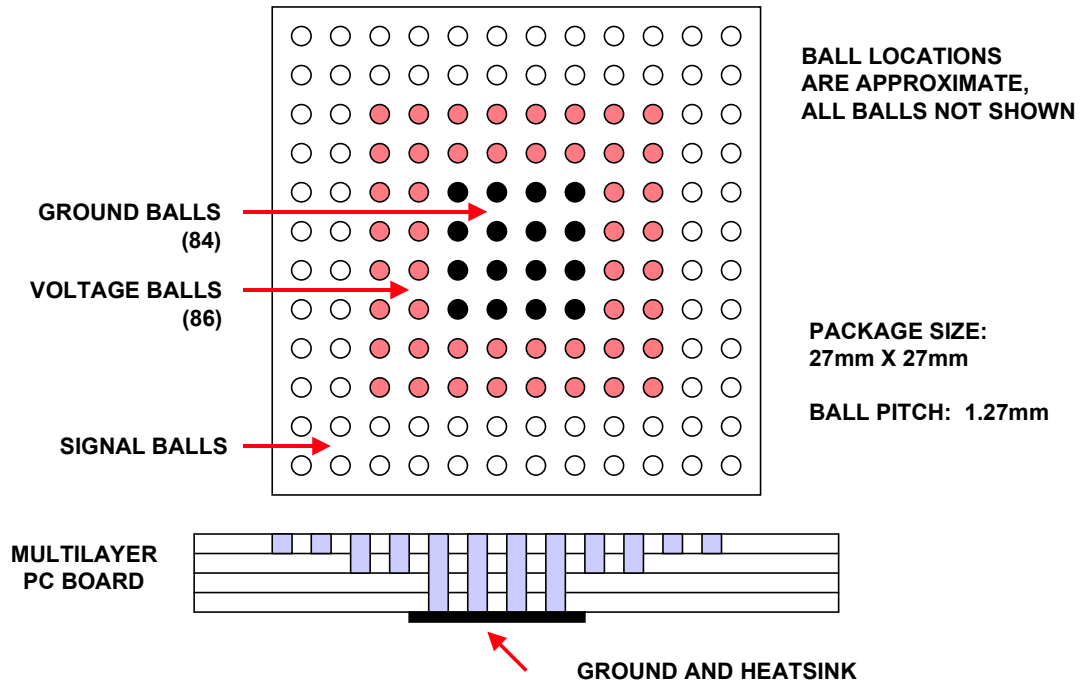


Figure 10.47

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DEALING WITH HIGH SPEED LOGIC

Much has been written about terminating printed circuit board traces in their characteristic impedance to avoid reflections. A good rule-of-thumb to determine when this is necessary is as follows: *Terminate the line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster).* A conservative approach is to use a 2 inch (PCB track length)/nanosecond (rise-, fall-time) criterion. For example, PCB tracks for high-speed logic with rise/fall time of 1ns should be terminated in their characteristic impedance if the track length is equal to or greater than 2 inches (including any meanders). Figure 10.48 shows the typical rise/fall times of several logic families including the SHARC DSPs operating on +3.3V supplies. As would be expected, the rise/fall times are a function of load capacitance.

TYPICAL DSP OUTPUT RISE TIMES AND FALL TIMES

- GaAs: 0.1ns
- ECL: 0.75ns
- ADI SHARC DSPs: 0.5 ns to 1 ns (Operating on +3.3V Supply)

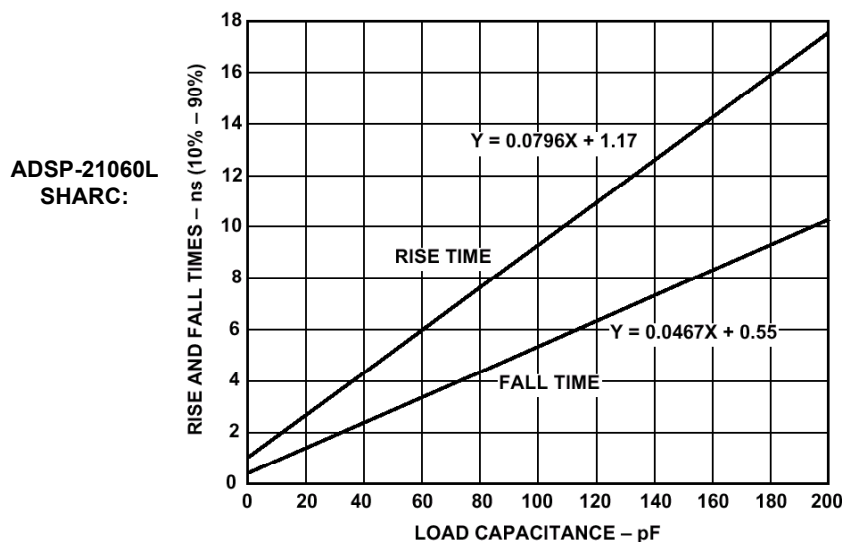


Figure 10.48

This same 2 inch/nanosecond rule of thumb should be used with analog circuits in determining the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max} , then the equivalent risetime, t_r , can be calculated using the equation $t_r = 0.35/f_{max}$. The maximum PCB track length is then calculated by multiplying the risetime by 2 inch/nanosecond. For example, a maximum output frequency of 100MHz corresponds to a risetime of 3.5ns, and a track carrying this signal greater than 7 inches should be treated as a transmission line.

Equation 10.1 can be used to determine the characteristic impedance of a PCB track separated from a power/ground plane by the board's dielectric (microstrip transmission line):

$$Z_0 (\Omega) = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left[\frac{5.98d}{0.89w + t} \right] \quad \text{Eq. 10.1}$$

where ϵ_r = dielectric constant of printed circuit board material;
 d = thickness of the board between metal layers, in mils;
 w = width of metal trace, in mils; and
 t = thickness of metal trace, in mils.

The one-way transit time for a single metal trace over a power/ground plane can be determined from Eq.10.2:

$$t_{pd} (\text{ns} / \text{ft}) = 1.017 \sqrt{0.475\epsilon_r + 0.67} \quad \text{Eq. 10.2}$$

For example, a standard 4-layer PCB board might use 8-mil wide, 1 ounce (1.4 mils) copper traces separated by 0.021" FR-4 ($\epsilon_r=4.7$) dielectric material. The characteristic impedance and one-way transit time of such a signal trace would be 88Ω and 1.7ns/ft (7"/ns), respectively.

The best ways to keep sensitive analog circuits from being affected by fast logic are to physically separate the two and to use no faster logic family than is dictated by system requirements. In some cases, this may require the use of several logic families in a system. An alternative is to use series resistance or ferrite beads to slow down the logic transitions where the speed is not required. Figure 10.49 shows two methods. In the first, the series resistance and the input capacitance of the gate form a lowpass filter. Typical CMOS input capacitance is 5pF to 10pF. Locate the series resistor close to the driving gate. The resistor minimizes transient currents and may eliminate the necessity of using transmission line techniques. The value of the resistor should be chosen such that the rise and fall times at the receiving gate are fast enough to meet system requirement, but no faster. Also, make sure that the resistor is not so large that the logic levels at the receiver are out of specification because of the voltage drop caused by the source and sink current which flow through the resistor. The second method is suitable for longer distances (>2 inches), where additional capacitance is added to slow down the edge speed. Notice that either one of these techniques increases delay and increases the rise/fall time of the original signal. This must be considered with respect to the overall timing budget, and the additional delay may not be acceptable.

Figure 10.50 shows a situation where several DSPs must connect to a single point, as would be the case when using read or write strobes bidirectionally connected from several DSPs. Small damping resistors shown in Figure 10.50A can minimize ringing provided the length of separation is less than about 2 inches. This method will also increase rise/fall times and propagation delay. If two groups of processors must be connected, a single resistor between the pairs of processors as shown in Figure 10.50B can serve to damp out ringing.

DAMPING RESISTORS SLOW DOWN FAST LOGIC EDGES TO MINIMIZE EMI/RFI PROBLEMS

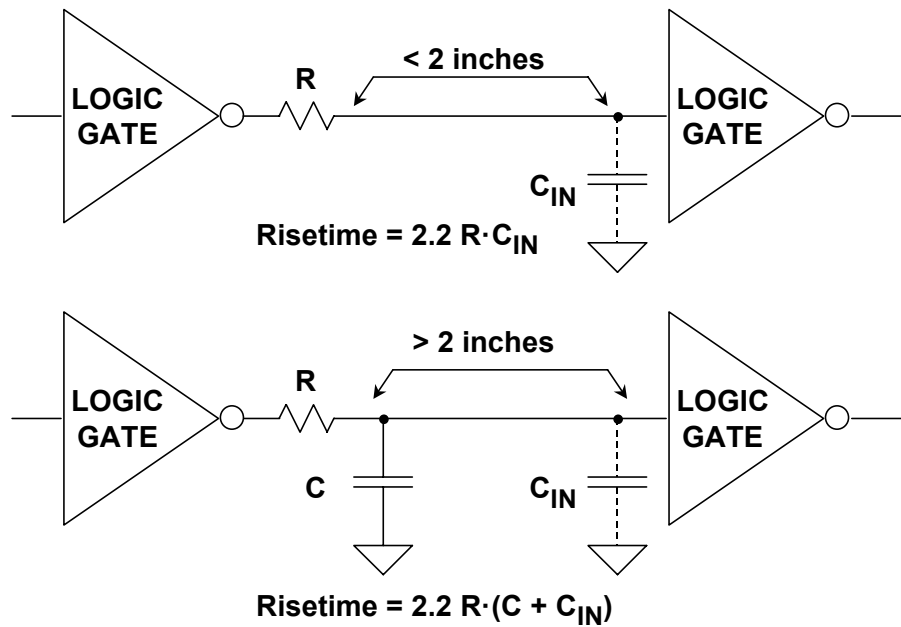


Figure 10.49

SERIES DAMPING RESISTORS FOR SHARC DSP INTERCONNECTIONS

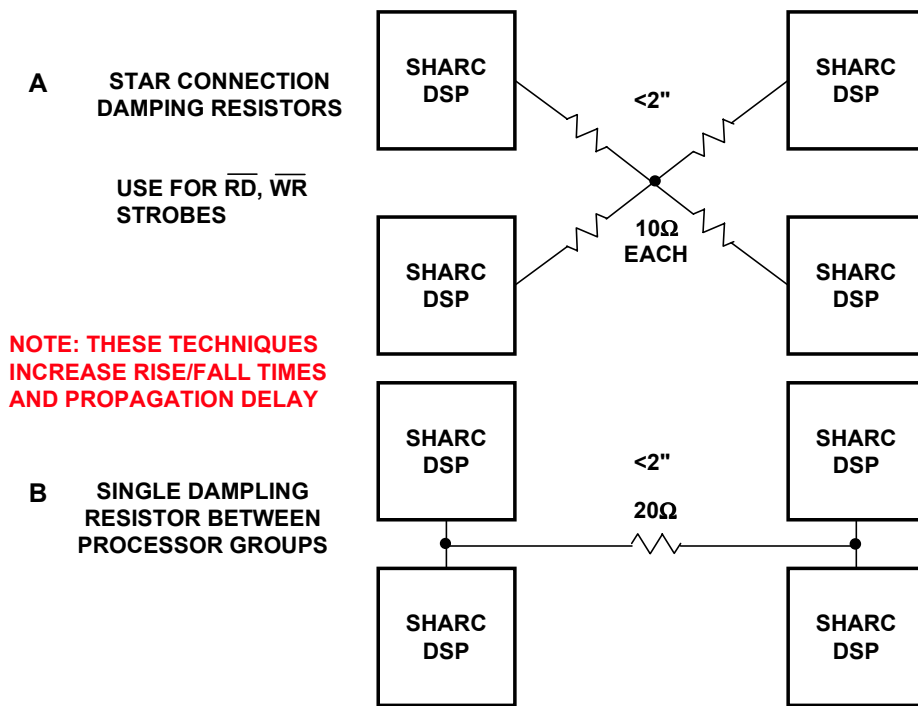


Figure 10.50

The only way to preserve 1ns or less rise/fall times over distances greater than about 2 inches without ringing is to use transmission line techniques. Figure 10.51 shows two popular methods of termination: end termination, and source termination. The end termination method (Figure 10.51A) terminates the cable at its terminating point in the characteristic impedance of the microstrip transmission line. Although higher impedances can be used, 50Ω is popular because it minimizes the effects of the termination impedance mismatch due to the input capacitance of the terminating gate (usually 5pF to 10pF). In Figure 10.51A, the cable is terminated in a Thevenin impedance of 50Ω terminated to +1.4V (the midpoint of the input logic threshold of 0.8V and 2.0V). This requires two resistors (91Ω and 120Ω), which add about 50mW to the total quiescent power dissipation to the circuit. Figure 10.51A also shows the resistor values for terminating with a +5V supply (68Ω and 180Ω). Note that 3.3V logic is much more desirable in line driver applications because of its symmetrical voltage swing, faster speed, and lower power. Drivers are available with less than 0.5ns time skew, source and sink current capability greater than 25mA, and rise/fall times of about 1ns. Switching noise generated by 3.3V logic is generally less than 5V logic because of the reduced signal swings and lower transient currents.

TERMINATION TECHNIQUES FOR CONTROLLED IMPEDANCE MICROSTRIP TRANSMISSION LINES

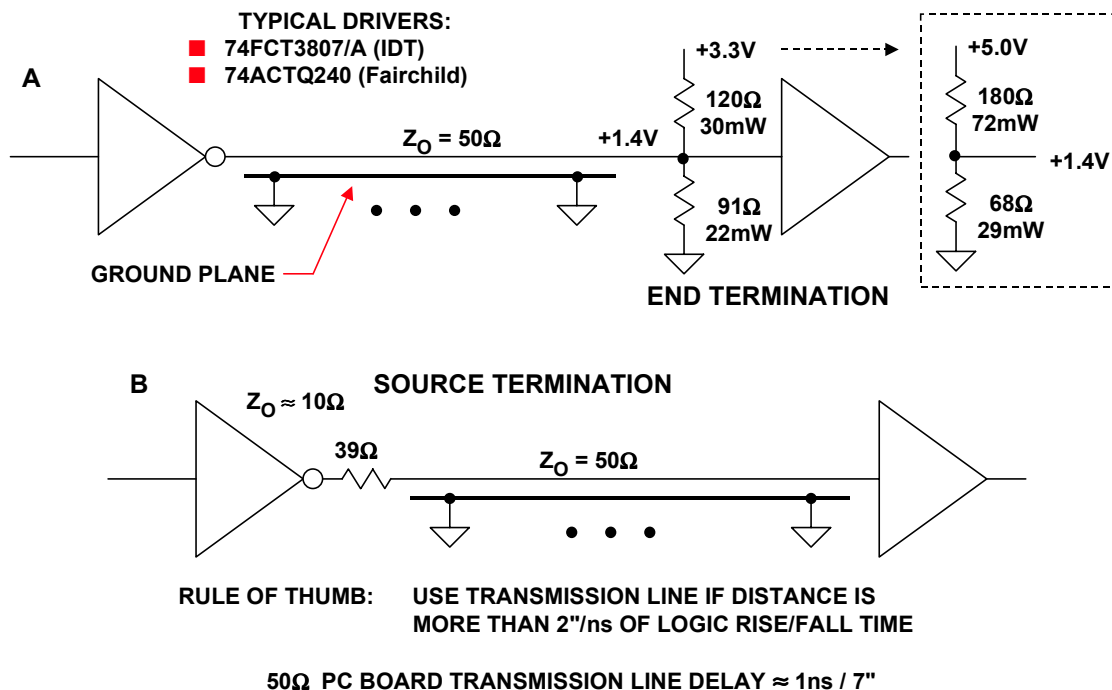


Figure 10.51

The source termination method, shown in Figure 10.51B, absorbs the reflected waveform with an impedance equal to that of the transmission line. This requires about 39Ω in series with the internal output impedance of the driver, which is generally about 10Ω. This technique requires that the end of the transmission line be terminated in an open circuit, therefore no additional fanout is allowed. The

source termination method adds no additional quiescent power dissipation to the circuit.

Figure 10.52 shows a method for distributing a high speed clock to several devices. The problem with this approach is that there is a small amount of time skew between the clocks because of the propagation delay of the microstrip line (approximately $1\text{ns}/7''$). This time skew may be critical in some applications. It is important to keep the stub length to each device less than $0.5''$ in order to prevent mismatches along the transmission line.

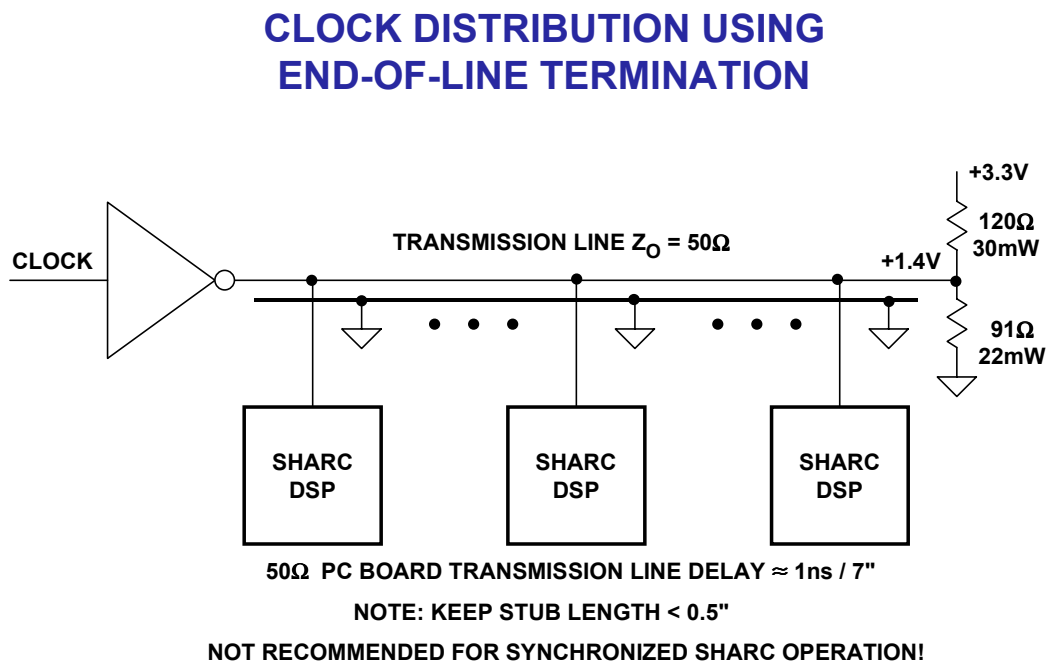


Figure 10.52

The clock distribution method shown in Figure 10.53 minimizes the clock skew to the receiving devices by using source terminations and making certain the length of each microstrip line is equal. There is no extra quiescent power dissipation as would be the case using end termination resistors.

Figure 10.54 shows how source terminations can be used in bi-directional link port transmissions between SHARC DSPs. The output impedance of the SHARC driver is approximately 17Ω , and therefore a 33Ω series is required on each end of the transmission line for proper source termination.

The method shown in Figure 10.55 can be used for bi-directional transmission of signals from several sources over a relatively long transmission line. In this case, the line is terminated at both ends, resulting in a DC load impedance of 25Ω . SHARC drivers are capable of driving this load to valid logic levels.

**PREFERRED METHOD OF CLOCK DISTRIBUTION
USING SOURCE TERMINATED TRANSMISSION LINES**

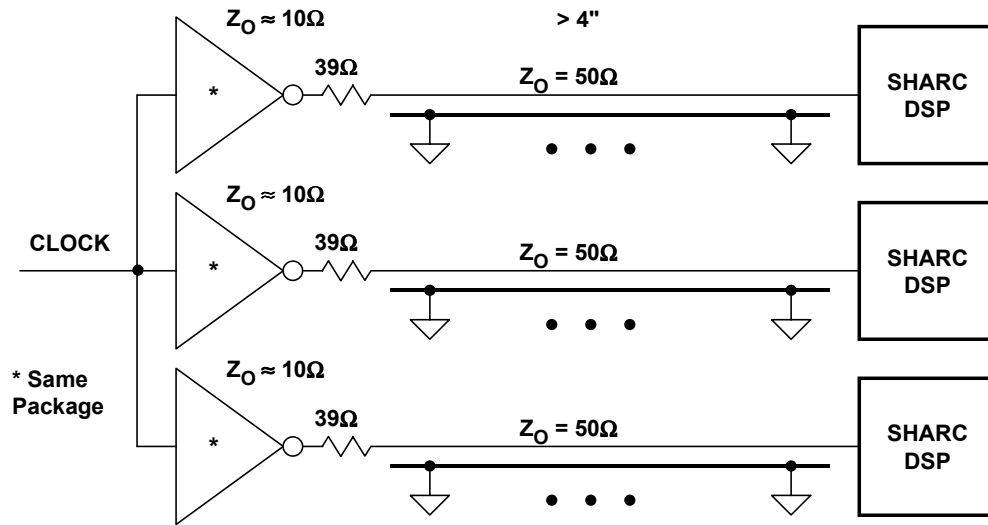


Figure 10.53

**SOURCE TERMINATION FOR BI-DIRECTIONAL
TRANSMISSION BETWEEN SHARC DSPs**

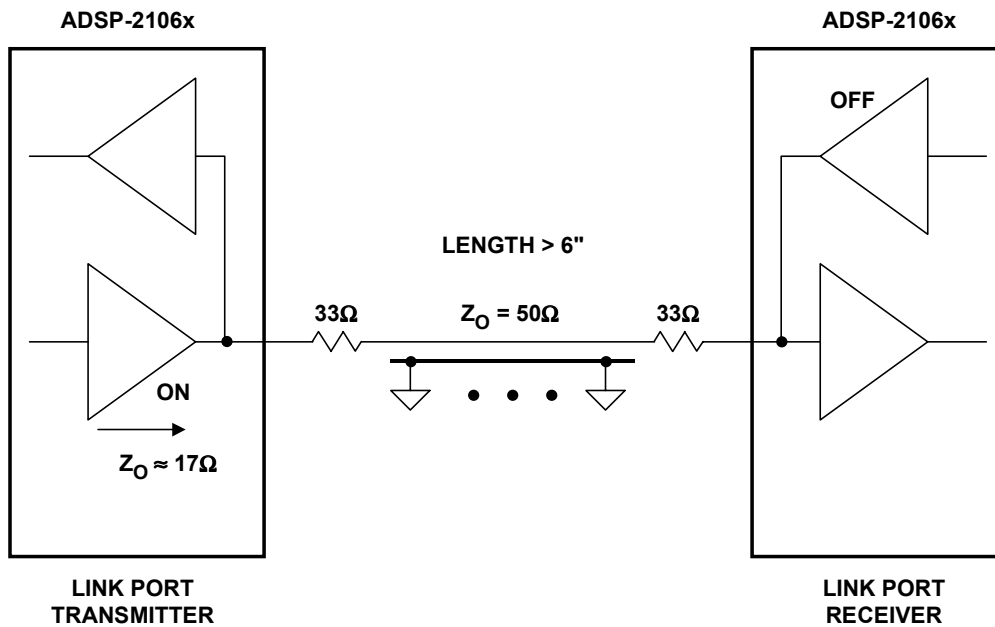
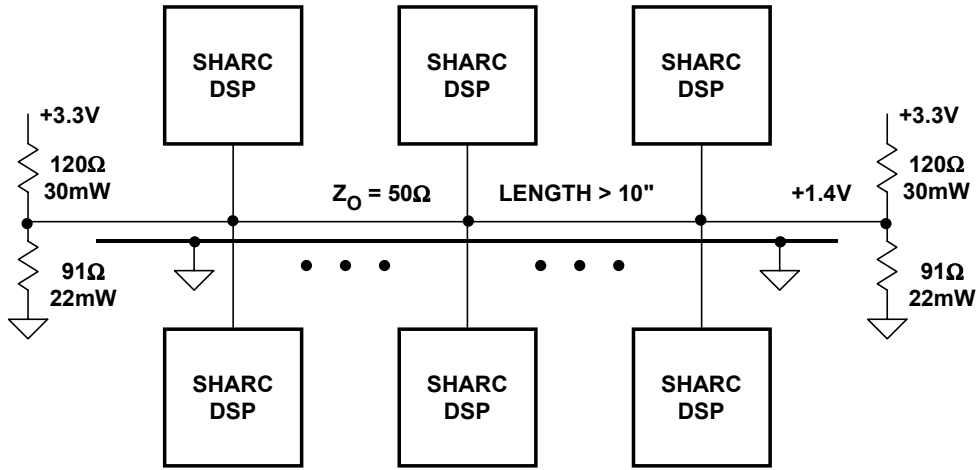


Figure 10.54

SINGLE TRANSMISSION LINE TERMINATED AT BOTH ENDS



NOTE: KEEP STUB LENGTH $< 0.5"$

NOT RECOMMENDED FOR CLOCKS IN SYNCHRONIZED SHARC OPERATION!

Figure 10.55

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