A Zero Voltage Switching Forward Converter Topology

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Abstract A zero voltage switching forward converter topology is presented in this paper. The topology employs an auxiliary circuit. Only a few small rating components and devices are added. The merits of the proposed topology include: lossless switching independent of the input and load conditions, simple control and power circuitry, and ability to operate in either voltage or current mode control. A steady state analysis is presented and the design procedure is illustrated. An 100W 300kHz prototype zero voltage switching forward converter is built which shows an efficiency improvement of approximately 5% as compared to a conventional hard switching forward converter.

1. Introduction

Telecommunication and computer systems are experiencing fast growth. These advanced systems have required distributed power supplies which have high efficiency and high power density and operate in constant frequency. In order to achieve high power densities, there is a trend to operate the power supplies at higher frequencies. However, when the switching frequency increases, the losses associated with the turn-on and turn-off of the devices in the power supplies also increase. Those losses are so significant that operation of the power supplies above 50kHz is prohibitive because of the low conversion efficiency and high cooling requirement.

To achieve high frequency operation, soft switching techniques are normally employed in the switch-mode power supplies. There are two types of soft switching, i.e., the zero voltage switching (ZVS) and the zero current switching (ZCS). It is shown in literature that ZVS is a better choice than ZCS in the MOSFET converter topologies [1].

In recent years, techniques such as the active clamp forward converters[2-8] have been developed. ZVS operation is realized in these converters. However, they have the following drawbacks: (i) needing an isolated, variable duty cycle gate drive for the clamp switch, (ii) requiring a modified PWM control technique to properly program the associated delays between gate drives as to achieve ZVS, (iii) losing ZVS under light load conditions, (iv) increasing the conduction losses, (v) unsuitable for the current mode control, and (vi) difficult to use due to the patent related legal issues.

This paper presents a ZVS technique for the forward converter topology which is able to overcome the above mentioned drawbacks. The proposed converter has (i) losses switching independent of line and load conditions, (ii) simple power and control circuitry, (iii) no increase in conduction losses, and (iv) ability to operate in either current and voltage mode control.

A steady state analysis of the circuit is presented and the design procedure is illustrated. Experiments on a prototype of 100W 5V 300kHz ZVS forward converter show an efficiency improvement of about 5% as compared to a conventional hard switching forward converter. The proposed converter topology, therefore, has potential in many low power level applications.

2. A ZVS Forward Converter Topology

Fig. 1 shows a ZVS forward converter topology employing an auxiliary circuit drawn inside the dashed line block.

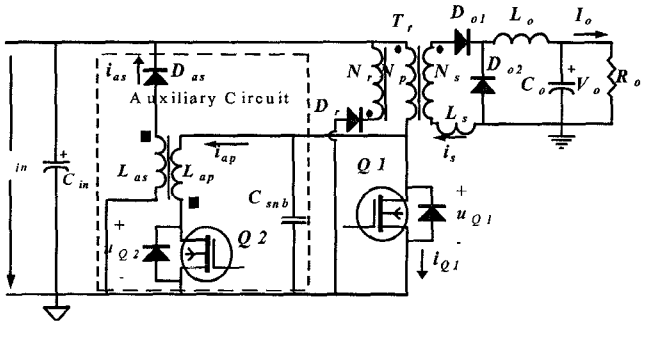


Fig. 1. A ZVS forward topology

In Fig. 1, *Q1* is the main switch, D_{o1} and D_{o2} are output rectifiers, L_o is the output inductor, C_{in} and C_o are the input and output capacitors, respectively, T_r is the power transformer with three windings: primary N_p, secondary N_s and tertiary N_r which is to reset the core of T_r, and D_r is a blocking diode in series with N_r.

The auxiliary circuit consists of a snubber capacitor C_{snb}, an auxiliary switch *Q2*, two coupled inductors L_{ap} and L_{as}, one blocking diode D_{as} and an additional small inductor L_s inserting into the secondary side.

3. Modes of Operation

Fig. 2 shows key waveforms of the proposed converter of Fig. 1. For each switching cycle, T_s, the converter operates in the following seven intervals.

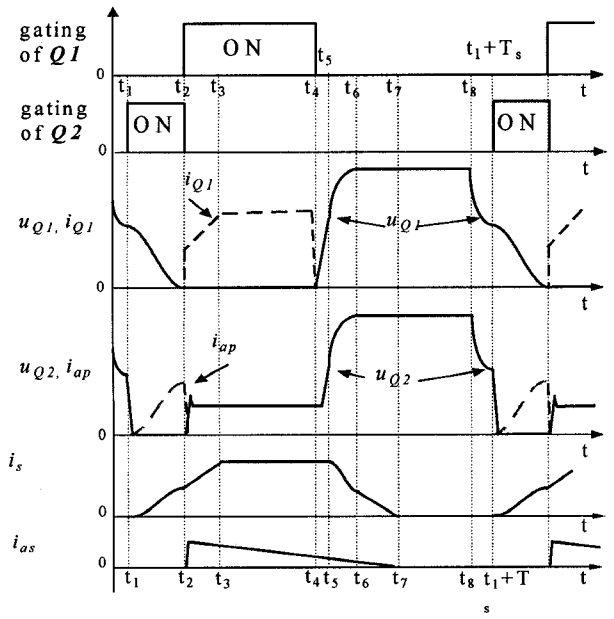


Fig. 2. Key waveforms of circuit in Fig. 1. The converter operates in seven modes per switching cycle. Variables are defined as shown in Fig 1.

3.1. Interval 1 ($t_1 < t \le t_2$)

Fig. 3(a) shows the circuit operation during this interval. At the beginning of this interval, *Q2* is switched ON. Thus, C_{snb}, L_{ap} and the power transformer form a resonant tank as shown in Fig. 4, and C_{snb} begins to discharge through L_{ap} and *Q2*.

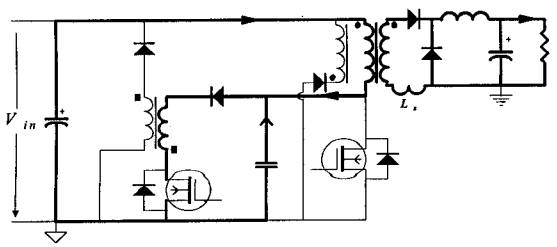
Assuming that L_m is much greater than L_{ap}, L_o is infinitive, and

$$L_s = n^2 L_{ap} \tag{1}$$

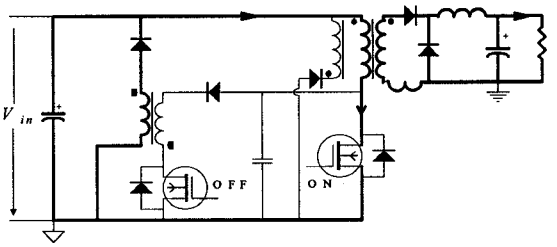
where, n is the reciprocal of the turns ratio of T_r. Hence, the falling drain voltage of *Q1* is found to be

$$u_{Q1}(t) = \frac{1}{2}V_{in} + (\frac{1}{2} + k)V_{in}\cos[\omega_n(t - t_1)] \tag{2}$$

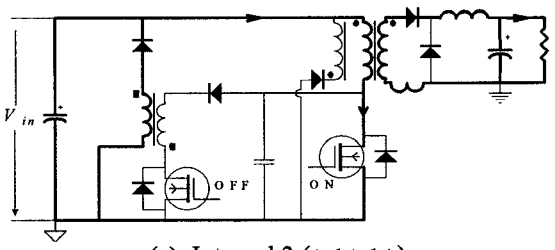
where, k is the factor by which the steady state drain



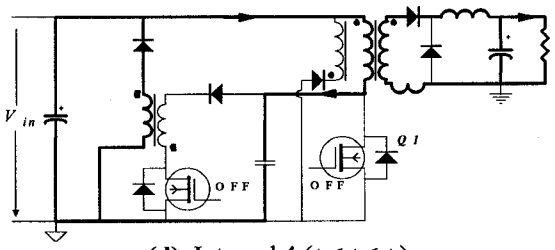
(a) Interval 1 ($t_1 < t \le t_2$)



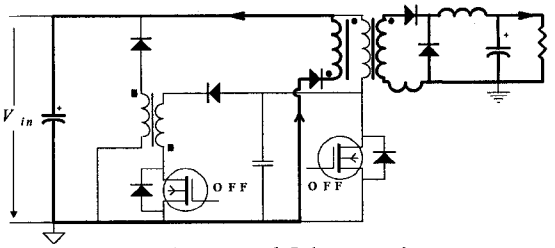
(b) Interval 2 ($t_2 < t \le t_3$)



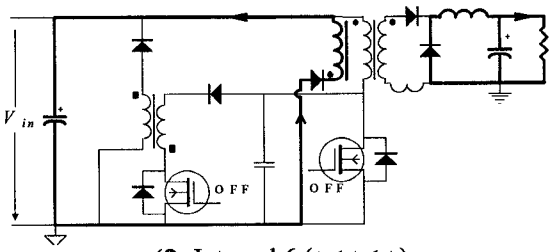
(c) Interval 3 ($t_3 < t \le t_4$)



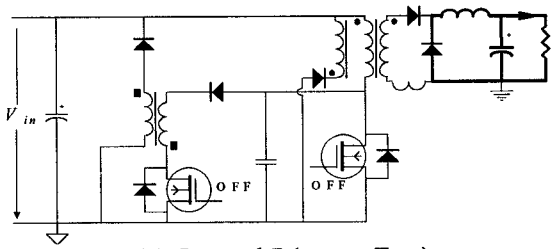
(d) Interval 4 ($t_4 < t \le t_5$)



(e) Interval 5 ($t_5 < t \le t_6$)



(f) Interval 6 ($t_6 < t \le t_7$)



(g) Interval 7 ($t_7 < t \le T_s + t_1$)

Fig. 3 Modes of operation of the converter of Fig. 1. The operation is divided into seven modes per switching cycle as depicted in (a) through (g).

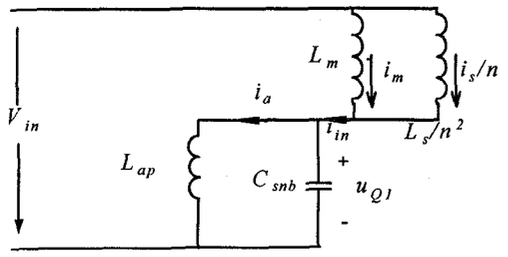


Fig. 4. The equivalent circuit of the discharging process in Interval 1. Variables are defined in Fig..

voltage of *Q1* deviates from V_{in} at the beginning of each switching cycle, and

$$\omega_n = \sqrt{\frac{1}{C_{snb}} \cdot \frac{L_{ap} + n^2 L_s}{n^2 L_{ap} L_s}} = \sqrt{\frac{2}{C_{snb} L_{ap}}} \tag{3}$$

It is noticed that, if k can be kept from going negative under all line and load conditions, u_{Q1} will always drop to zero within half the resonant period and maintain this zero voltage by latching in of the body diode of *Q1*. This can be achieved by the way described in the analysis of Interval 7 below.

The current flowing through L_{ap} is given by

$$i_{ap}(t) = \frac{V_{in}}{2L_{ap}}(t - t_1) + (\frac{1}{2} + k)\frac{V_{in}}{\omega_n L_{ap}} \sin[\omega_n (t - t_1)] \tag{4}$$

and the total primary current is

$$i_{in}(t) = \frac{V_{in}}{2L_{ap}}(t - t_1) + (\frac{1}{2} + k)(\frac{1}{\omega_n L_{ap}} - \omega_n C_{snb}) V_{in} \sin[\omega_n (t - t_1)] \tag{5}$$

Refer to Fig. 4, the secondary current of the transformer can be determined by

$$i_s(t) = \frac{1}{n} \cdot \frac{L_m}{L_m + n^2 L_s} i_{in}(t) \approx \frac{1}{n} i_{in}(t) \tag{6}$$

Since D_{as} is reverse biased and *Q1* is OFF,

$$i_{as}(t) = i_{Q1}(t) = 0 \tag{7}$$

At the end of this interval, i_{ap} reaches a peak value given by

$$I_{ap} = i_{ap}(t_2) = \frac{V_{in}}{2L_{ap}}(t_2 - t_1) \tag{8}$$

and the secondary current reaches a value given by

$$I_{s1} = i_s(t_2) = \frac{V_{in}}{2nL_{ap}}(t_2 - t_1) \tag{9}$$

3.2. Interval 2 ($t_2 < t \le t_3$)

Fig. 3(b) shows the circuit operation during this interval. At the beginning of this interval, *Q1* is switched ON under zero voltage condition, hence there are no switching losses. *Q2* is switched OFF. The abrupt stop of current in L_{ap} reverses the voltage polarity at the dotted ends of the coupled inductors, and D_{as} becomes forward biased and starts to conduct, feeding the stored energy in the coupled inductors back to the input line. When D_2 is conducting, L_{as} sees a constant voltage V_{in}, then the current flowing through it decreases linearly as given by

$$i_{as}(t) = I_{as} - \frac{V_{in}}{L_{as}}(t - t_2) \tag{10}$$

where I_{as} is the initial current of this process and is determined by

$$I_{as} = I_{ap}\sqrt{L_{ap}/L_{as}} \tag{11}$$

Through coupling, L_{ap} sees a reflected voltage, which gives *Q2* a voltage stress at its turnoff, as given by

$$u_{Q2}(t) = V_{in}\sqrt{L_{ap}/L_{as}} \tag{12}$$

As L_s sees a constant voltage nV_{in}, the secondary current rises linearly,

$$i_s(t) = \frac{nV_{in}}{L_s}(t - t_2) + I_{s1} \tag{13}$$

The current in *Q1* follows the secondary current through the coupling of the transformer windings. Both D_{o1} and D_{o2} are conducting, to give the total current in L_o. But current in D_{o1} is rising and that in D_{o2} is falling, linearly.

3.3. Interval 3 ($t_3 < t \le t_4$)

Fig. 3(c) shows the circuit operation during this interval. At the beginning of this interval, current in D_{o1} reaches the value of the current in L_o. Current in D_{o2} exhausts. Power is delivered to the load in the same manner as in a conventional forward converter, that is,

$$i_s(t) = I_o \tag{14}$$

$$i_{Q1}(t) = nI_o \tag{15}$$

3.4. Interval 4 ($t_4 < t \le t_5$)

Fig. 3(d) shows the circuit operation during this interval. At the beginning of this interval, *Q1* is switched OFF. L_s and C_{snb} comprise a resonant tank as shown in Fig. 5. Currents in D_{o1} and that into C_{snb} fall

resonantly, corresponding to the resonant rise of the drain voltage of $Q1$ which is governed by

$$u_{Q1}(t) = V_{in} - V_{in}\cos[\omega_r(t-t_4)] + \frac{nI_o}{\omega_r C_{snb}}\sin[\omega_r(t-t_4)] \quad (16)$$

where

$$\omega_r = 1/\sqrt{n^2 L_s C_{snb}} \quad (17)$$

It is noticed that C_{snb} slows down the rise of the drain voltage. Thus, a ZVS is facilitated in $Q1$ in this way at turn-off.

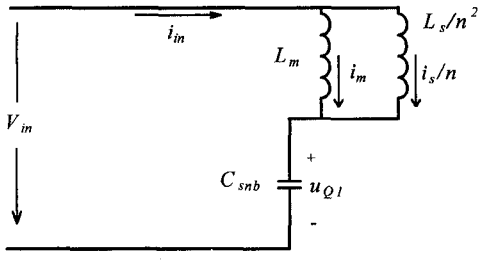


Fig. 5. The equivalent circuit of the charging process in Interval 5. The variables are defined in Fig. 1.

At the same time, L_s sees a voltage $n(V_{in}-u_{Q1})$. Thus,

$$i_s(t) = \frac{1}{n}\cdot\{\omega_r C_{snb} V_{in}\sin[\omega_r(t-t_4)] + nI_o\cos[\omega_r(t-t_4)]\} \quad (18)$$

At the end of this interval, the drain voltage of $Q1$ reaches a peak value of $2V_{in}$, and the secondary current reaches a value given by

$$I_{s2} = i_s(t_5) \quad (19)$$

3.5. Interval 5 ($t_5 < t \le t_6$)
Fig. 3(e) shows the circuit operation during this interval. At the beginning of this interval, D_r becomes forward biased and starts to conduct, and thus clamps the voltage of the primary windings of T_r at a voltage of $-V_{in}$, and the drain of $Q1$ is clamped at $2V_{in}$. In this way, the core of T_r is reset. L_s sees a constant negative voltage, $-nV_{in}$. Thus,

$$i_s(t) = I_{s2} - \frac{nV_{in}}{L_s}(t-t_5) \quad (20)$$

This interval continues until i_s reaches zero.

3.6. Interval 6 ($t_6 < t \le t_7$)
Fig. 3(f) shows the circuit operation during this interval. At the beginning of this interval, the current in L_s, or the secondary current, exhausts. Then D_{o1} is reverse biased and D_{o2} freewheels the total inductor current in L_o. As the magnetizing current does not reach zero before the end of this interval, the drain voltage of the main switch $Q1$ is still clamped until the end of this interval..

3.7. Interval 7 ($t_7 < t \le t_1+T_s$)
Fig. 3(g) shows the circuit operation during this interval. At the beginning of this interval, the core resetting finishes and the clamp action is removed. C_{snb} and the magnetizing inductance L_m of T_r forms a resonant loop, with a slower resonant frequency due to the largeness of L_m. The drain voltage of $Q1$ intends to ring about a voltage level of V_{in}, starting from $2V_{in}$. This process can be describes as

$$u_{Q1}(t) = V_{in}\{1+\cos[\omega_0(t-t_7)]\} \quad (21)$$

At the end of this interval, one switching cycle finishes. The drain voltage of $Q1$ reaches a steady state value equal to the voltage at the beginning of this cycle. Accordingly, the factor by which this steady state voltage deviates from V_{in} can be found as

$$k = \cos[\omega_0(T_s + t_1 - t_7)] \quad (22)$$

where,

$$\omega_0 = 1/\sqrt{L_m C_{snb}} \quad (23)$$

As indicated in Section 3.1, it is expected that k maintains positive under all operating conditions. This can be achieved, as revealed in Eqs. (22) and (23), by selecting a relatively large L_m so as to prevent k from going negative.

Following Interval 7, the process repeats from Interval 1 through 8.

4. Design Procedure

In this section, a design procedure to select the various components of the auxiliary circuit of Fig. 1 is given. The selection criteria for the main power circuit are not given here as it is a conventional circuit which has been extensively published in the literature.
Assume that the following parameters are known:
(i) D_{max}--maximum duty cycle of $Q1$,
(ii) f_s--switching frequency,
(iii) L_m--magnetizing inductance of T_r,
(iv) n--reciprocal of the turns ratio of T_r,
(v) V_o--output voltage, and
(vi) the input voltage range.

4.1 Auxiliary switch duty cycle D_{aux}
It corresponds to a half of the resonant period of the tank consists of C_{snb}, L_{ap} and L_s. In order not to affect the core resetting of the power transformer, D_{aux} should be limited by:

$$D_{aux} \le (1-2\cdot D_{\max}) \tag{24}$$

D_{aux} may also be determined by the control chip like UC3855, where it is fixed to about 0.08. Thus the design should observe this factor.

4.2. Snubber capacitor C_{snb}

The value of C_{snb} determines the rise time of the drain voltage of $Q1$ at its turn-off, as described in Eq. (16). For a very short duration, it is approximated that

$$\Delta u_{Q1}(t) \approx \frac{nI_o}{C_{snb}}\Delta t \tag{25}$$

Limiting the rise of u_{Q_1} below V_{in} within the demanded time t_r. Thus, from Eq. (25),

$$C_{snb} \ge \frac{nI_o}{V_{in}} t_r \tag{26}$$

On the other hand, the rise time should not exceed the gap left by $2D_{max}$ and D_{aux}, which gives a limit

$$t_5 - t_4 \le (1-2D_{\max} - D_{aux})T_s \tag{27}$$

Combining Eqs. (25) and (27),

$$C_{snb} \le \frac{n I_o}{2V_{in}}(1-2D_{\max} - D_{aux})T_s \tag{28}$$

4.3. Coupled inductors, L_{ap}, L_{as}, additional inductor L_s

L_{ap} should be selected so that the duration of Interval 1 is a half of the resonance period determined by Eq. (3). L_{as} should be large enough so as to suppress the turn-off voltage stress on $Q2$ as described in Eq. (12). But L_{as} should also be limited so that the release of the stored energy after Interval 1 can finish within one switching cycle. Hence, these inductors values are found to be as follows.

$$L_{ap} = \frac{2D_{aux}^2}{\pi^2 f_s^2 C_{snb}} \tag{29}$$

$$L_{as} \le (\frac{1-D_{aux}}{D_{aux}})^2 L_{ap} \tag{30}$$

$$L_s = n^2 L_{ap} \tag{31}$$

4.4. Auxiliary switch $Q2$

In selection, trade off should be made between the least inherent capacitance and the least on-resistance so as to result in the least total losses in $Q2$. Its voltage rating is the same as of $Q1$. Its current rating should be able to handle the peak discharging current given by Eq. (8).

4.5. Blocking diode D_{as}

It is a fast recovery diode with low forward voltage drop. The maximum reverse voltage it sustains is given by

$$V_{R\_D2} = (1+\sqrt{\frac{L_{as}}{L_{ap}}}V_{in\_\max} + \sqrt{\frac{L_{as}}{L_{ap}}}\frac{V_o}{n} \tag{32}$$

where V_{in_max} is the high level of the input voltage.

It should be able to handle a peak current given by Eq. (11).

4.5. A design example

A design example is given below. Table 1 shows the principle specifications and parameters of the main power circuit of the prototype forward converter. Table 2 shows the parameters of the auxiliary circuit in the prototype converter, which are selected according to the selection criteria presented above.

Synchronous rectifiers are employed in the prototype converter according to the design procedure presented in [8].

specification	selection	parameter	selection
V_{in-min}	40V	L_m	150μH
V_{in-max}	60V	n	1/3
P_o	100W	C_o	200μF
V_o	5V	$Q1$	IFR640*
$D_{\max}$	0.40	D_{o1} and D_{o2}	MTP75N05*
f_s	300kHz	Controller	UC3855

* Two in parallel. Ratings of IFR640 are 200V and 18A, and those of MTP75N05 are 50V and 75A

Table 1. Principle specifications and parameters of the main power circuit of the prototype forward converter.

parameter	selection	parameter	selection
C_{snb}	10nF	L_{as}	100μH
L_{ap}	3μH	$Q2$	IRF634*
L_s	0.33μH	D_1, D_2	HFA08TB*

* Ratings of IRF634 are 250V and 8A, and those of HFA08TB are 600V and 8A.

Table 2. Components of the auxiliary circuit in the prototype forward converter.

5. Experimental Results

A prototype ZVS forward converter has been built based on the design example. The principle specifications and parameters of the converter are shown in Tables 1 and 2. The converter is operated at 300kHz and outputting 100W at 5V.

Fig. 6 shows the characteristic waveforms of the voltage and current of the main switch *Q1*. The negative portion of the current waveform is owing to the conduction of the body diode of *Q1* after its drain voltage reaches zero in Interval 1.

Fig. 7 shows the characteristic waveforms of the auxiliary switch. It does have some turn-off losses, but this type of losses can be further reduced by depressing the voltage stress at turn-off. This can be fulfilled by increasing the turns ratio of the coupled inductors (refer to Eq. (12)). The losses associated with *Q2* are much less than the saved switching losses from the main switch *Q1*. Hence the total switching losses are much less in the ZVS operation than in the hard switching operation.

Figs. 8, 9, 10 and 11 show key waveforms of the main switch *Q1* and the auxiliary switch *Q2*, respectively, under different line and load conditions. It is seen that ZVS is always achieved.

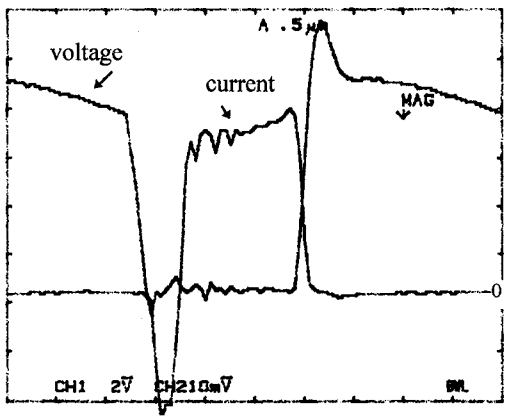


Fig. 6. The experimental results of the drain voltage and current of *Q1* in a prototype ZVS converter of Fig. 3.1. Operating conditions: P_o=100W, V_{in}=50V, f_s=300kHz. Scales: vertical-2A/div., 20V/div., horizontal- 0.5μs/div.

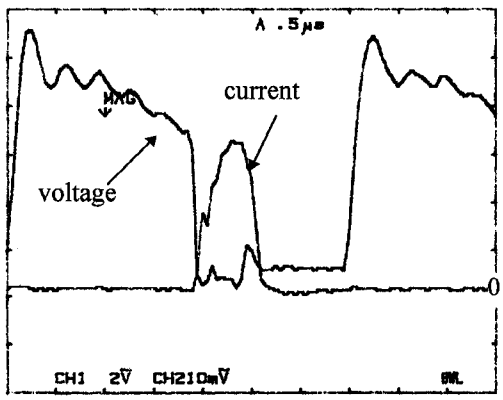


Fig. 7. The Experimental results of the drain voltage and current waveforms of *Q2* in Fig. 1. The operating conditions are the same as in Fig. 6. Scales: vertical-1A/div., 20V/div., horizontal- 0.5μs/div.

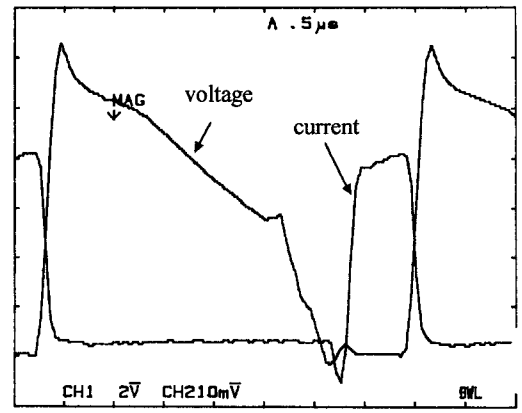


Fig. 8. Experimental results: the current and voltage of *Q1* at high line full load. P_o=100W, V_{in}=60V, f_s=300kHz. Scales: vertical-20V/div., 2A/div; horizontal-0.5μs/div.

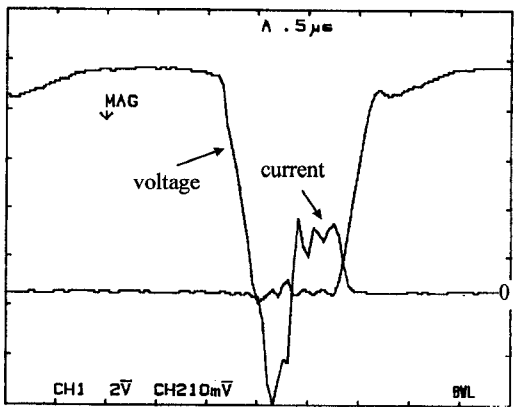


Fig. 9. Experimental results: the current and voltage of *Q1* at high line light load. Operating condition: P_o=20W, V_{in}=60V, f_s=300kHz. Scales: vertical-20V/div., 2A/div., horizontal-0.5μs/div.

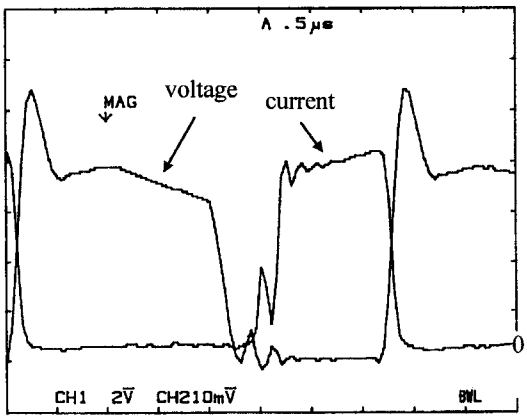


Fig. 10. Experimental results: the current and voltage of *Q1* at low line full load. Operating conditions: P_o=100W, V_{in}=40V, f_s=300kHz. Scales: vertical-20V/div., 2A/div.; horizontal-0.5μs/div.

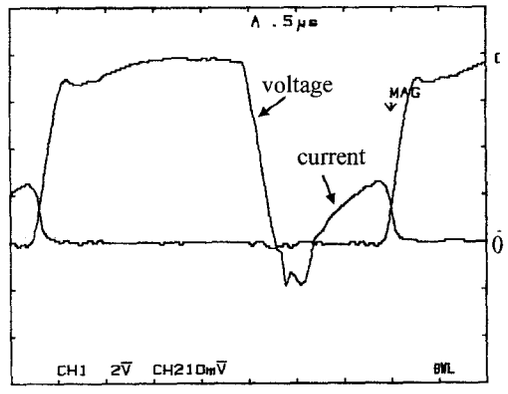


Fig. 11. Experimental results: the current and voltage of *Q1* at low line light load. Operating conditions: P_o=20W, V_{in}=40V, f_s=300kHz. Scales: vertical-20V/div., 2A/div., horizontal-0.5μs/div.

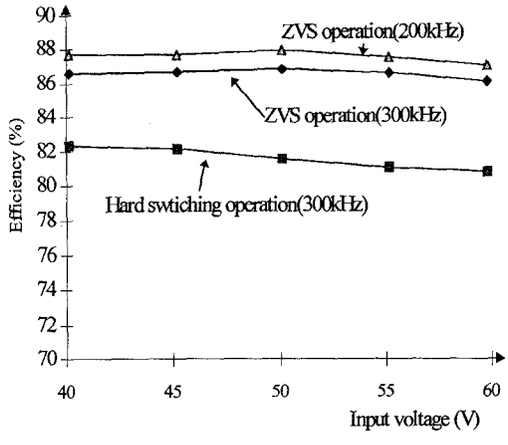


Fig. 12. The efficiencies vs. input voltage of the prototype converter in ZVS operation and hard switching operation of the forward converter. Operating conditions: P_o=100W, V_o=5V.

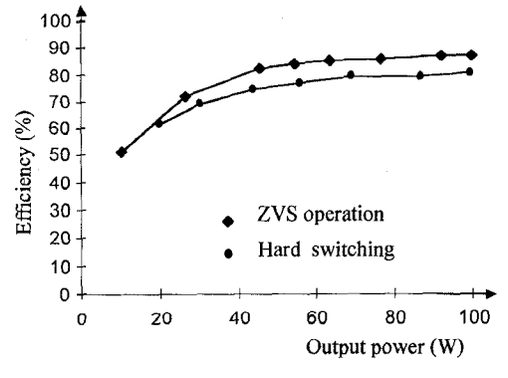


Fig. 13. The efficiencies vs. load of the prototype converter in ZVS operation and hard switching operation. Operating conditions: V_{in}=50 V, f_s=300 kHz

Fig. 12 shows the experimental results the efficiency vs. input voltage under full the load condition (100W). The comparison between the efficiencies of the ZVS and the hard switching operation of the prototype forward converter is made. The hard switching forward also employs synchronous rectifiers. The comparison shows that ZVS indeed makes a significant increase (by about 5%) in efficiency.

ZVS operation at frequency of 200 kHz is also tested, where the snubber capacitor and the primary of the coupled inductor are adjusted to suit for this frequency. The efficiency is about 1% higher than that at 300kHz. The gain in efficiency is due to the reduced switching losses in the auxiliary switch, and the reduced losses in the gate drives of the synchronous rectifiers.

Fig. 13 shows the efficiency vs. load under given input voltage for both the proposed and conventional circuits. The proposed circuit always has better efficiency than the conventional hard switching forward converter.

6. Conclusions

In this paper a ZVS forward converter topology has been presented and analyzed. The proposed topology maintains ZVS independent of load and line conditions and has a simple circuitry. The experimental results show that the proposed topology has about 5% higher efficiency than the conventional hard switching forward topology. The proposed topology is hence proved to be useful in many low power level industrial applications.

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