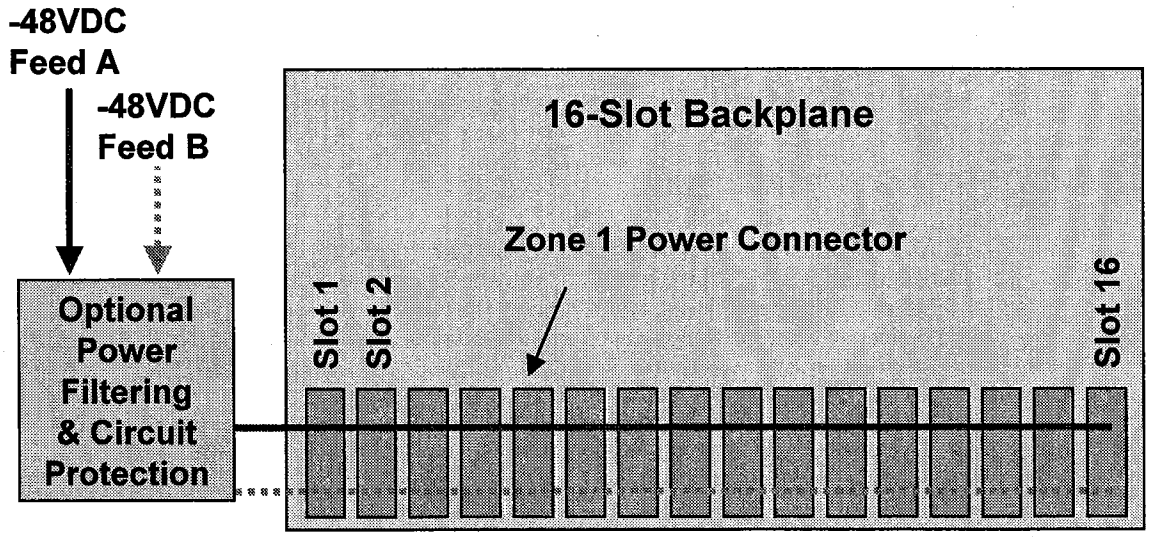
Power distribution 4

This section describes power distribution at the Shelf and Board level for PICMG® 3.0 products. Any information relating to Frame or Cabinet level power distribution is for information only and is not mandatory. Safety and regulatory requirements are discussed in Section 7, "Regulatory guidelines."

4.1 Dual -48 VDC power distribution

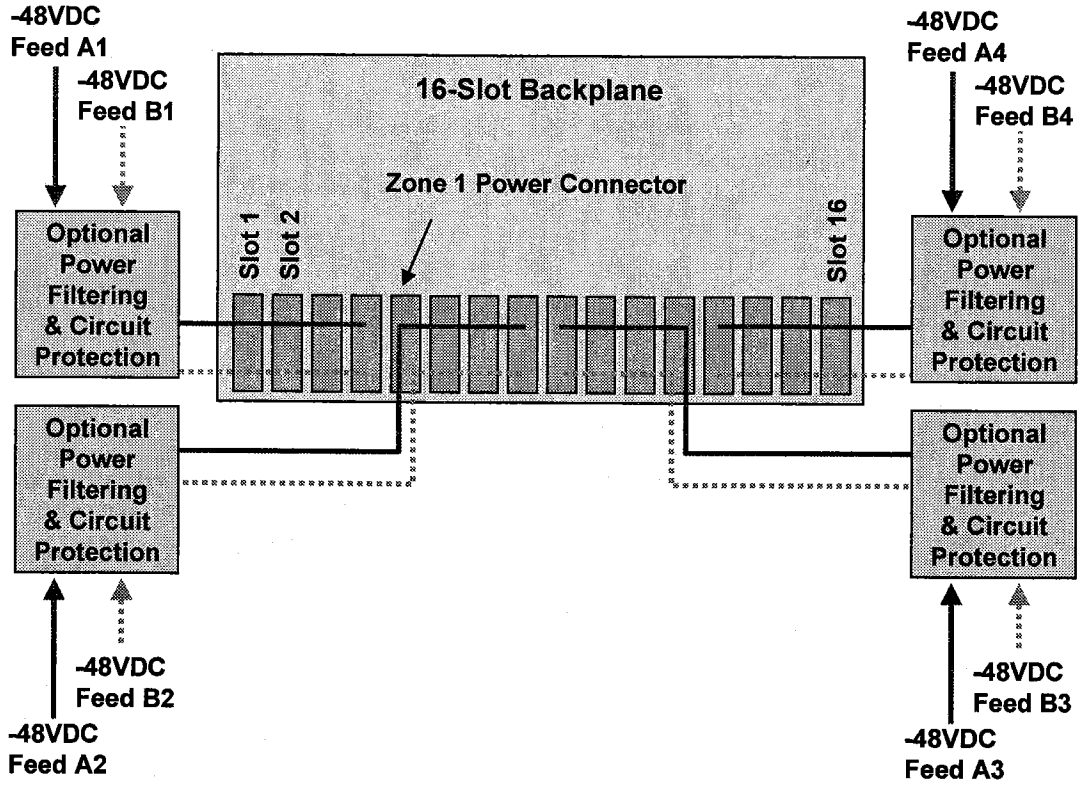
Dual, redundant -48 VDC Feeds are provided to each Frame from the one or two power plants within a facility. In some facilities, a signal-conditioning panel, usually mounted at the top of the Frame, provides filtering to minimize radiated and conducted noise, Feed cable inductor compensation, overcurrent protection, and voltage ripple. The two primary Feeds are typically split into a number of branches but remain electrically isolated. These branches are then also fused and filtered to prevent downstream shorts and malfunctions from propagating beyond a single Shelf or sub-Shelf. Shelves requiring modest power may be fed by a single pair of Feeds or by multiple pairs of Feeds to keep the current per Feed to a modest level. Figure 4-1, "Shelf level power distribution example (2 Feeds)," illustrates this concept. (For simplicity, fusing is not shown in the diagram.)

Figure 4-1 Shelf level power distribution example (2 Feeds)



Multiple branches from each Battery Plant may also be used to minimize fault domains and increase reliability. In cases where multiple branches are used from each Battery Plant, the Backplane is segmented to maintain isolation between all branches, as shown in Figure 4-2, "Shelf level power distribution example (8 Feeds)."

Figure 4-2 Shelf level power distribution example (8 Feeds)



For more information, see Section 4.1.3, "Single or multiple Feeds to the Shelf and Backplane."

4.1.1 Power architecture

PICMG® 3.0 Shelves **shall** provide (and Boards **shall** receive) dual DC Feeds (referred to in this document as "Feed A" and "Feed B"). The convention used will specify negative voltages, since the positive side of each Feed, while isolated from any Logic Grounds, **may** be referenced to earth in a typical installation. While the term -48 VDC is used to generically refer to the input voltage, each Feed **may** vary as shown in Section 4.1.2, "Supported voltage levels."

In Frame level power distribution, power filtering and circuit protection are expected to be within the distribution panel on the Frame. Shelves without Shelf-level power filtering and circuit protection require Frame level power distribution. Shelves with Shelf-level power filtering and circuit protection can be used with or without Frame level power distribution.

PICMG® 3.0 Shelves **shall** distribute filtered power Feeds to each Front Board through the Zone 1 connector as described in Section 2.4.1.1, "Description." This connector **shall** be mounted on a Backplane that provides power to each Board. PICMG® 3.0 systems **shall** have only the dual, redundant -48 VDC Feeds available for powering Boards.

Boards **shall** be built with LOGIC_GND used as the GND reference for the local power generated via isolating power supplies. These are normally DC/DC converter(s) powered by the dual -48 VDC power Feeds supplied through the P10 connector. Boards **shall** provide DC isolation

between the -48 VDC power domain and the LOGIC_GND-based power domain. All conduits of the -48 VDC domains and the isolated local power domain **shall** observe the mutual Creepage and Clearance distances between conduits of different power domains.

The -48 VDC power domain on a Board **should** be limited to structures required between the Backplane power connector and the isolating DC/DC converter(s) generating the local power(s), such as fuses, diodes, filters, capacitors, and pre-charge circuitry.

Although the VRTN potential of the -48 VDC power is grounded next to the power source and possibly in other areas throughout the facility, the realities of a building-wide power distribution network in a telecommunication environment are such that the SHELF_GND for a Frame, Shelf, or Board can see a DC potential difference of several Volts from the earth potential of the central office. (For example, GR-1089 [R6-1] requires equipment to deal with a 3 VDC differential.). Boards and Shelves **shall** provide DC isolation between LOGIC_GND and SHELF_GND, except as noted in Section 4.2.2, "Shelf Ground and –48 VDC return."

Boards **shall** provide DC Isolation between the -48 VDC power domains and SHELF_GND as well. Refer to Section 4.2.2, "Shelf Ground and –48 VDC return," for further guidance to grounding.

Any power required by a RTM (Rear Transition Module) **shall** only be provided by the Front Board to which it is connected through the Zone 3 connector.

4.1.2 Supported voltage levels

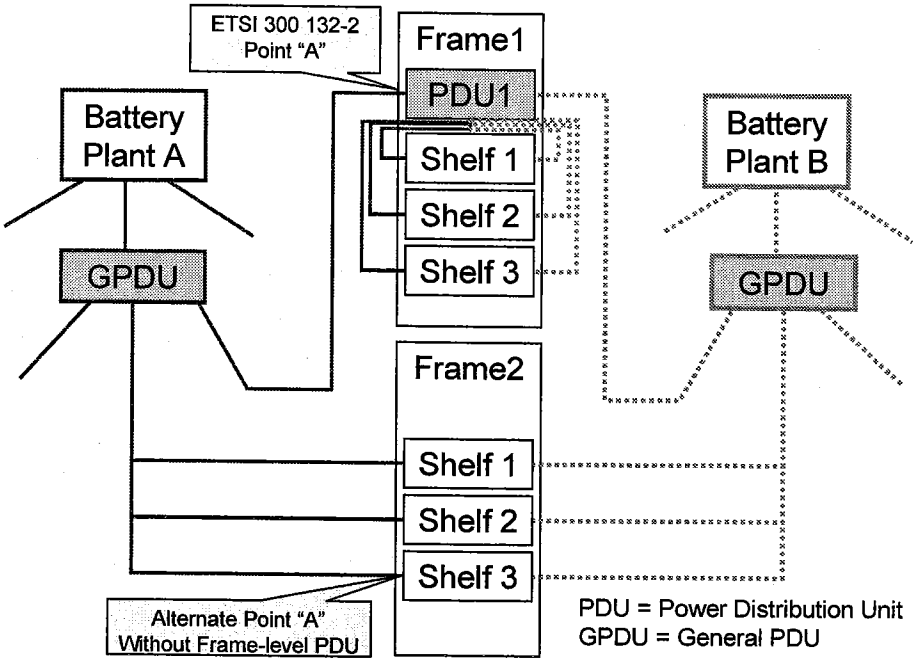
4.1.2.1 Voltage level background information (informative)

Table 4-1 ETS 300 132-2 static voltage levels

	-48 VDC systems	-60 VDC systems
Nominal operating voltage	-48 VDC	-60 VDC
Maximum operating voltage	-57 VDC	-72 VDC
Minimum operating voltage	-40.5 VDC	-50 VDC
Degraded operating voltage	-40.5 VDC to -44 VDC	Not specified
Non-operating voltages with no equipment damage	0 VDC to -40.5 VDC, -57 VDC to -60 VDC	0 VDC to -50 VDC, -72 VDC to -75 VDC

These operating voltages are measured at "A," which is the input to the telecommunications equipment (see Figure 4-3, "Power distribution with and without a Frame-level PDU"). This may be thought of as "the end of the power cable as it enters the Frame." Some reduction in services or capabilities is allowed in the degraded operating voltage range. Note that the Zone 1 power connector supports both -48 VDC and -60 VDC systems, but ETS 300132-2 states that -60 VDC systems are expected to be supported for a transitional period and that -48 VDC systems will be the standard power interface at some time in the future. Also, note that equipment is not required to operate during the non-operating ranges listed above, but the equipment must be able to restart operation after operating voltages are re-established.

Figure 4-3 Power distribution with and without a Frame-level PDU



4.1.2.2 Voltage level requirements

Shelf requirements

- PICMG® 3.0 Shelves **shall** be fully operational over a supply voltage range of -44 VDC to -72 VDC.
- PICMG® 3.0 Shelves **may** support a supply voltage lower than -40.5 VDC.
- PICMG® 3.0 Shelves **may** provided degraded support when operating below -44 VDC.
- PICMG® 3.0 Shelves **shall not** be damaged by supply voltages in the range of 0 VDC to -75 VDC.
- Input power distribution circuits **shall** comply with the appropriate requirements in the IEC 60950, UL 60950, and EN 60950 for TNV-2 circuits.

Board and FRU requirements

- PICMG® 3.0 Boards **shall** be fully operational over a supply voltage range of -43 VDC to -72 VDC.
- PICMG® 3.0 Boards **may** support a supply voltage lower than -39.5 VDC.
- PICMG® 3.0 Boards **may** provide degraded support when operating below -43 VDC. When a PICMG® 3.0 Board is operating in this "degraded support" range, it **should** continue operating when the low voltage transients as described in Section 4.1.4.3, "Transients," but is not required to do so.
- PICMG® 3.0 Boards **shall not** be damaged by supply voltages in the range of 0 VDC to -75 VDC.

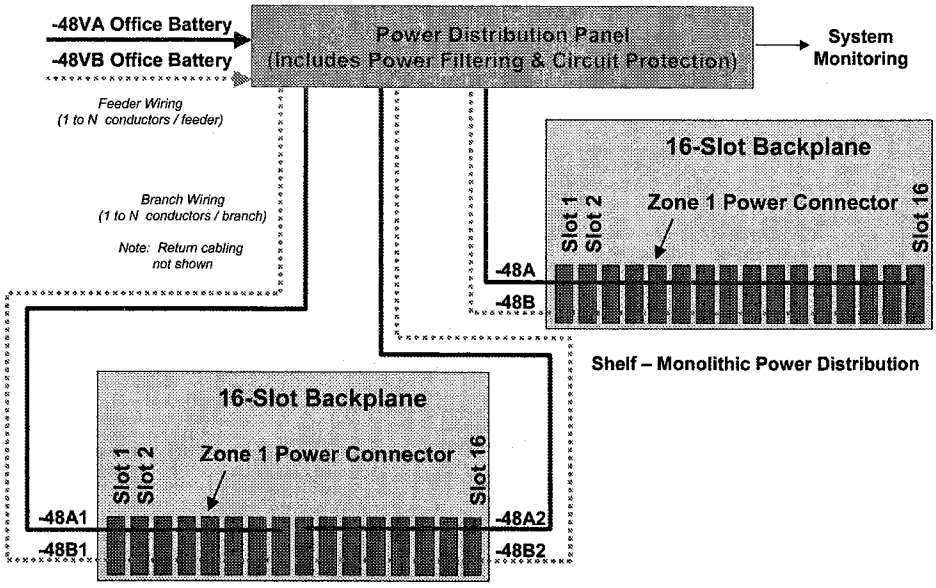
- PICMG® 3.0 Boards **should** provide for the management subsystem to be powered when the supply voltage is as low as -38 VDC.
- Input power distribution circuits **shall** comply with the appropriate requirements in the IEC 60950, UL 60950, and EN 60950 for TNV-2 circuits.
- PICMG® 3.0 Boards **shall** have a voltage cutoff threshold between -32 VDC and -36 VDC. Boards **shall** draw no more than 10 mA if the input voltage level drops below the Board's cutoff level for more than 2 seconds.
- If power drops below the minimum supported Board-level input voltage for longer than the period of the transients in Section 4.1.4.3, "Transients," PICMG® 3.0 Boards **may** disable Payload power until the Board-level input voltage range has exceeded the degraded support threshold (-43 VDC) for at least five (5) seconds.
- All other Shelf elements feeding off the -48 VDC power inputs **should** meet the same requirements as Boards.

There will typically be some voltage drop within a Shelf due to filtering (see Section 4.1.5, "Filtering") and Shelf-level overcurrent protection plus a voltage drop across the Backplane traces. For that reason, the lower Board-level voltage requirements are one Volt lower than what is seen on the input to the Shelf. Note that ripple and hash requirements are called out in Section 4.3.2.1, "Power supply noise voltages."

4.1.3 Single or multiple Feeds to the Shelf and Backplane

PICMG® 3.0 systems are capable of dissipating as much as 200 W per single-Slot Board in addition to the power consumption requirements of the fans and other Shelf elements. In a 16-Slot Shelf, over 3200 W of office battery power must be provided through Battery Plant wiring. Either monolithic load wiring (one set of power inputs for the Shelf) or distributed load wiring (multiple sets of power inputs, each providing power to a subset of Shelf Slots) **may** be utilized, as shown in Figure 4-4, "Multiple power Feeds to a Shelf." Regardless of wiring topology, all wiring **shall** be sized to carry the full current load under fault conditions.

Figure 4-4 Multiple power Feeds to a Shelf



Monolithic load wiring **may** be implemented using either single- or multi-conductor methods. If multi-conductor wiring is used, all conductors for a given power input **shall** be terminated on the same power lug at the Shelf. The maximum voltage drop between the power lug and the Zone 1 power pins at any Slot **shall** be 1.0 V.

Distributed load power wiring provides connections between the Shelf and multiple power sources. The wiring for each power input, whether single-conductor or multi-conductor, **shall** be attached to a unique power lug on the Backplane. The maximum voltage drop between the power lug and the Zone 1 power pins at any Slot **shall** be 1.0 V.

4.1.4 Fusing and fault protection

In this section, the term "fuse" or "fusing" will be used to describe any circuit protection devices that are intended to interrupt DC power in the event of an over current situation. These devices might include conventional fuses, circuit breakers, in-line semiconductor devices, such as IGBTs (Insulated Gate Bipolar Transistors) or FETs (Field Effect Transistors), or other protection devices.

Fusing is a complex issue, and this specification describes the minimum required for PICMG® 3.0 compliance. Individual designs can incorporate more sophisticated fusing and circuit protection, although care **should** be taken to ensure that the overall system management architecture as described in Section 3, "Shelf management," can determine where faults, due to fuse opening or other circuit protection devices, have occurred.

Fusing and power monitoring at the Frame level are outside the scope of this document.

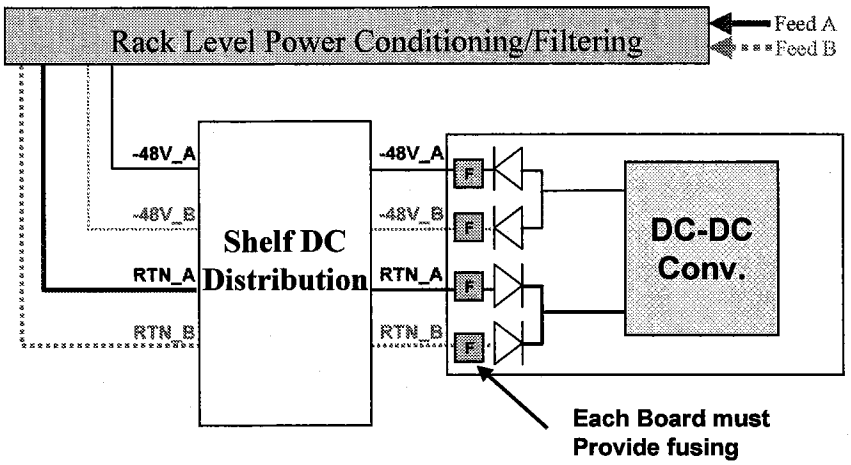
Shelf-level fusing can be used to protect the Shelf and Backplane in the event of an abnormal fault such as mis-wiring of Shelf power, conductive particulate contamination, or other events. It is not required to perform this function since some installations rely on Frame-level PDUs.

Board level fusing **shall** be provided on each -48 VDC Feed and its corresponding return as it enters the Board. Since there are dual Feeds, there **shall** be at least four fusing devices, and they **shall** be located between the individual Feeds as they enter the Board and any diode OR'ing or power conversion that might take place to combine the two Feeds into a single supply or return on the Board. For examples of this, see Figure 4-5, "Fusing example"; Figure 4-9, "Typical power distribution in a Shelf," and Figure 4-13, "Example of diagram with diode coupling of input power."

Boards **shall** keep the A and B Feeds isolated so that current cannot flow between -48V_A and -48V_B and so that current cannot flow between VRTN_A and VRTN_B. Diodes **may** be used for isolating the Feeds on Boards.

This fusing (see Figure 4-5, "Fusing example") is intended to protect the Shelf and Backplane from any damage if a Board develops a low impedance short. This fusing is also designed to minimize any disturbance the low impedance short might have on other operating Boards in the system, especially those adjacent to the failed Board. This fusing is not intended to protect the failed Board or any components or traces on it from damage. Additional protection for those purposes is optional.

Figure 4-5 Fusing example



Fusing for each Feed entering the Board **shall** be rated for less than 16.5 A at the Board's minimum operating voltage. Such fusing **should** be approximately 40-50% over the rated current load. For a 400 W double-wide Board, this results in a 15 A fuse rating, and, for a 200 W Board, this would be a 7 A fuse rating. Fusing for each return line **shall** be rated higher than the supply line fuse rating and **shall** be rated for 20 A or less.

The overcurrent mechanisms on PICMG® 3.0 Boards **shall** have I^2t ratings between 15 and 100 (such as a Littelfuse™ 325007 fuse) to provide sufficient protection and avoid nuisance blowing. Fuses **may** be either fast acting or slow blow style. Slow blow fuses will have a higher I^2t value and lower instances of nuisance blowing. Higher current Boards **may** use multiple overcurrent mechanisms on separate Feeds to power converters to meet this rating. The overcurrent mechanisms **shall** meet or comply with TNV-2 fusing requirements in sub-clause 2 of UL 60950, EN 60950, and IEC 60950.

The Backplane and Shelf **shall** provide the following without damage to the Backplane or Shelf:

- 20 A current flow to any Slot

- Low enough impedance to allow at least 220 A to flow in less than 4 ms in a short circuit condition to any single Slot
- 220 A current flow to any single Slot for 4 ms

The non-isolated power Feeds in the Board **shall** meet the following requirements without damage to the Board:

- Low enough impedance to allow at least 220 A to flow in less than 4 ms in a short circuit condition.
- 220 A current flow for 4 ms.

4.1.4.1 Inrush current limiting

Inrush current for a PICMG® 3.0 Shelf **shall not** exceed the following inrush current limits (see Table 4-2, "Ratio of inrush current limits"). Note that the values in Table 4-2, "Ratio of inrush current limits," are ratios, not absolute numbers. These are based on the ratio of instantaneous current value (I_t) versus the manufacturer's maximum rated continuous current draw (I_m).

Table 4-2 Ratio of inrush current limits

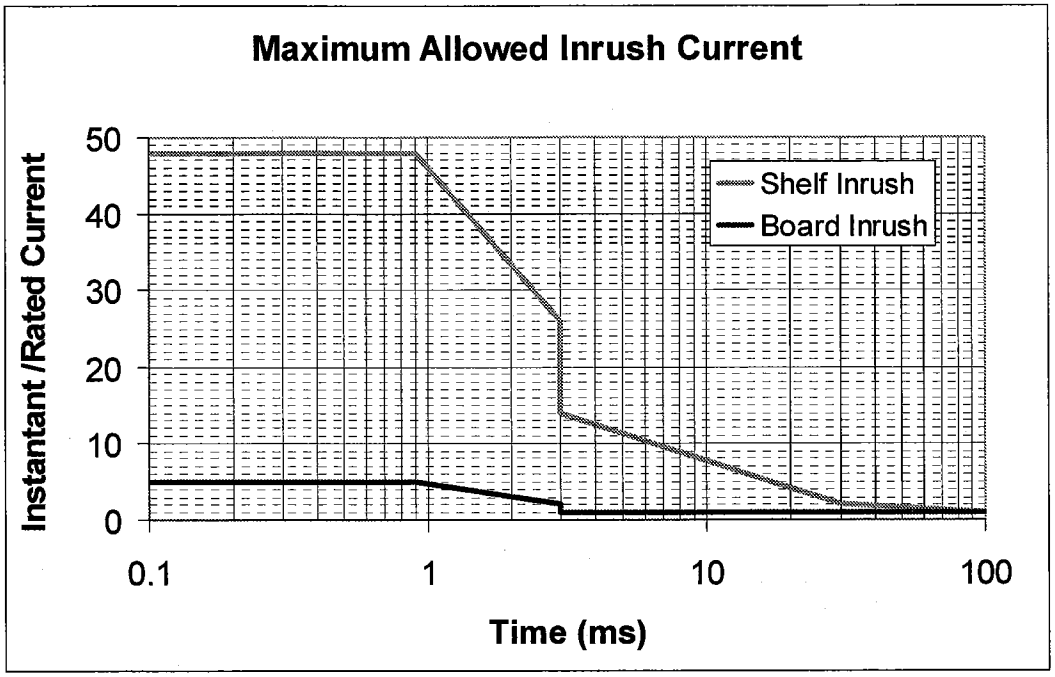
Time range	Shelf limits (I_t/I_m) at Interface A	Board limits (I_t/I_m)
0 to 0.9 ms	48	5
0.9 to 3 ms	Logarithmic decline from 48 to 26	Logarithmic decline from 5 to 2
3 to 30 ms	Logarithmic decline from 14 to 2	1 (I_m)
30 to 100 ms	Logarithmic decline from 2 to 1	1

The Shelf limits support compliance with Section 4.7 of ETS 300 132-2. The two sets of limits provide guidance for Board and Shelf designers. The limits in the Table 4-2, "Ratio of inrush current limits," are reflected in Figure 4-6, "Ratio of maximum allowed current surge."

Inrush current for PICMG® 3.0 Boards **shall not** exceed the inrush current limits shown in Table 4-2, "Ratio of inrush current limits." This requirement applies to the two main Feeds. The connectors **should** be fully mated when these surges occur.

The EARLY_A and EARLY_B contacts are provided so that Boards can charge the bulk capacitors through early power pins during the Board insertion process. These contacts are typically current limited with resistors. The EARLY_A and EARLY_B pins **shall not** draw more than 4 A at any time. After insertion, no more than 300 mA in total **shall** be drawn from the EARLY_A and EARLY_B contacts together.

Figure 4-6 Ratio of maximum allowed current surge



4.1.4.2 Battery Plant characterization for fusing (informative)

Figure 4-7, "Plant model for fault analysis," shows a simplified model of a Battery Plant and a PICMG® 3.0 system to show the effect of what happens when a short is created (modeled by using the switch S1).

Figure 4-7 Plant model for fault analysis

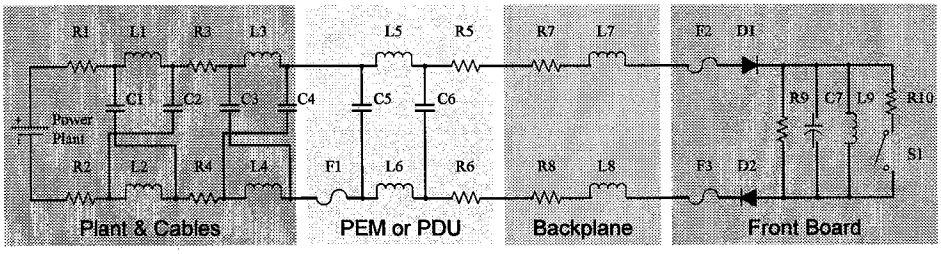
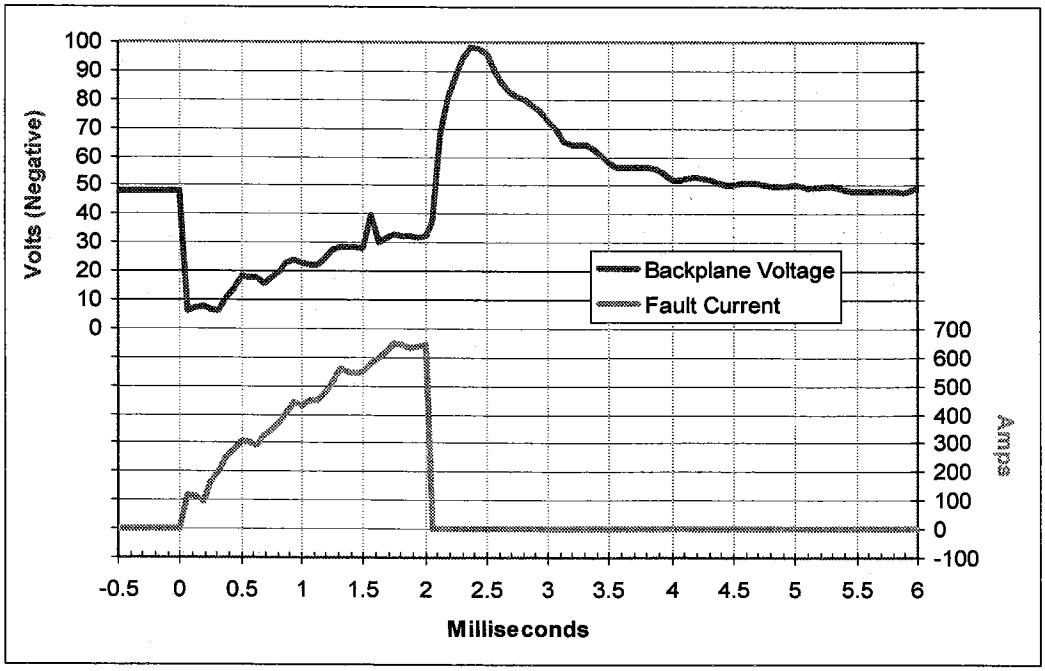


Table 4-3 Power distribution model for fault analysis—plant to Board

	Description	Value each
Plant	Battery Bank, insignificant source impedance	-44 to -72 VDC
R1, R2, R3, R4	Distribution cable resistance (2V drop total @ 3KW)	6.6 mΩ
L1, L2, L3, L4	Distribution cable inductance (1uH/m, 20m length)	5 µH
C1, C2, C3, C4	Cross-coupled capacitance (inc. cross-talk)	100pF
F1	PDU or PEM over-current protection (Fuse or CB)	1.9 mΩ
L5, L6	PDU or PEM filter elements	10-100 µH
C5, C6	PDU or PEM filter elements & compensation for L1, L2	10-100 µF
R5, R6	Total resistance per leg of PDU or PEM	<5 mΩ
R7, R8	Backplane trace and contact resistance	<5 mΩ
L7, L8	Backplane inductance	<10nH
F2, F3	Front Board fuses	15A @ I2t = 100
D1, D2	Front Board ORing diodes	10A Schottky
R9	Front Board load resistance	200W max
C7	Front Board capacitive load	3000 µF
L9	Power converter inductance	1 µHy
R10	Fault resistance	Overload range

When a short occurs on the Front Board, the fault current and input voltage are affected as shown in Figure 4-8, "Example fault transients."

Figure 4-8 Example fault transients



As is shown in Figure 4-8, "Example fault transients," the input voltage range will drop to neighboring Boards until the overcurrent device trips. This undervoltage condition is a subset of the transient conditions shown below. If fuses outside the limits in Section 4.1.4, "Fusing and fault protection," were used, the neighboring Boards would have a substantially longer period to operate through a short and a greater risk of losing power.

4.1.4.3 Transients

Shelves and Boards **shall** provide continuous operation in the presence of transients shown in the following table.

Table 4-4 Transient characteristics

Voltage	Duration	Comments	Protected by
± 200 Volts	5 µs	-100 to -200 Volts	Frame or Shelf
± 100 Volts	10 µs	-75 to -100 Volts	Board
± 75 Volts	10 ms	10 Volts per ms—Rise or Fall	Board
± 0 Volts	5 ms	50 Volts per ms—Fall 12.5 Volts per ms—Rise Assumes prior voltage is above -44 VDC for Shelves, -43 VDC for Boards.	Board

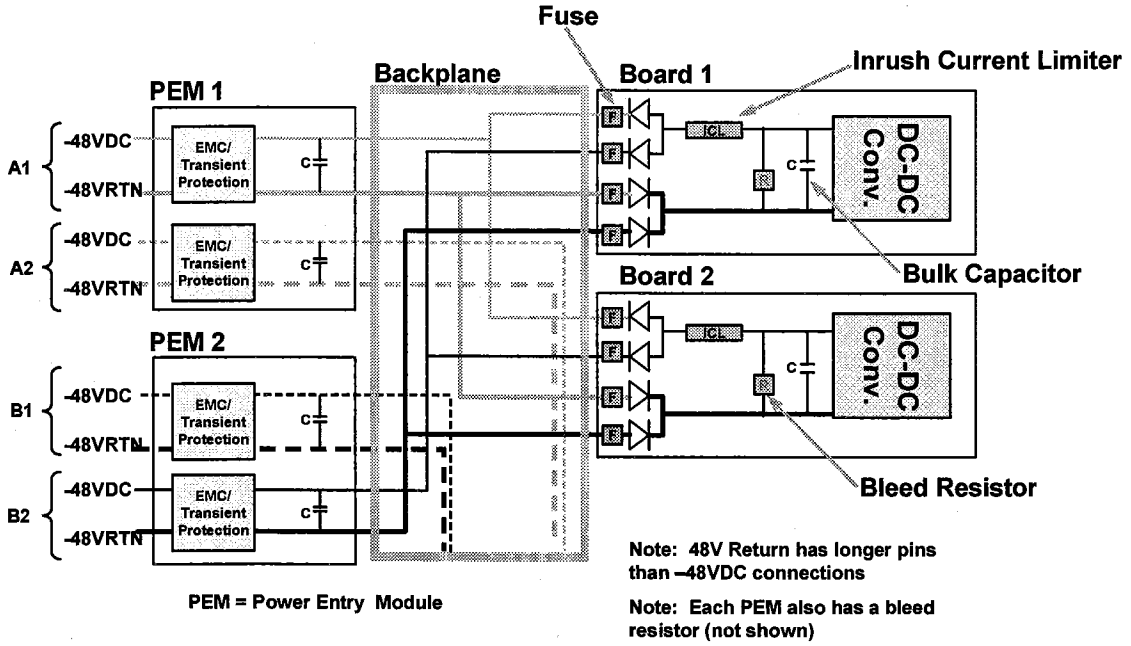
The transients in Table 4-4, "Transient characteristics," are taken from the AT&T NEDS requirements. Note that the 0 Volt transient can also occur during a short circuit, as indicated in Figure 4-8, "Example fault transients."

All other Shelf elements feeding off the -48 VDC power inputs **should** meet these same requirements.

4.1.4.4 Fusing and local energy storage

Figure 4-9, "Typical power distribution in a Shelf," shows a typical power distribution system for a PICMG® 3.0 Shelf (see Figure 4-13, "Example of diagram with diode coupling of input power," and Figure 4-14, "Example diagram without diode coupling of input power," for more examples).

Figure 4-9 Typical power distribution in a Shelf



Note: The bulk capacitor shown in Figure 4-9, "Typical power distribution in a Shelf," enables the Board to survive the 5 ms 0 Volt transient described in Figure 4.1.4.3, "Transients." The bulk capacitor also provides enough capacity to operate through a short on another Board. In Figure 4-9, "Typical power distribution in a Shelf," if Board 2 shorts power to ground, the voltage on both the A and B Feeds may dip momentarily until the fuse in Board 2 blows. Once the fuse on Board 2 blows, the power level will return to its normal levels and the capacitor will recharge. ***(End of Note)***

PICMG® 3.0 Boards **shall** provide a mechanism on-board (such as bulk capacitance) to provide at least 5 ms of power, at the maximum rated current load, to keep the Board operational. Such capacitance may be on either or both sides of the DC-DC converter or voltage regulator module. PICMG® 3.0 Boards **shall** provide a discharge mechanism (such as a bleed resistor) to discharge the capacitance mechanism to less than -60 VDC and less than 20 joules within one second of disconnection from the Backplane to protect service personnel from possible shock.

Traces between the Zone 1 power connector and fusing devices **should** be located to minimize the distance to reduce the risk of catastrophic failure in the event of a short circuit in this area. The fuse and any leads **should** be covered to minimize the chance of incidental contact (i.e., dropped screwdriver or paper clip) causing a short prior to where the on-board fuse limits the current for the Board. This protects the Backplane.

The current flowing through Enable A and Enable B **shall** be limited to less than 100 milliamps. This current limiting device **should** occur in the protected, covered area described above.

4.1.5 Filtering

PICMG® 3.0 specifies a standard set of Board and Shelf level requirements to allow inter-operability while maintaining appropriate agency conducted and radiated emissions requirements. Since -48 VDC is distributed to all active components of the Shelf, the primary noise source in the Shelf is typically the DC-DC converters that convert -48 VDC to the various regulated voltage rails required by the Board or FRU.

4.1.5.1 Board conducted emissions

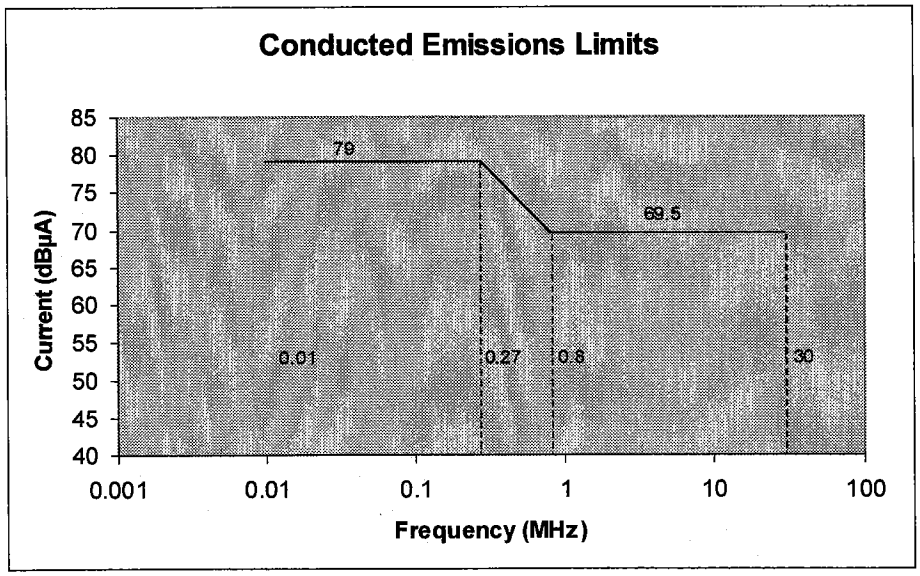
The main filtering function is performed in the Board. The Board **shall** ensure that the conducted emissions remain below the levels of CISPR 22 Class B.

4.1.5.2 Shelf Conducted emissions

As more Boards are added and since the noise sources are asynchronous, the source impedance of the additional Board appears as another load to the first Board. The common mode model demonstrates a similar situation. If we assume that the Board impedance is defined and that all the Boards have a relatively high impedance compared to the load impedance, then the addition of similar Boards causes a power increase of 10 LogN (N= number of Boards added) to be seen at the input of the system power filter. For a Shelf that can accommodate 14 Boards, that amounts to 11.5 dB greater conducted noise into the system power filter than the noise resulting from a single Board; for a 16-Board Shelf, this results in 12.04 dB greater conducted noise.

The specification mandates that the main emissions filtering function is performed in the Board. The Shelf will aggregate the conducted emissions from up to 16 Boards. This requires a minimum attenuation of 11.5 dB. To provide a good margin, the Shelf **shall** provide an attenuation of 18 dB between 150 kHz and 30 MHz. The Shelf **should** provide a minimum of 18 dB of attenuation in the frequency range of 30 MHz to 1.0 GHz as shown in Figure 4-10, "Conducted emissions limits." This will bring the aggregate level of the Shelf-conducted emissions to below the required levels.

Figure 4-10 Conducted emissions limits



Note: The system designer should note that the filter must match the input supply and Backplane power impedances. Power cabling can have a wide rage of values between 20 Ohms and 120 Ohms. A Backplane power impedance can be between 0.1 Ohms to 5 Ohms. A Board power impedance can range between 1 and 40 Ohms.

Note: The system designer should note the contribution caused by longitudinal conversion losses of differential noise (not covered by CISPR 22) to the common mode noise levels. At the proposed power levels of a typical system, the differential noise contribution could cause certification failures.

4.1.5.2.1 Shelf filter testing

It is not feasible to define a test method for a Shelf in Isolation. However, the test method of IEC 61000-4-6 can be applied to a populated Shelf with active Boards to the limits of CISPR 22.

4.1.5.3 Radiated emissions

Radiated emissions are difficult to specify and test without a full system. Boards are the primary source of radiation, and it is the responsibility of the Board designer to reduce emissions. The enclosure designer is responsible for ensuring a reasonably closed EMC shield, but it is up to the system designer/integrator to test the system against the required standards.

4.1.5.3.1 Board radiated emissions

Board radiated emissions can be minimized by good layout and decoupling techniques. To assist in meeting the radiation requirement, the Board **should** have a metal plate connected to Shelf Ground on Component Side 2 of the PCB.

4.1.5.3.2 Shelf radiated emissions

The Shelf **shall** use best engineering practices to contain radiated emissions below the levels of CISPR 22 Class B as part of the Shelf subsystem. Attention **shall** be given to the integrity of the Front Board and RTM Face Plates and the sealing on cooling and other apertures.

4.1.6 Board power sequencing

4.1.6.1 Introduction

Power sequencing in the Board takes place at two levels: the hardware level and the hardware management level. The hardware power sequencing, which follows, ensures a safe insertion and withdrawal of a Board. The hardware management system then takes over to ensure that the Board is powered up in a manageable configuration.

For an example of a power subsystem, see Section 4.3, "Board-level power conversion."

4.1.6.2 Power and ground sequencing

During a Board insertion, the ESD segment #1 and the Guide Rail provide the first electric contact between the Board and the Shelf. This contact provides a discharge path to the Shelf Ground, as described in Section 2.2.5, "ESD discharge strip." The second ESD segment discharges Logic Ground.

Power sequencing is provided by pins of different lengths in the power connector and the Subrack (see Appendix B, "Power connector," for more information). The mating sequence is shown in Table 4-5, "Mating sequence for insertion of Boards."

Table 4-5 Mating sequence for insertion of Boards

Stage	Element	Engagement to nominally seated Board
1	ESD Strip #1	
2	ESD Strip #2	
3	ESD Strip #3	
4	Zone 3 Alignment/Keying Pin	~ 25 mm
5	Zone 3 Connectors	~ 23 mm (maximum)
6	Zone 2 Alignment/Keying Pin	~ 18 mm
7	Front Face Plate Alignment/Ground Pin	~ 15 mm
8	SHELF_GND, LOGIC_GND, VRTN_A, VRTN_B, EARLY_A, and EARLY_B in Zone 1	9.54 mm
9	-48 V_A	6.54 mm
10a	-48 V_B	4.04 mm
10b	Zone 1 Management/Address/Ring Voltage Pins	3.74 mm
10c	Zone 2 Ground Shields	3.62 mm
11	Zone 2 Signal Pins	2.25 mm
12	ENABLE_A, ENABLE_B in Zone 1	1.44 mm

The first pins to mate in the power connector are the logic and Frame/Shelf Grounds and the EARLY_A; EARLY_B; VRTN_A; and VRTN_B pins. The EARLY_A and EARLY_B pins allow for the pre-charge of the power converter input capacitance. At a 0.5 meters per second insertion rate, this provides a 3 millisecond time period between the early power contact and the ENABLE_A contact. Operational power for a Board **shall** be drawn through -48V_A and -48V_B. Board designers **may** use the EARLY_A and EARLY_B pins for pre-charge or may leave the pins disconnected.

The Board designer must ensure that the inrush current is within limits described in Section 4.1.4.1, "Inrush current limiting."

The -48V_A and -48V_B pins are the main power Feeds to the Board. They are staged differently so that the supply planes A and B are not disturbed at the same time. The ring/test, management, addressing, and Zone 2 pins connect next.

The last pins to engage in the power sequence are the enable pins ENABLE_A and ENABLE_B. Backplanes **shall** connect EARLY_A to -48V_A; EARLY_B to -48V_B; ENABLE_A to VRTN_A; and ENABLE_B to VRTN_B.

Figure 4-11 Board insertion sequence diagram

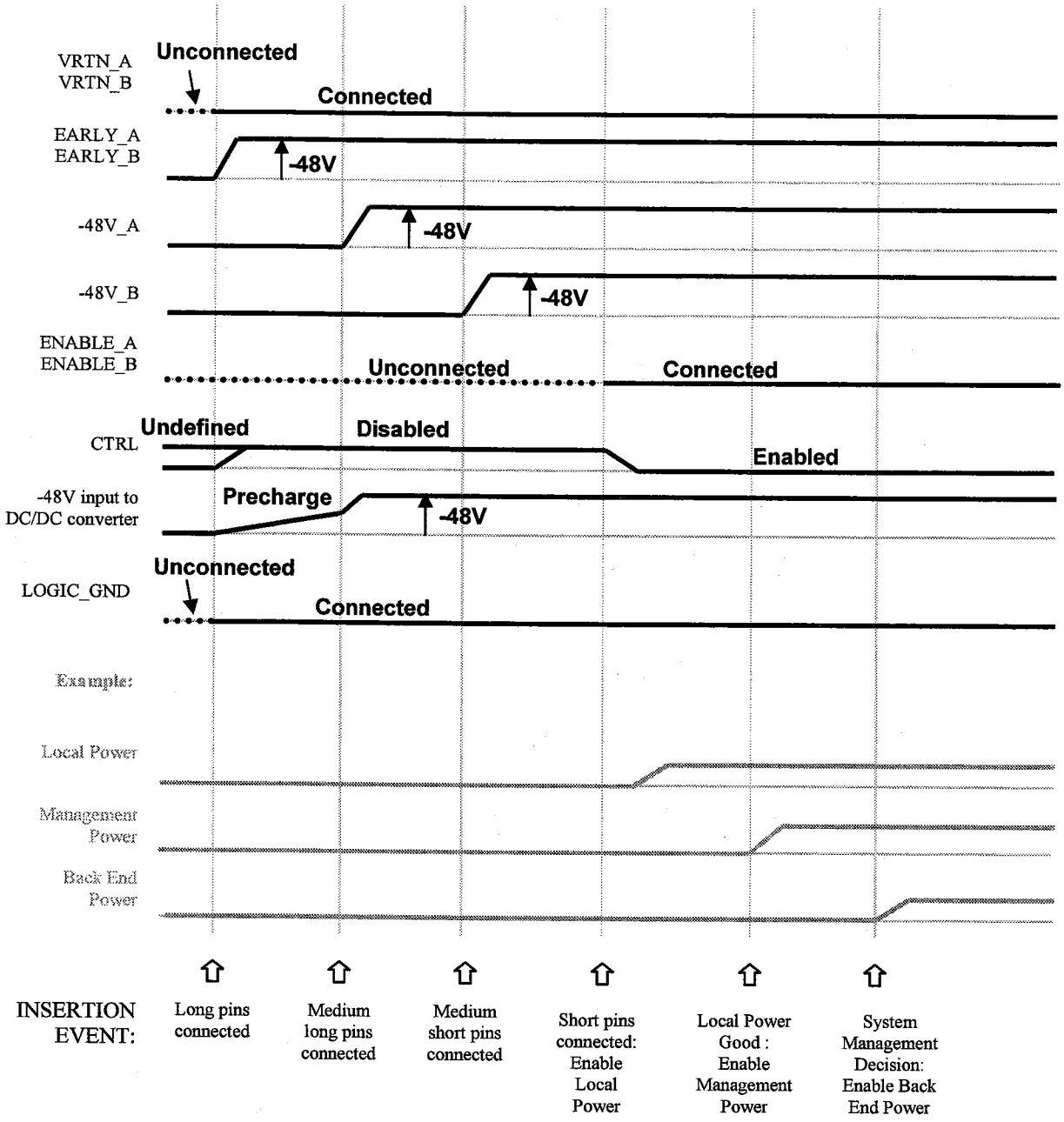
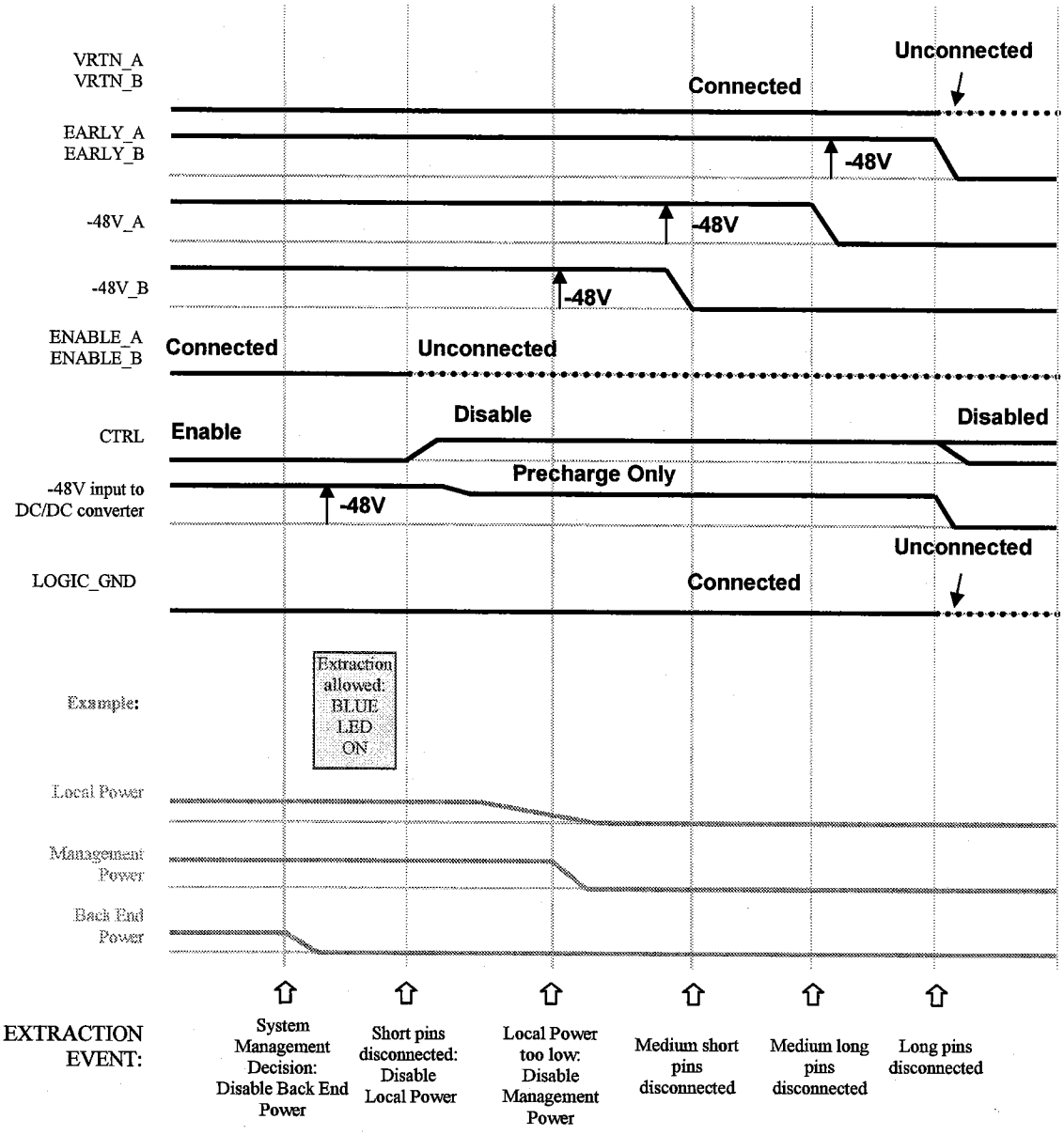


Figure 4-12 Board extraction sequence diagram



4.1.6.3 Management power

Boards in the Subrack **shall not** consume more than 10 W total power (including consumption at the on-board power converters) from all power sources until they have negotiated power-up rights with the Shelf Manager. This includes powering the IPM Controller and idle power consumed in the power converters.

As noted in Section 4.1.2, "Supported voltage levels," the management subsystem **may** be powered at voltage levels below the minimum Payload voltage level.

However, if the input voltage drops below the cutoff voltage threshold as specified in Section 4.1.2, "Supported voltage levels," the management power **may** not be provided.

4.1.6.4 Payload power

As noted in Section 3.9, "Shelf power and cooling," FRUs must not turn on Payload power until they have negotiated with the Shelf Manager to do so. Each FRU **shall** have an IPM Controller responsible for controlling FRU power above the management/idle power as specified in Section 4.1.6.3, "Management power."

4.2 Grounding strategy

4.2.1 Shelf Ground

All front Panels (including those for Front Boards, RTMs, and Shelf elements such as fan trays) **shall** be connected to Shelf Ground. Each FRU **should** be connected to Shelf Ground through both a reliable Face Plate connection and through a Backplane connector.

Each Shelf **shall** provide at least one dual-pole grounding lug for Shelf Ground.

4.2.2 Shelf Ground and –48 VDC return

Both Mesh and SPR (single-point return) grounding strategies are in common use. In SPR environments, the Shelf (safety) ground wiring is kept separate from the –48VRTN lines all the way to the Battery Plant, where they are eventually tied together. In a meshed ground environment, the safety grounds and return lines are tied together at equalization plates throughout the facility. In meshed grounding environments, the same cabling is often used for both Shelf Ground and –48VRTN; this is commonly called a "2-wire" system (-48VDC, -48VRTN/SHELFGND). In SPR environments, Shelf Ground must be maintained separately; this is commonly called a "3-wire" system (-48VDC, -48VRTN, SHELFGND). Three-wire systems are the most restrictive from a design perspective.

PICMG® 3.0 Shelves **shall** isolate the -48 VDC return lines from Shelf Ground. However, Shelves **shall** provide a mechanism at the Shelf level to provide the installer the option to tie the Shelf Ground and -48 VDC return lines A and B together.

4.2.3 Shelf Ground and Logic Ground

Requirements regarding Logic Ground and Shelf Ground isolation vary in different telecom applications.

A Front Board and RTM **shall** have a DC resistance of greater than 9 MOhms between Logic and Shelf Grounds as measured with a 100 V test voltage.

A Shelf **shall** provide a mechanism to interconnect Logic Ground and Shelf Ground. Each Front Board, RTM, or FRU **should** provide a mechanism for an installer-configurable, low-impedance connection between Logic Ground and Shelf Ground in the vicinity of the Face Plate. The impedance value is application specific.

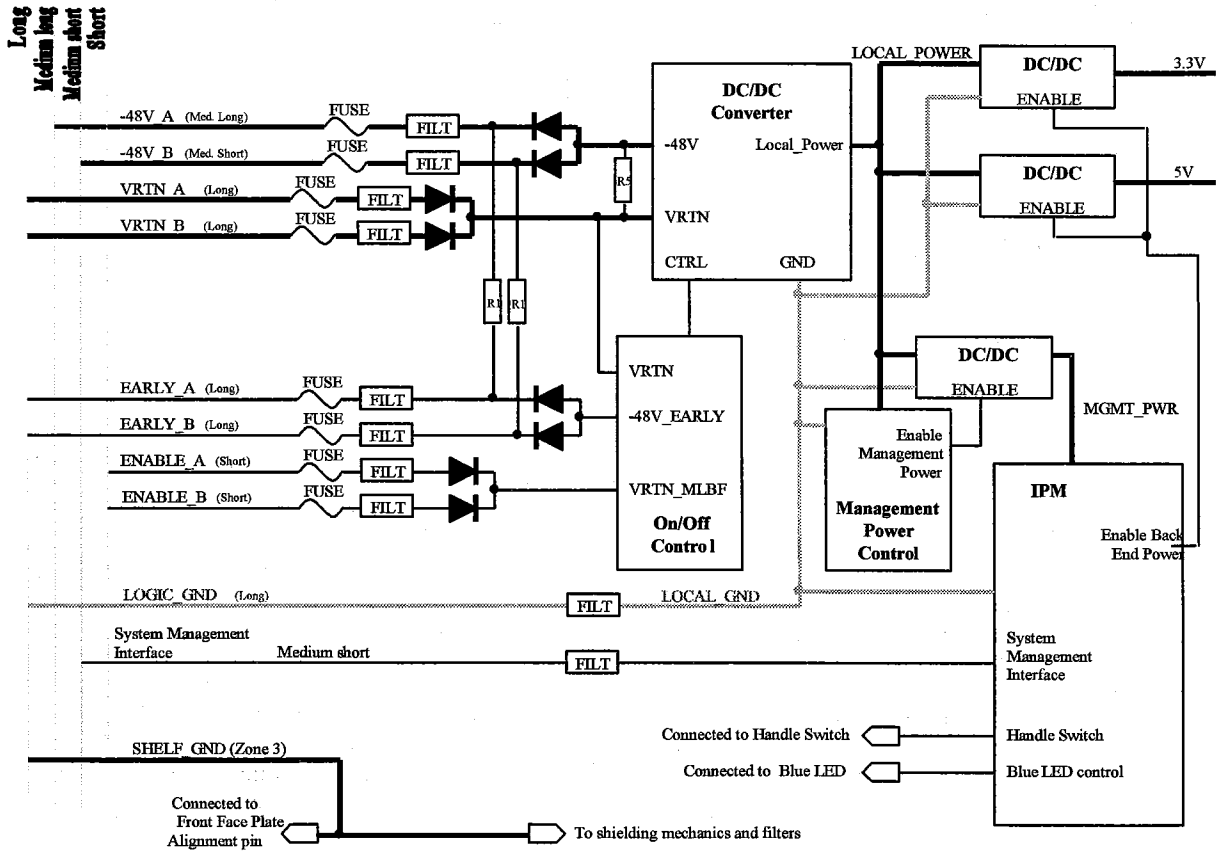
4.3 Board-level power conversion

4.3.1 Conversion architectures

Each -48 VDC Feed remains isolated and is fed individually to each Board Slot through the Backplane. There are two basic methods for combining the dual redundant Feeds.

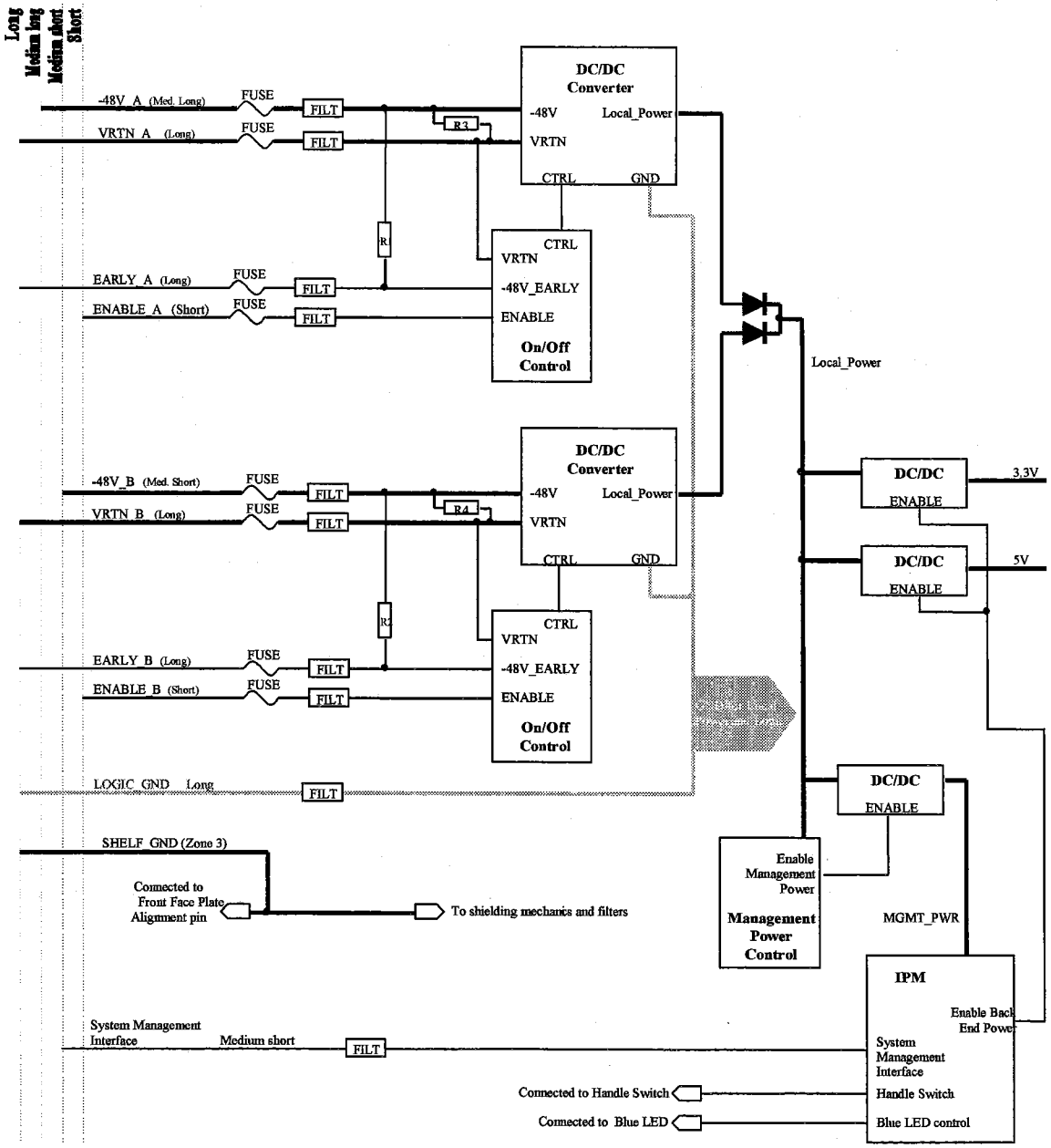
One method, shown in Figure 4-13, "Example of diagram with diode coupling of input power," combines the two Feeds through diode OR'ing and delivers the combined single Feed to on-FRU DC/DC converter(s). If either Feed fails, all power **shall** be delivered by the surviving Feed.

Figure 4-13 Example of diagram with diode coupling of input power



The second method, shown in Figure 4-14, "Example diagram without diode coupling of input power," is to direct each of the two Feeds to its own DC/DC converter. The outputs of the converters are then combined to provide power to the on-FRU circuits.

Figure 4-14 Example diagram without diode coupling of input power



4.3.2 DC to DC converter requirements

The input voltage requirements for DC to DC converters on Boards are found in Section 4.1.2.2, "Voltage level requirements." Inrush current limits are found in Section 4.1.4.1, "Inrush current limiting."

The DC to DC converter **shall** withstand a DC offset of up to 600 V from Logic and Shelf Grounds on the following pins: -48V_A; -48V_B; EARLY_A; EARLY_B; VRTN_A; and VRTN_B.

4.3.2.1 Power supply noise voltages

Section 4.1.4.2, "Battery Plant characterization for fusing (informative)," requires conformance with the conducted emissions requirement of IEC 61000-4-6. These currents will give rise to an AC noise voltage (hash or ripple) on the DC supply.

The impedance between the power input to the Shelf and the J10 connector for any Slot **shall** be less than 10 Ohms from 10 kHz to 30 MHz.

Note: In practice, power plane (or shape) impedance can be maintained to less than two Ohms. From the above, the expected noise will be less than 1427 mV from 10 kHz to 270 kHz; less than 384 mV - $20\log_{10}f$ from 270 kHz to 800 kHz; and less than 480 mV from 800 kHz to 30 MHz.