LINE INPUT AC TO DC CONVERSION AND INPUT FILTER CAPACITOR SELECTION

The input rectifier/filter section of an off-line power supply converts the 50-60Hz AC line voltage to a DC voltage, Vin, which powers the downstream high frequency switching section. A circuit diagram typical of a dual range input rectifier/filter section is shown in Figure 1. For 230 volt line operation, the input rectifiers are configured as a full-wave bridge. For 117 volt operation, the input circuit is reconfigured as a voltage doubler, so that Vin will be approximately the same as under 230 volt operation. While it is technically possible to operate the input section as a bridge at both 230V and 117V, the switching regulator would have to be designed to operate over a much larger Vin range which would significantly increase its cost.

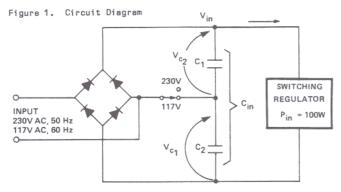


TABLE I - 100 WATT INPUT RECTIFIER/FILTER SECTION

		117V	117V	230V	
		BRIDGE	DOUBLER	BRIDGE	
		(60Hz)	(60Hz)	(50Hz)	
RMS Line Voltage	Vac	99-135	99-135	195-265	v
Peak Line Voltage	Vok	140-191	280-382	276-375	V
Max Ripple Voltage	٧r	40	80	76	V
DC Input Voltage	Vin	100-191	200-382	200-375	V
Input Capacitance	*Cin	203	80	61	μF
Doubler Capacitance	*C1,C2	_	160	(122)	μF
Charging Time	tc	1.954	2.275	2.345	ms
Peak Charge Current	*ichg	3.64	3.28	1.82	A
RMS AC Chrg Current	*Ichg	1.54	1.126	.771	A

* For power levels other than 100 watts, multiply capacitance and current values by $P_{in}/100$ [$P_{in} = P_0/L$].

Input filter capacitance C_{in} determines V_{r} , the $100/120\,Hz$ peak to peak ripple voltage component of V_{in} (see Figure 2). At low line voltage, V_{r} determines the minimum input voltage, V_{min} , which is an important consideration in the design of the switching supply. V_{min} defines the transformer turns ratio required to achieve the specified output voltage at maximum duty cycle.

If the input filter capacitance is too small, the resulting large ripple voltage will require increased duty cycle range and control loop gain to maintain the specified output voltage. Vmin will be less, resulting in poor transformer utilization, higher peak current through the switching transistors, and higher peak inverse voltage across the output rectifiers.

Input filter capacitance larger than necessary will not only cost more, the recharging current pulses drawn from the line will be narrower and larger in amplitude (Figure 2). This hurts the line power factor and increases EMI. The higher RMS input current causes increased losses in the line, input rectifiers and filter capacitors, and can impair reliability.

A reasonable rule of thumb is to compromise on a ripple voltage 25-30% of the minimum peak line voltage, resulting in acceptable capacitor size, weight and cost. Table I shows the resulting values for 117V bridge operation with V_{\min} of 100V, and 117V doubler and 230V bridge operation with V_{\min} of 200V, for a switching supply with 100 watt power input. The input filter capacitors are designed to supply the full load energy of the supply and hold V_{in} above the desired V_{\min} between AC line peaks. With the switched dual range input section (117V doubler or 230V bridge) filter capacitor requirements are determined by the voltage doubler configuration.

DESIGN EQUATIONS AND CALCULATIONS:

The following examples are given for full-wave bridge operation from the 230 volt line (195-265V), and full-wave bridge and voltage doubler operation from the 117 volt line (99-135V).

Since virtually all the losses in the switching power supply are downstream of the input rectifer/filter, the input section must handle the entire power input, $P_{\rm in}$ (equal to full load power output divided by efficiency). Power input in these examples is assumed to be 100 wetts at full load. The resulting capacitance and current values can be adjusted for any other power input by multiplying by the actual $P_{\rm in}/100$.

Between line peaks, the input filter capacitor must supply the entire full load energy requirement of the supply. Ripple voltage $V_{\rm T}$ must be small enough to maintain $V_{\rm IR}$ greater than the desired $V_{\rm min}$ under worst case conditions of low line frequency, low line voltage and full load. Energy required at 100 watts for

one entire line cycle at 50Hz (worst case used with 230V line):

$$W_{in} = \frac{P_{in}}{f} = \frac{100}{50} = 2.0 \text{ Joules (Watt-seconds)}$$
 [1]

At <u>60Hz</u>, the energy required for one line cycle at 100 watts is reduced to 1.667 <u>Joules</u>.

FULL WAVE BRIDGE OPERATION

Referring to Figures 1 and 2, input filter capacitor Cin [C1 in series with C2] charges to peak line voltage each helf cycle. Cin then discharges, providing all the energy required by the switching supply until it is recharged at the next helf cycle. Energy from Cin each half line cycle is:

$$W_{in}/2 = \frac{1}{2} C_{in} (V_{pk^2} - V_{min^2})$$

$$C_{in} = \frac{W_{in}}{V_{pk^2} - V_{min^2}} \qquad (2)$$

Figure 2. Bridge Waveforms

As shown in Figure 2, the recharging time, t_{C} , is established by the intercept of the capacitor voltage waveform with the rectified AC line:

$$V_{min} = V_{pk} \cos(2\pi f t_c)$$

$$t_c = \frac{\cos^{-1}(V_{\min}/V_{Dk})}{2\pi f}$$
 [3]

CAPACITOR

Assuming a rectangular charging current pulse of peak amplitude icha (constant current during the charging interval):

$$\Delta Q = i_{chg} \Delta t = C \Delta V$$

$$i_{chg} = C (V_{pk} - V_{min})/t_c$$
 (4)

The RMS AC component of the charging current, I_{chg} , is conducted through the filter capacitors and contributes to capacitor heating due to their equivalent series resistance (ESR). The DC component of the total RMS charging current does not pass through the capacitor and does not contribute to capacitor heating.

$$I_{chg} = \sqrt{ICHG^2 - IDC^2} = \sqrt{ichg^2 tc 2/T - ichg^2 (tc 2/T)^2}$$

$$I_{chg} = ichg \sqrt{tc 2f - (tc 2f)^2}$$
[5]

The switching supply discharges the input capacitors by drawing high frequency pulses of current. The AC component of the RMS

discharge current, Idis, also causes filter capacitor heating. The filter capacitors must be selected to have RMS current ratings greater than the total RMS AC current components. This is an important consideration for capacitor reliability.

Total ICAP =
$$\sqrt{I_{chg}^2 + I_{dig}^2}$$
 [6]

The DC component of the high frequency discharge current pulses equals the DC component of the charging current from the line. Because the form factor of the high frequency discharge current at low line is much better (closer to 1.0) than the charging current waveform, the RMS AC discharge current, Idis, is much less than I_{chg} , depending somewhat on the switching circuit topology.

For 230V (50Hz) bridge operation: At 195V minimum line voltage, the minimum peak voltage, Vpk, is 276V. Conservatively assume 270V peak, allowing for drops in rectifiers and line. From Equation (2):

$$C_{in} = \frac{2}{270^2 - 200^2} = 61 \mu F$$

Charging pulse width from Equation (3):

$$t_c = \frac{\cos^{-1}(200/270)}{2\pi \cdot 50} = 2.345 \text{ ms}$$

Peak charging current from Equation (4):

$$i_{\text{chg}} = 61(270-200)/2.345 \times 10^{-3} = 1.82 \text{ A}$$

RMS charging current from Equation (5):

$$t_0.2f = 2.345x10^{-3} 2.50 = .2345$$

$$I_{chg} = 1.82 - \sqrt{.2345 - .2345^2} = .771 A$$

For 117V (60Hz) bridge operation (normally used only for single range 117V input): At 99 volts minimum line, minimum Vpk is 140V. Conservatively assume 135V peak, allowing for drops in rectifiers and line:

$$C_{\text{in}} = \frac{1.667}{135^2 - 100^2} = 203 \ \mu\text{F}$$

$$t_{\text{c}} = \frac{\cos^{-1}(100/135)}{2\pi \ 60} = 1.954 \ \text{ms}$$

$$i_{\text{chg}} = 203(135-100)/1.95 \ \text{x} \ 10^{-2} = 3.64 \ \text{A}$$

$$t_{\text{c}} \ 2f = 1.954 \text{x} 10^{-2} \ 2 \ 60 = .2345$$

$$I_{\text{chg}} = 3.64 \sqrt{.2345 - .2345^2} = 1.54 \ \text{A}$$

Referring to Figures 1 and 3, at minimum line voltage (99V), the peak voltage is 140V. Conservatively assume 135V peak, allowing for drops in rectifiers and line.

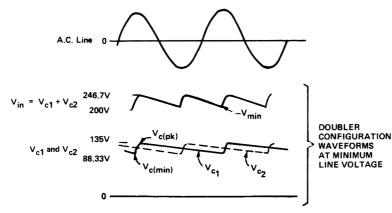


Figure 3. Voltage Doubler Waveforms

C1 and C2 alternately charge to peak line voltage. Note that whenever the input voltage, V_{in} , is at instantaneous minimum, one capacitor is at its minimum, but the other capacitor is half way between peak and minimum voltage. The minimum voltage on each capacitor corresponding to an overall V_{min} of 200V can be approximated as follows:

$$V_{\min} = V_{\text{Clmin}} + V_{\text{C2avg}} = V_{\text{Cmin}} + \frac{V_{\text{Cmin}} + V_{\text{Cpk}}}{2}$$

$$V_{\text{Cmin}} = \frac{2V_{\min} - V_{\text{Cpk}}}{3} = \frac{2(200) - 135}{3} = 88.33 \text{ V}$$
 (7)

C1 and C2 each discharge for a complete cycle. Each capacitor must supply half the energy required by the switching regulator for an entire line cycle:

$$W/2 = \frac{1}{2}C_1(V_{Cpk^2} - V_{Cmin^2})$$

$$C1 = C2 = \frac{W}{V_{Cpk^2} - V_{Cpin^2}} = \frac{1.667}{135^3 - 88.33^2} = 160 \ \mu\text{F}$$

 C_{in} , the series combination of C_1 and C_2 , equals $80~\mu F$

Note that the voltage doubler operated from the 117V line requires larger C_{in} than the 230V bridge input, so that for supplies with duel range 117/230 volt input, the 117V doubler

operation dictates the filter capacitor requirements.

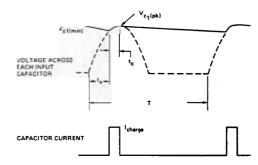


Figure 4. Voltage Doubler Charging Current

Figure 4 shows the waveforms associated with charging each of the input capacitors in the voltage doubler configuration at full load and minimum line voltage. Recharge time, tc, is established by the intercept of the capacitor voltage waveform with the rectified AC line:

 $V_{Clmin} = V_{Clnk} \cos(2\pi f t_c)$

$$t_{c} = \frac{\cos^{-1}(VC1min/VC1pk)}{2\pi f}$$

$$t_{c} = \frac{\cos^{-1}(88.3/135)}{2\pi f} = 2.275 \text{ ms}$$

Assuming a rectangular charging current pulse of peak amplitude ichg (constant current during the charging interval):

$$\Delta Q = i_{chg} \Delta t = C \Delta V$$

$$i_{chg} = C (V_{pk} - V_{min})/t_{c}$$

$$i_{chg} = 160(135-88.3)/2.275 \times 10^{-3} = 3.28 \text{ A}$$

The RMS current in each capacitor is:

$$I_{chg} = i_{chg} - \sqrt{t_c f} - t_c f^2$$

$$t_{cf} = 2.275 \times 10^{-3} 60 = .1365$$

$$I_{chg} = 3.28 - \sqrt{.1365} - .1365^2 = 1.126 A$$