APPLICATION INFORMATION

Predictive Timing Operation

The essence of SP6003A, the predictive timing circuitry, is based on several U.S. patented technologies. This assures higher rectification efficiency by a) eliminating high cross conduction current under all operating conditions and b) significantly reducing the body diode conduction losses in the synchronous rectifier.

V_{DD} Decoupling Capacitor

The IC is sensitive to large supply voltage ripple. If the IC drives a MOSFET with significant input capacitance, Ciss, the ripple due to gate drive energy transfer can create large ripple. Therefore, it is most suitable to add a high frequency decoupling ceramic capacitor of 0.01μF~0.1μF between Vdd to ground, and the capacitor should be placed as close proximity to the driver as possible.

Ramp Capacitor Selection (Cramp)

The ramp capacitor selection is frequency dependent. The capacitance selection should be made in according to the plot below:

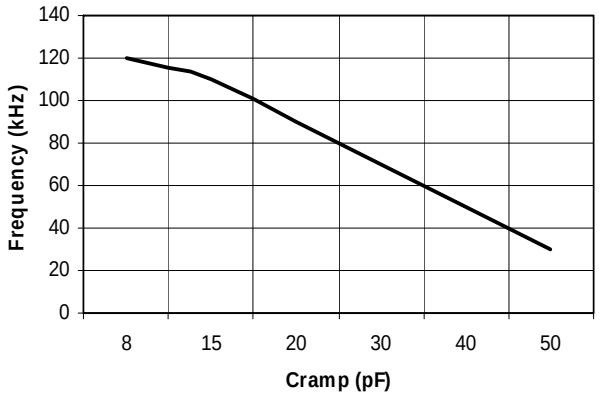


Fig. 1

The ramp capacitor selection is dependant on the range of the On and OFF times of the synchronous rectifier. In most application it is necessary to work to a narrow duty cycle. The ramp capacitor voltage charges from about 0.7 volts during the ON time. The charging current is 80 μA. For proper operation of the internal timing it is necessary to limit the ramp amplitude to 3.8 volts. This voltage limits and the maximum ramp ON time sets the minimum size capacitor needed. Since it is usually desirable to achieve proper operation down to essentially zero duty cycle, the capacitor minimum size can be represented as a function of frequency.

$C_{min} = I_{charge} * dT/dV = I_{charge}/F/dV;$

Since $I_{charge} = 80\mu A$ & dV=3.8V-0.7V,

$C_{min}=2.66*10^{-5}/F$

A capacitor size should be selected to meet the above criteria including the frequency tolerance and the capacitor tolerance over temperature. The criterion for the maximum suitable capacitance is less precise because it is driven by noise constraints. If a larger capacitor is chosen, the ramp voltage becomes lower and there is more jitter on the pulse width due to noise. It is usually advantageous to operate with as high a ramp voltage as possible for this reason. The minimum ramp amplitude occurs at the maximum converter operating duty cycle because this is when the MOSFET is conducting for the shortest period of time. For converters that need to be able to operate to a wider duty cycle, the capacitance should be close to the minimum calculated above to prevent noise problems.

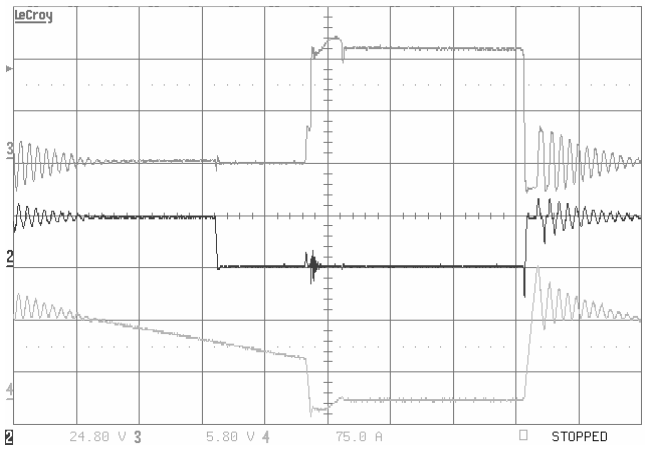


Fig. 2

Figure 2 illustrates the characteristic waveforms of a flyback converter with input voltage of 110VAC.

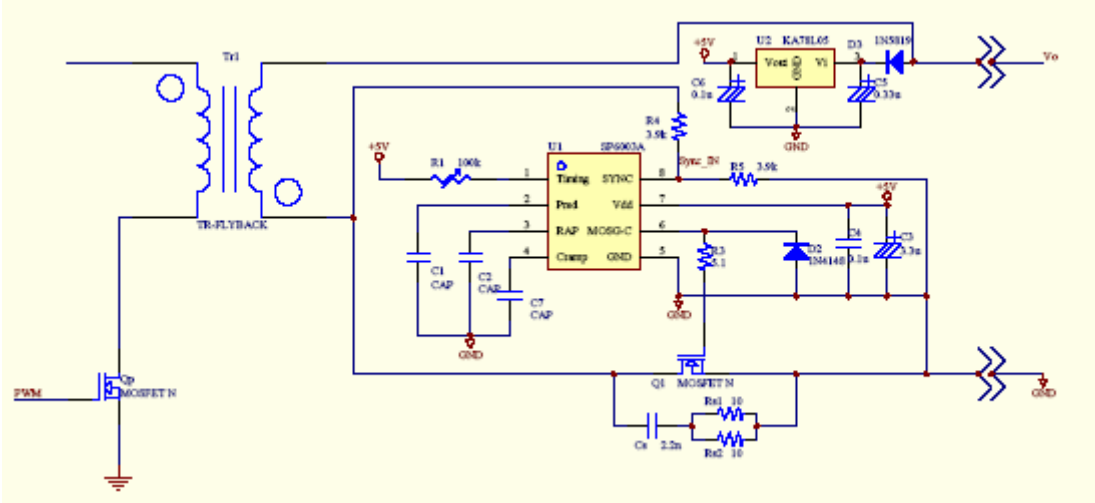


Fig. 3: Application Schematic

Channel 3 (2µs/DIV & 2V/DIV) indicates the SYNC voltage on the secondary side of a flyback transformer at 77 kHz, channel 2 (2µs/DIV & 5V/DIV) is the SP6003A output pin, MOSG-C, connects to the gate of MOSFET, and channel 4 (2µs/DIV & 10A/DIV) designates the input current (I_D). Notice the timing gap between the falling edge of MOSG-C and the rising edge of SYNC is 3.5µs with no ramp capacitor connected. Figure 3 is the equivalent circuit for this particular application.

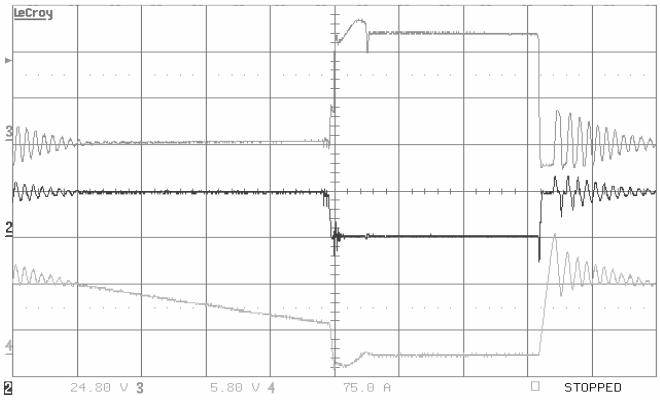


Fig. 4

With 33pF added to C_{ramp} pin with respect to ground, the timing gap immediately shortens and the ON time of the gate increased from 8.2µs to 11.6µs, as shown in figure 4. Thus, the efficiency is improved by approximately 0.655%. The output for this converter is set at 5V/8A.

For typical flyback application with 50 kHz to 120 kHz operations, a ramp capacitor value of 10 pF to 47pF is recommended. This allows the gate ON time to reach 10-12 microseconds for narrow pulse widths.

Timing Adjustment

The Timing pin provides adjustment of the patented dv/dt filter circuit that differentiates between the real power and ring-back no-power transformer secondary voltage positive waveform. Under light or no load conditions, the output current will be discontinuous. For that condition the transformer voltage "rings" back positive. The SP6003A detects positive transformer secondary voltage to establish power transmission, and determines the SR MOSFET turn ON time. However, it is not desirable to turn on the MOSFET during the "ring-back". The dv/dt filter detects the true power pulse from the "ring-back".

- Connect resistor to V_{DD}.

The first option is the nominal setting. For this condition, the Timing pin is left open or no connection. In result, the ON time of MOSG-C should be turned ON at every cycle. If not, the timing needs to be adjusted. Figure 5 illustrates an example of several ON time cycles missing:

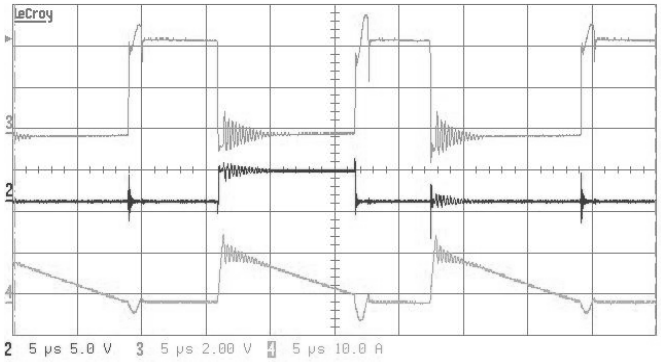


Fig. 5

The Timing adjustment should be performed under light load circumstance. A variable resistor, 0~100KΩ, is connected from Timing pin to VDD and adjust the variable resistor until the waveform at MOSG-C pin appears in every cycle. If this is unable to achieve, connect the variable resistor to ground and follow the same procedures. But be careful, once the correct resistor value is exceeded, more ON time cycles will appear during oscillation. It is best to eliminate these.

Once the variable resistor is adjusted to the correct value, the output waveform of pin MOSG-C should be ON at every cycle as shown in Figure 6. Then measure the resistance of the variable resistor. The typical value is between 8KΩ to 20KΩ.

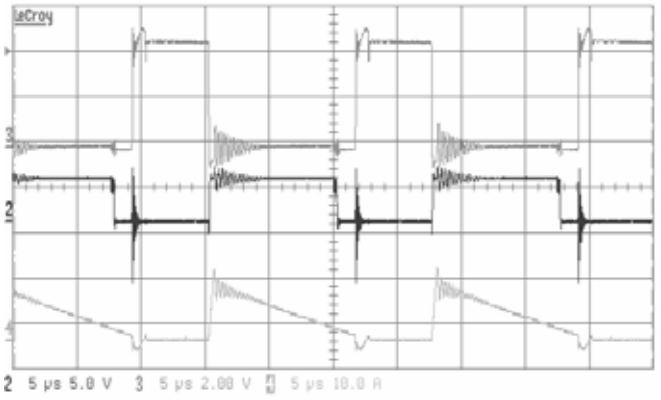


Fig. 6

For light load condition, the equivalent waveform with correct resistor value connected to Timing pin is demonstrated in figure 7. The output of MOSG-C pin is turned ON at every cycle. Observe during "ring-back", the MOSFET remains OFF. The dv/dt filter will differentiate between the true power pulses from the "ring-back" pulses.

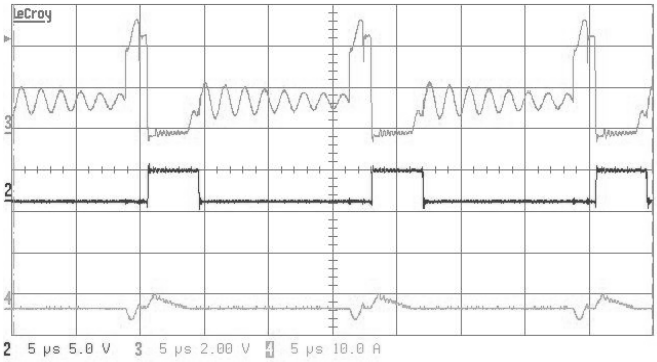


Fig. 7

SYNC Voltage

The Sync input voltage stands between VDD and VDD + 0.5 volts. It is necessary to use a resistor divider if the Sync voltage is much higher than 5 volts. R4 and R5 function as a voltage divider, in which the voltage from the secondary side of the transformer might reach as high as 40V-60V. The maximum allowable voltage for this pin is 7.5 volts. When the voltage is reached above this limit, the IC may suffer permanent damage. Therefore, it is recommended to insert a 1-5KΩ resistor in between Sync, Pin 1, to ground so the voltage can be lowered.

Here is another example of a 3.3V/3.69A output converter with everything adjusted at no load:

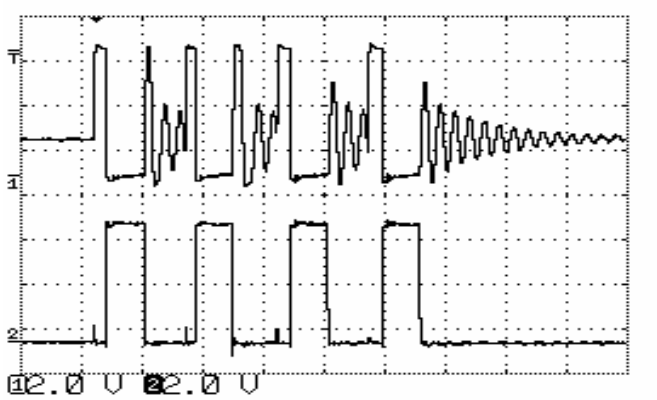


Fig. 8

In this application, the resistor for Timing pin is adjusted at 8.80KΩ to VDD and no Cramp capacitor is needed. The converter is using a green-mode PWM IC at primary side, and figure 8 demonstrates the output, MOSG-C (channel 2), during burst mode (channel 1).

Rapid Adjustment

The internal "Rapid Adjustment" circuit initiates a delay to assure that the drive circuit will not false trigger when there is a very fast reduction in pulse width required in the pulse width modulation. This can occur in regulators for very high di/dt load changes demanded by such loads as microprocessors. False triggering could result in a high cross conduction current for a few nanoseconds. A capacitor can be connected among Rapid-Adj to ground that sets the amount of filtering. For most applications, a capacitor of 100 pF is suitable.

Alternate Power Source

For applications with single set of transformer output, a way to deliver power to the IC can be derived from the isolated secondary voltage via a voltage regulator KA7805 or 78L05 as shown in figure 3. KA7805 is selected in this application. An input (0.33uF) and output (0.1uF) capacitor is also required for the voltage regulator. This is an acceptable approach for voltages from 6.5 volts minimum ripple valley voltage to 35 volts maximum peak voltage.

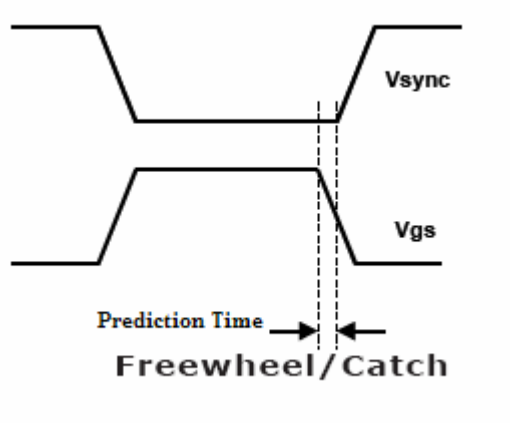
Some converters have output rated at 5V, an alternate power source for the IC could be delievered from that source, figure 9 demonstrates this schematic:

MOSG-C

Since the output of this IC delivers a square wave of 0~5 volts at various frequencies, a logic level MOSFET is most applicable for the Synchronous Rectifiers. R3 is recommended at 5Ω and D2 is a small signal Schottky diode, such as BAT54, 1N5817, or 1N5819 or switching diode 1N4148.

Predictive timing circuit operation (Pred)

The IC operates on the principle of "prediction". For freewheeling (catch) control applications, the prediction time is defined as time interval from the falling edge of Vgs to the rising edge of the synchronizing signal as shown at below. The goal is to keep prediction time as short as possible to keep minimum body diode conduction.



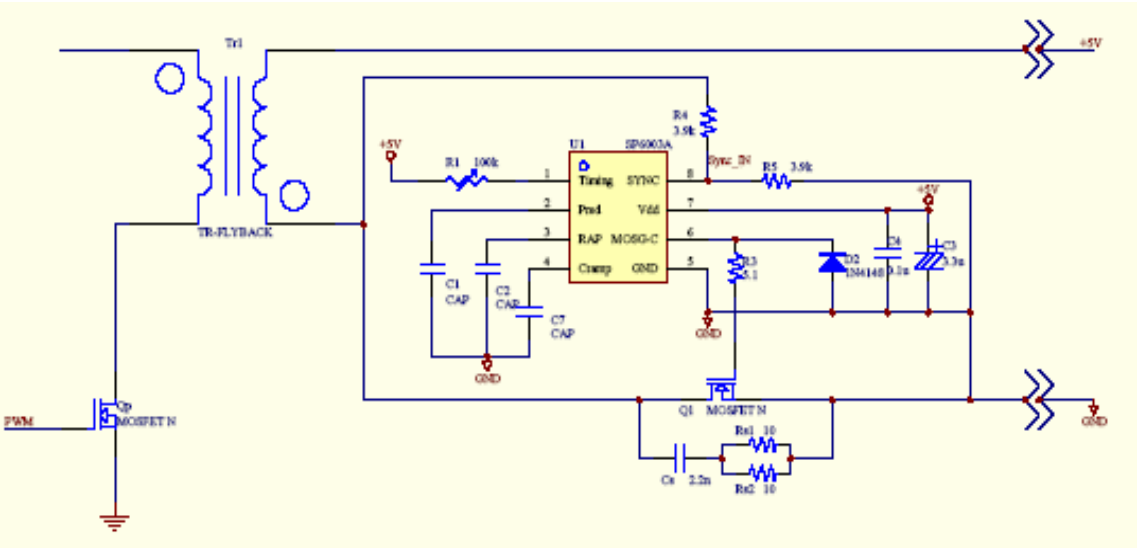


Fig. 9: Alternative Power Source Circuit

The Prediction logic uses the previous cycles to control SR operation in the present cycle. The predictive turn OFF time is adjusted by the capacitance on Pred pin. When the actual prediction time is more than that set by the capacitance on Pred pin, the IC reduces the Prediction time in the next cycle. When the actual prediction time is less than that set by the capacitance on Pred pin, the IC increases the prediction time in the next cycle.

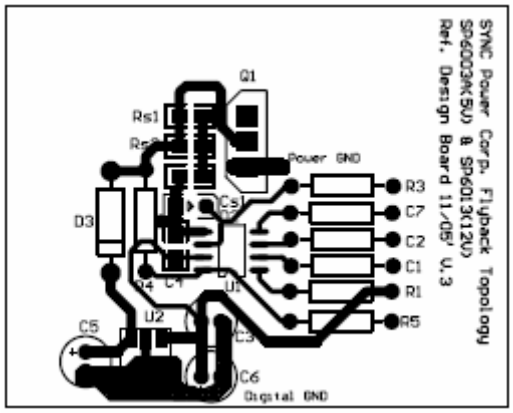


Fig. 10: Front View (1.5x its actual size)

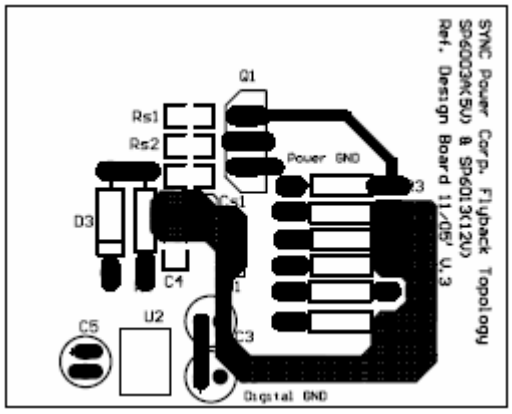


Fig. 11: Back View

Reference Design Board

To familiar with SP6003A, the reference design board should be checked by using function generator before connecting to the converter. Do not connect the MOSFET onto the reference board. Force 5V Vdd at C6 of the board and force square wave at R5 which is connected to the SYNC pin of SP6003A. The square wave should be adjusted to V_H> 3.9V and V_L<0.9V. MOSG-C pin will have a square wave shown.

There are a couple of necessary steps when installing the reference design board onto an existing flyback converter:

Step 1: Short out the existing Schottky diode.

Step 2: Find the ground connection from the output of the transformer and split it to two segments. When doing so, be as close to the transformer's output as possible and try to avoid contacts with any other components.

Step 3: Place any MOSFET with drain connecting to the output of the transformer and source to the other segment that was split from step 2. It is best if attached directly onto the PCB/converter directly. At this point, the gate should connect to source.

Step 4: Try turn on the converter and it should able to generate output, even though it is using the body diode of the MOSFET to conduct.

Step 5: Remove the MOSFET from step 4 and place the reference design board by attaching the drain and source of the MOSFET from the reference board to the converter.

Step 6: Voltage divider. In most application, the peak input voltage is more than 25 volts into pin 8, SYNC; the recommended voltage at this pin is 5-7.5 volts. R4 & R5 are used as voltage divider. Two 3.3-3.9K resistors are used for default settings.

Step 7: Timing adjustment. The Timing adjustment should be performed under light load circumstance. A variable resistor, 0~100KΩ, is connected from Timing pin to V_{DD} and adjust the variable resistor. Changing the resistor value will change dv/dt slope. This resistor value normally is from 8Kohm to 20Kohm. The typical relation between resistor value and the Delta T is shown in Figure 12.

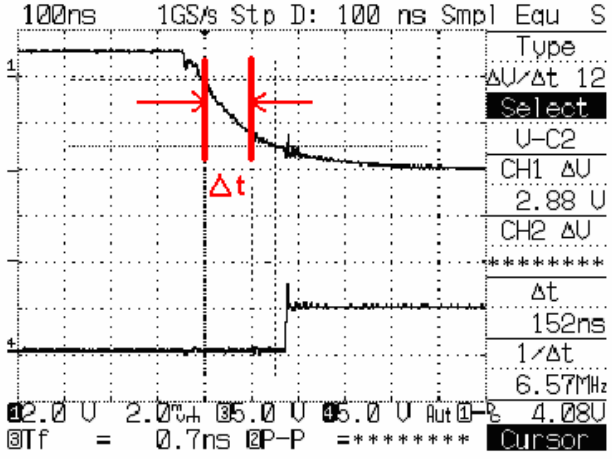


Fig.12

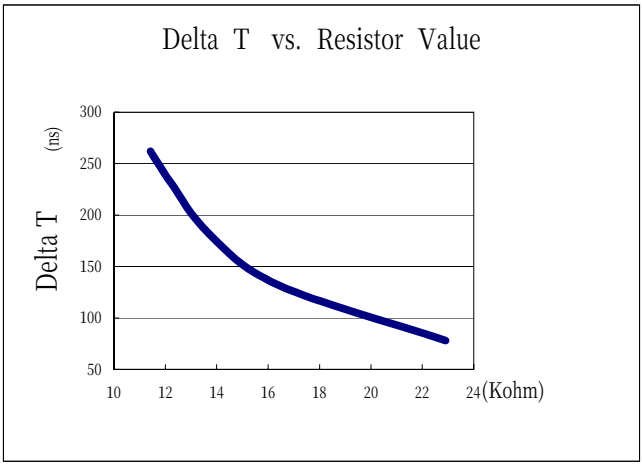


Fig. 13

Once the resistor value is adjusted correctly, the SP6003A gate will be triggered as shown in Figure 14.

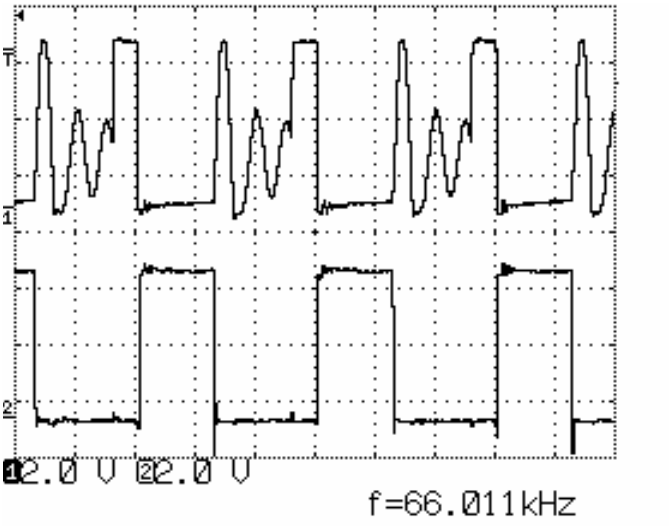


Fig. 14
Ch 1 : Drain Waveform ; Chl 2 : Output Gate Waveform

Step 8: Cramp selection. The size of this capacitor is frequency dependent. The recommended value ranges from 10pF to 100pF. Please refer to page 1 for more details.

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