Analysis of the Active-Clamped Soft-Switched Forward Converter without Output Filter

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Abstract – **This paper analyzes an active-clamped soft-switched forward converter without output filter. Differently from the topology presented in [1], the transformer reset is obtained by using an active clamp subcircuit instead of a loss-less passive snubber. This solution avoids the use of a second inductor and auxiliary diodes and allows a better exploitation of the converter components, since now both the main and the auxiliary switch turn on at zero voltage and zero current, and they turn off at zero voltage by using a loss-less capacitor. The resulting topology is practically identical to that of an active-clamped flyback converter, except for the reversed transformer secondary side polarity. Thus, in addition to the converter analysis, the paper presents a comparison between the proposed converter and the active-clamped flyback converter, by testing two prototypes rated for 48W output power.**

I. INTRODUCTION

Many isolated DC-DC converter topologies suitable for low power applications have been presented in the literature, showing various characteristics, depending on the particular application and input-output specifications. All of them try to reduce size and cost of the overall converter by using the minimum number of passive components, especially of the magnetic ones. The DCM forward converter without output filter [1] follows this guideline for the main power stage, even if it uses a snubber inductor to provide a proper transformer core reset. In this paper, the loss-less passive snubber employed in [1] has been substituted by an active clamp with the advantage of reducing the component count and increasing the converter operating range. The resulting topology appears to be similar to the so called direct coupling converter (DCC) presented in [2], where an asymmetrical half bridge is used for supplying the converter. However, the use of the active clamp instead of the asymmetrical half bridge changes the converter behavior, that is worth investigating. Moreover, the presented topology turns out to be identical to an active-clamped flyback converter, except for the reversed connection of the transformer secondary winding [3,4]. Thus, it is interesting to compare the two topologies, moving from a given set of converter specifications.

In the following sections, a detailed converter analysis is presented, aimed to identify a suitable design procedure. Experimental tests done on a forward and a flyback prototype, allow to highlight merits and limitations of the presented topology.

II. CONVERTER DESCRIPTION

The proposed active-clamped soft-switched forward DC-DC converter without output filter is shown in Fig. 1. As already explained in [1], the absence of the output filter allows DCM operation only, making this topology suitable for low power applications.

The active clamp is used to provide proper reset for the transformer, whose primary leakage inductance is denoted as L_d in Fig. 1. According to step-down operation, the output voltage U_{op} reflected to the transformer primary side must be lower than the input voltage U_g. The lossless snubber capacitor C_S includes the MOSFET output capacitances as well as any stray capacitance between the S_1 drain node and ground. As explained in the following, this capacitance provides zero voltage switching at turn off as well as a controlled dv/dt across switches, while the DCM operation implies zero current and zero voltage switch turn on as well as a soft rectifier diode turn off. The converter main waveforms in a switching period are shown in Fig. 2. As we can see, each switching period can be subdivided into five intervals described in the following. In order to simplify the notation, the time origin was implicitly selected at the beginning of each sub-interval. For the precise behavior of current and voltage waveforms refer to Appendix A.

Interval $T_{0l} = T_l - T_0$ *[see Fig. 3a].* Instant T_0 marks the end of the "off" interval of the main switch and begins when the auxiliary switch S_2 is turned off under zero voltage condition. The primary current i_d, that was flowing through S_2 and C_r, starts to discharge capacitor C_S, charged at

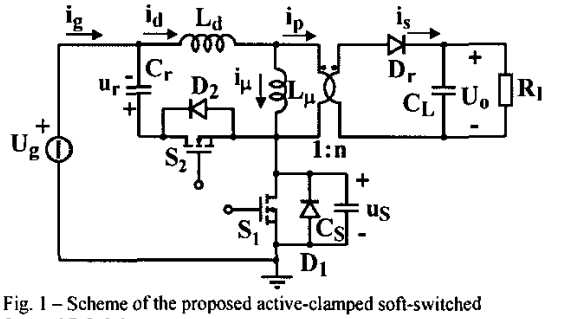

Fig. 1 – Scheme of the proposed active-clamped soft-switched forward DC-DC converter.

voltage $U_1 = u_S(T_0)$, in a resonant way until the transformer primary voltage becomes equal to the output voltage reflected to the primary side U_{op}. This condition is expressed by the following equation ($n = N_2/N_1$ is the transformer turns ratio):

$$\left(U_g - u_S(T_1)\right)\frac{L_\mu}{L_d + L_\mu} = U_{op} = \frac{U_o}{n} \qquad (1.a)$$

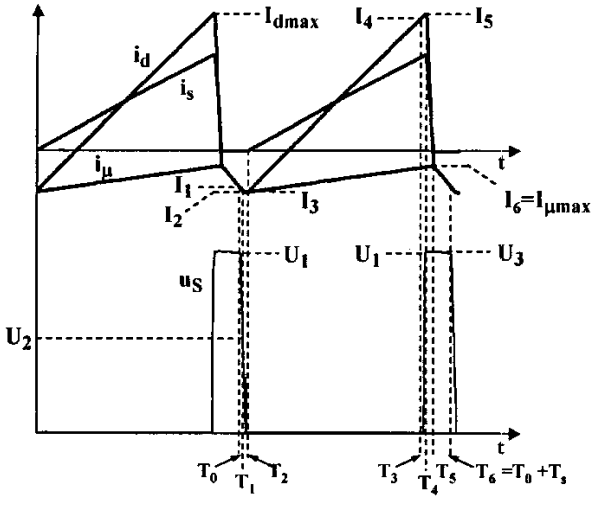

Fig. 2 – Main converter waveforms in a switching period

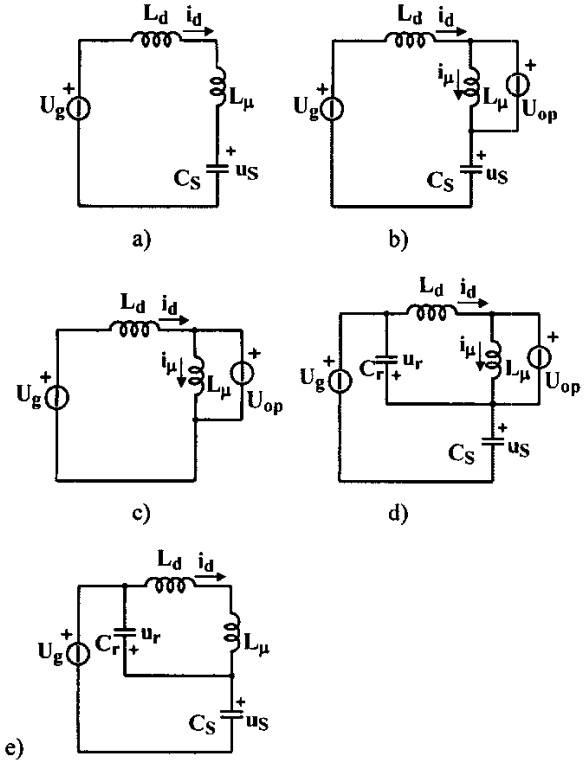

Fig. 3 - Subcircuits corresponding to different intervals during a switching period. a) interval T_{01}; b) interval T_{12}+ T_{34}; c) interval T_{23}; d) interval T_{45}; e) interval T_{56}

$$u_S(T_1) = U_2 = U_g - U_{op}\left(1 + \frac{L_d}{L_\mu}\right) = U_g - U_{op}(1+\beta) \qquad (1.b)$$

where $\beta = L_d/L_\mu$. The value of current $i_d = i_\mu$ at the end of this interval has been denoted as I_2 (see Fig. 2).

Interval $T_{12} = T_2$-T_1 [see Fig. 3b]. At instant T_1, the secondary diode D_r starts conducting clamping the transformer primary voltage to U_{op}. Consequently, the magnetizing current begins to increase linearly, according to (2), while the leakage inductance L_d continues to resonate with capacitor C_S bringing its voltage to zero at instant T_2 and turning on S_1 body diode D_1. Thus, the end of this interval is imposed by the condition $u_S(T_{12}) = 0$ and the corresponding value of current i_d is denoted as I_3.

$$i_\mu(t) = I_2 + \frac{U_{op}}{L_\mu}t \qquad (2)$$

Interval $T_{23} = T_3$-T_2 [see Fig. 3c]. This interval represents the actual switch on-time during which energy is transferred to the output from the source. The constant voltages across both L_d and L_μ impose a linear increase of the respective currents, i.e.:

$$i_d(t) = I_3 + \frac{U_g - U_{op}}{L_d}t \qquad (3)$$

while i_μ continues to follow the relation (2). Note that from instant T_2 until current i_d reverses polarity, the main switch S_1 can be turned on at zero voltage and current. At the end of this interval the value of current i_d is I_4 (see Fig. 2).

Interval $T_{34} = T_4$-T_3 [see Fig. 3b]. S_1 is opened at instant T_3 starting a resonance between L_d and C_S: the voltage across S_1 increases until D_2 starts conducting. The magnetizing current i_μ continues to increase linearly according to (2). At the end of this interval the value of current i_d is I_5 (see Fig. 2).

Interval $T_{45} = T_5$-T_4 [see Fig. 3d]. The turn on of diode D_2 puts the reset capacitor C_r dynamically in parallel with C_S and clamps the switch voltage at u_r+U_g. Consequently, while i_μ continues to increase, i_d decreases until the two currents become equal at instant T_5. This zeroes the secondary current i_s causing the turn off of the secondary diode D_r. Note that from instant T_4 until current i_d reverses polarity, the auxiliary switch S_2 can be turned on at zero voltage and current.

Interval $T_{56} = T_6$-T_5. During this interval the two inductances L_d and L_μ together resonate with C_r+C_S ending the switching interval. At instant T_6 the voltage across the main switch equals U_1 (steady-state operation).

III. Simplified Analysis

In order to find a reasonable design procedure for this converter it is convenient to make the following simplified

assumptions (see Fig. 2): $T_{01} = T_{12} = T_{34} = 0$, $I_1 = I_2 = I_3 = I_{\mu min}$, $I_4 = I_5 = I_{dmax}$, $u_r(t) = U_r$ = constant.

According to these simplifications, the switching period can be subdivided into two main phases: *powering phase* $T_{PW} = T_{ON}+T_R$, and *idling phase* $T_I = T_S-T_{PW}$.

1) Powering phase $T_{PW} = T_{ON}+T_R$. In this phase, that corresponds to interval $T_{23}+T_{35}$ in Fig. 2, the magnetizing current increases linearly according to the following relation:

$$i_\mu(t) = I_{\mu min} + \frac{U_{op}}{L_\mu} t \tag{4}$$

and its maximum value is reached at the end of this interval:

$$I_{\mu max} = i_\mu(T_{PW}) = I_{\mu min} + \frac{U_{op}}{L_\mu} T_{PW} \tag{5}$$

Current i_d, instead, increases linearly during T_{ON} and decreases linearly during T_R, i.e.:

$$i_d(t) = I_{\mu min} + \frac{U_g - U_{op}}{L_d} t \quad 0 \le t \le T_{ON} \tag{6}$$

$$I_{dmax} = i_d(T_{ON}) = I_{\mu min} + \frac{U_g - U_{op}}{L_d} T_{ON} \tag{7}$$

$$i_d(t) = I_{dmax} - \frac{U_r + U_{op}}{L_d}(t - T_{ON}) \qquad T_{ON} \le t \le T_{ON} + T_R \tag{8}$$

At the end of this phase currents i_d and i_μ are equal, i.e.:

$$I_{\mu min} + \frac{U_{op}}{L_\mu}(T_{ON} + T_R) = I_{dmax} - \frac{U_r + U_{op}}{L_d} T_R = I_{\mu min} + \frac{U_g - U_{op}}{L_d} T_{ON} - \frac{U_r + U_{op}}{L_d} T_R \tag{9}$$

In the last equation the relation (7) was used. Note that (7) gives also the peak current in both main and auxiliary switches, while the peak current in the secondary diode D_r is I_{dmax}/n.

2) Idling phase $T_I = T_S+T_{PW}$. In this phase, currents i_d and i_μ remain equal and are given by:

$$i_d(t) = I_{\mu max} - \frac{U_r}{L_d + L_\mu}(t - T_{PW}) \qquad T_{PW} \le t \le T_S \tag{10}$$

From the above relations we are now able to find all the parameters needed for a correct converter design. In particular, from the volt-second balance across L_μ, we can write:

$$U_{op}(d + d_R) = U_r \frac{L_\mu}{L_d + L_\mu}(1 - d - d_R) \tag{11}$$

where $d = T_{ON}/T_S$ is the converter duty-cycle and $d_R = T_R/T_S$. Using (9) and (11) and eliminating d_R, the following simple estimation for the voltage across capacitor C_r is derived:

$$U_r = \frac{d}{1-d} U_g \tag{12}$$

Substituting (12) into (11) gives the following expression for d_R:

$$d_R = \frac{d(1-d)(U_g - U_{op}(1+\beta))}{d(U_g - U_{op}(1+\beta)) + U_{op}(1+\beta)} \tag{13}$$

where $\beta = L_d/L_\mu$.

The average current through the secondary diode D_r can now be calculated:

$$\bar{i}_{sec} = \frac{\bar{i}_d - \bar{i}_\mu}{n} = \frac{1}{nT_s}\int_0^{T_{PW}} (i_d(\tau) - i_\mu(\tau))d\tau = \frac{d^2}{2nf_s L_d} \frac{U_g(U_g - U_{op}(1+\beta))}{d(U_g - U_{op}(1+\beta)) + U_{op}(1+\beta)} = \frac{U_o}{R_L} \tag{14}$$

where the last equality comes from steady-state operation hypothesis. From (14), an expression for the voltage conversion ratio as a function of duty-cycle and load resistance can be derived as follows:

$$M_p = \frac{U_{op}}{U_g} = -\frac{d}{2(1-d)}\left(\frac{1}{1+\beta} + \frac{d}{k}\right) + \sqrt{\left[\frac{d}{2(1-d)}\left(\frac{1}{1+\beta} + \frac{d}{k}\right)\right]^2 + \frac{d^2}{k(1-d)(1+\beta)}} \tag{15}$$

where $k = 2L_d f_s/R_{Lp}$ is the a-dimensional parameter usually found in DCM operating converters.

The average current supplied by the input voltage generator is given by:

$$\bar{i}_g = \frac{1}{T_s}\int_0^{T_{ON}} i_d(\tau)d\tau = I_{\mu min} d + \left(\frac{U_g - U_{op}}{2L_d f_s}\right) d^2 = \bar{i}_{sec} \frac{U_o}{U_g} \tag{16}$$

where the last equality comes from the converter power balance under the assumption of unity efficiency. From (16), (14) and (5) it is possible to find the following expressions for the magnetizing current:

$$I_{\mu min} = -\frac{dU_{op}}{2f_s L_d} \frac{\beta + d(1 - M_p(1+\beta))\left(\frac{1}{M_p} - 1\right)}{d(1 - M_p(1+\beta)) + M_p(1+\beta)} \tag{17}$$

$$I_{\mu max} = -\frac{dU_{op}}{2f_s L_d} \frac{-\beta + d(1 - M_p(1+\beta))\left(\frac{1}{M_p} - 1\right)}{d(1 - M_p(1+\beta)) + M_p(1+\beta)} \tag{18}$$

$$I_{\mu avg} = -\frac{dU_{op}}{2f_s L_d} \frac{d(1 - M_p(1+\beta))\left(\frac{1}{M_p} - 1\right)}{d(1 - M_p(1+\beta)) + M_p(1+\beta)} \tag{19}$$

As far as the component voltage stresses are concerned, the peak voltage across main and auxiliary switches is given by:

$$U_{Smax} = U_r + U_g = \frac{U_g}{1-d} \tag{20}$$

where (12) has been used. The maximum voltage across the secondary diode D_r is:

$$U_{Drmax} = n\frac{U_r}{1+\beta} + U_{op} \tag{21}$$

Fig. 4 reports the behavior of the main converter design parameters calculated using the set of converter component values listed in Table I. Fig. 4a shows the control

characteristics, i.e. the voltage conversion ratio as a function of the duty-cycle for different values of parameter *k*. As we can see these characteristics are much similar to the usual control characteristics of a buck converter operating in DCM. The theoretical maximum voltage conversion ratio corresponding to a unity duty-cycle is given by:

$$M_{p\max} = \frac{1}{1+\beta+k} \qquad (22)$$

Looking at (19) and taking (22) into account, we can easily verify that the average magnetizing current is always negative, thus the transformer operates like two coupled inductors, storing a non negligible energy. As a consequence, an air gap should be used in order to avoid the core saturation. This also helps to obtain the desired leakage inductance L_d.

The maximum voltage across the switches and secondary diode at nominal power as a function of converter duty-cycle is reported in Fig. 4b: like any active-clamp structure, there is no theoretical limitation on maximum duty-cycle

Table I - Converter parameters used in Fig. 4

U_g = 12+24V	U_o = 12V	P_o = 50W
L_d = 1μH	C_S = 2.5nF	C_r = 1μF
L_μ = 10μH	n = 1.67	f_S = 200kHz

except for the need to maintain the switch voltage stress at a reasonable level. On the other hand, the converter presented in [1] had both a maximum and minimum duty-cycle limitation in order to ensure a proper operation of the loss-less snubber and a proper transformer core reset. Note that the maximum voltage across the switches may not correspond to the maximum input voltage as (20) could suggest, because of the different duty-cycle needed to obtain the corresponding voltage conversion ratio (the curves are obtained from (12) and (20) keeping the output voltage constant). In Fig. 4c, the values of the magnetizing current and the peak input current are reported as a function of duty-cycle at nominal power: as we can see the component current stress rapidly increases at lower duty-cycle values (higher input voltage values). This behavior is likely to reduce the converter efficiency when the converter must be designed for operation with a wide input voltage range.

IV. Soft-Switching Condition

In this converter, the main switch turns on at zero voltage and zero current only if capacitor C_S is completely discharged before the application of the turn on command signal to S_1. The reverse condition applies to the auxiliary switch S_2, i.e. the capacitor C_S must be completely charged to U_r+U_g value before the turn on of S_2. In order to ensure the soft-switching condition for S_1, intervals T_{01} and T_{12} must be analyzed. In particular, during interval T_{12}, voltage u_S must reverse, thus turning on the S_1 body diode D_1. This condition can be checked by controlling that the minimum value reached by voltage u_S, if it was not clamped by diode D_1, is negative. Following this procedure, using (A.4) and considering a constant current value $I_{\mu\min}$ during the two time intervals, the minimum output power that still guarantees the soft-switching condition for S_1 was found to be one tenth of the nominal power.

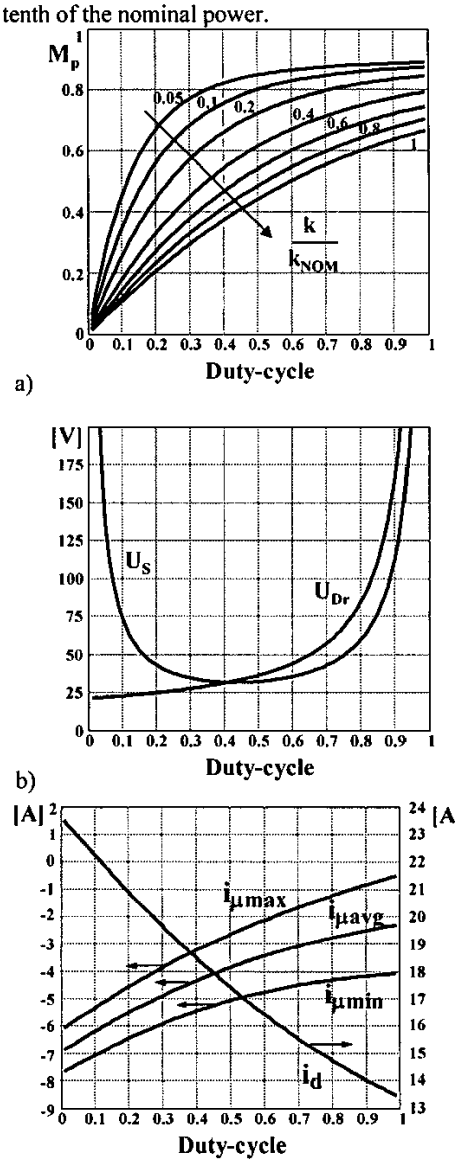

Fig. 4 - Main converter design parameters calculated using the set of converter component values listed in Table I as a function of duty-cycle. a) voltage conversion ratio for different values of the normalized parameter k; b) switch and secondary diode voltage stress at nominal power; c) magnetizing current and peak input current values

As far as S_2 soft-switching condition is concerned, we must ensure that during interval T_{34} the voltage u_S reaches the value U_r+U_g causing the turn on of diode D_2. Once again, this condition can be checked by calculating the maximum value voltage u_S can reach during the resonance between C_s and L_d, if it was not clamped by the turn on of diode D_2. In order to do that, eq. (A.7) was used and considering an input current value equal to I_{dmax}: it is easily to see that for the given converter parameters the soft-switching condition for S_2 is always satisfied. From (A.1),

(1.b), (A.4), and (A.7) it is possible to estimate the time intervals $T_{01}+T_{12}$ and T_{34} that give an indication of the dead times needed between the S_1 and S_2 drive signals in order to obtain the correct soft-switching commutation.

V. Design Considerations

From the analysis carried out in the previous sections, we have seen that the converter parameters must be chosen in order to suit the desired input voltage and output current ranges, while minimizing voltage and current stresses in the main devices. Moreover, the soft-switching condition should be maintained for an as wide as possible load range.

The two parameters that have the greater impact on converter performance are the transformer turns ratio n and the leakage inductance L_d. To give an idea of their effect, Fig. 5 reports different component stresses as a function of the transformer turns ratio *n* for different L_d values (the other converter parameters are those listed in Table I). For each *n* value five parameters are shown (from left to right): $I_{\mu min}$, I_{dmax}, I_{Drmax}, U_{Smax}, U_{Drmax}. From these data we can make the following considerations:

- lower L_d values cause an increase of switch and diode current stress and a decrease of the absolute value of the magnetizing current negative peak, together with a decrease of switch and diode voltage stress;
- higher *n* values cause a slight increase of switch current stress and of the absolute value of the magnetizing current negative peak, while the diode current stress decreases together with the maximum switch and diode voltages. Note that the voltage stress variation reduces at higher turns ratios.

Table II – Component stresses at different magnetizing inductance values (other parameters as in Table I)

L_μ [μH]	d_{onmax}	$I_{\mu min}$ [A]	I_{dmax} [A]	I_{Drmax} [A]	U_S [V]	U_{Dr} [V]
5	0.90	-6.90	19.9	12.0	115	155
10	0.80	-5.88	19.6	11.8	59	83
20	0.75	-5.37	19.5	11.7	49	70

Note that for any L_d value, there is a limited range of possible transformer turns ratios.

As a good compromise between current and voltage stresses, the values reported in Table I were selected. Finally, Table II reports the same converter parameters for three different magnetizing inductance values, demonstrating the weak impact of such parameter on component stresses.

As a last comment, the voltage stress reported in Fig. 5 and Table II neglects the voltage ripple across capacitor C_r, so that a suitable safety margin should be considered when calculating these values.

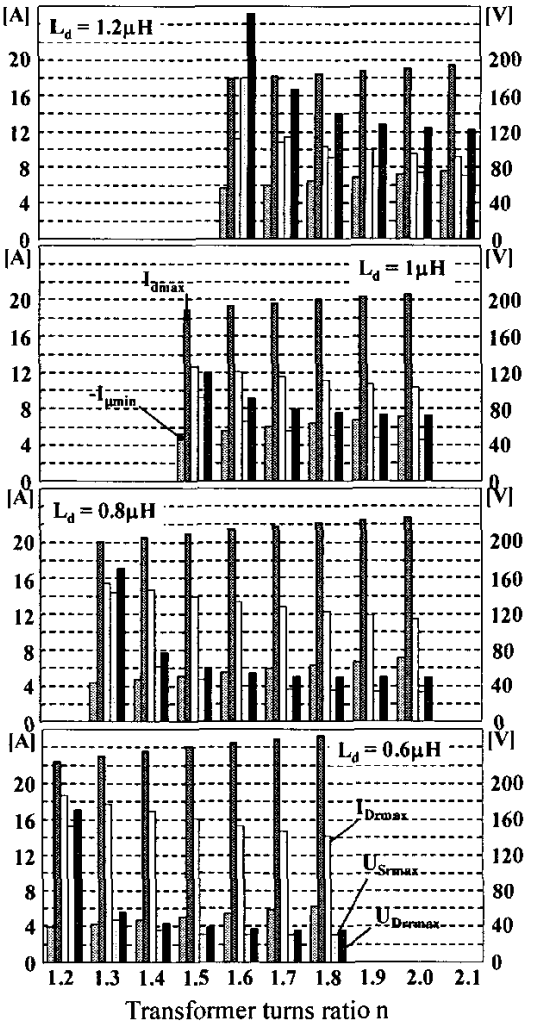

Fig. 5 – Component stresses as a function of transformer turns ratio n at different L_d values

VI. Experimental Results

A two complementary outputs converter prototype, whose parameters are given in Table I, was developed. The transformer was built on a RM10 core size (N_1=3, N_2=5+5) and an external E14 core (N=3) was used to obtain the desired overall leakage inductance L_d. A R = 100Ω-C = 500pF series snubber was used across each secondary diode in order to damp parasitic oscillations caused by the transformer secondary leakage inductance. A 10μF polyester output filter capacitor was used for each output and also for the input. The employed active components are IRF540 MOSFET and DSS16-01 Schottky diodes. Fig. 6 reports the main converter waveforms in a switching period at nominal output power for minimum and maximum input voltages: as we can see, the converter behaves as predicted by the theoretical analysis, except for the presence of a 10V voltage spike across the main switch caused by component and layout parasitic inductance in the loop comprising C_s,

D_2, C_r and the input capacitor (not shown in Fig. 1). Note the negative U_{GS} voltage at the beginning of the S_1 turn on interval revealing the soft-switching commutation. Observe that the non linear behavior of input current i_d during the turn on interval is caused by a substantial ripple on the input capacitor and a non negligible voltage drop across the main switch caused by its on resistance.

For the purpose of comparison an active-clamped flyback converter was built using the same specifications and employing practically the same components (with only a different transformer turns ratio). The main converter waveforms are shown in Fig. 7: once again, the zero voltage commutation is ensured, while the CCM operation allows to process the same power with a lower current stress, especially at higher input voltages. Note also, the much lower duty-cycle variation to cope with the input voltage variation, as compared to the forward converter.

Fig. 8, reports the efficiency comparison between the two prototypes: as we can see, for the used converter specifications, the flyback topology shows the best performance mainly because of the lower conduction losses. In fact, being the forward converter forced to work in DCM, its input current has a much higher RMS value as compared to the flyback one. For this reason, the presented topology should be more indicated for high-voltage low-power applications.

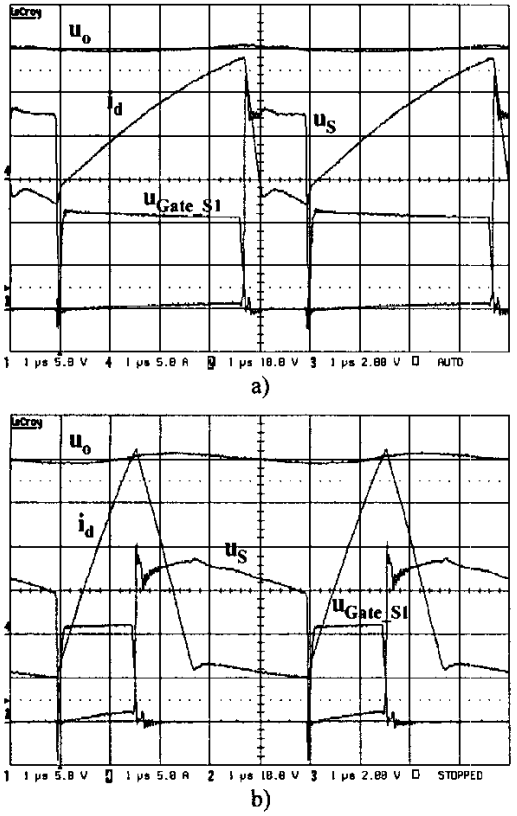

Fig. 6 - Measured main converter waveforms of the forward prototype in a switching period $U_o = \pm 12V$, $P_o = 48W$. a) @$U_g = 12V$; b) @$U_g = 24V$ (i_d: 5A/div, u_S: 10V/div, u_{GS}: 5V/div, u_o: 2V/div)

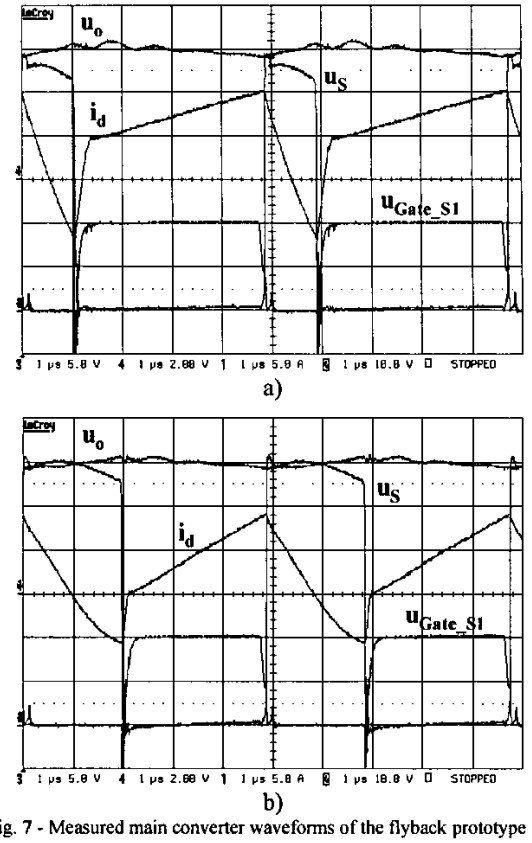

Fig. 7 - Measured main converter waveforms of the flyback prototype in a switching period $U_o = \pm 12V$, $P_o = 48W$. a) @$U_g = 12V$; b) @$U_g = 24V$ (i_d: 5A/div, u_S: 10V/div, u_{GS}: 5V/div, u_o: 2V/div)

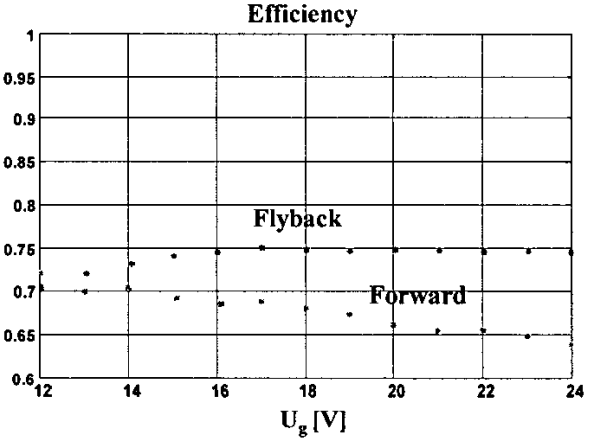

Fig. 8 – Efficiency comparison between the presented forward converter and the active-clamped flyback converter as a function of input voltage

VII. Conclusions

A simple soft-switching forward DC-DC converter suitable for low power applications is presented. The converter uses an active-clamp to provide a proper transformer reset and, at the same time, zero voltage and zero current turn-on of both switches as well as zero voltage turn-off, thanks to a loss-less snubber capacitor. The discontinuous conduction mode

(DCM) guarantees a soft diode turn off and allows to eliminate the inductive output filter. A detailed converter analysis was given, aimed to highlight advantages and drawbacks of the topology. Experimental results verify and validate the theoretical analysis.

VIII. ACKNOWLEDGMENT

The authors would like to thank Dr. Eng. Matteo Bonaldo for its support in the experimental activity.

APPENDIX

In the following, the equations describing voltage and current behavior during a switching period are given. In order to simplify the notation, the time origin was implicitly selected at the beginning of each sub-interval.

1 - *Interval* $T_{01} = T_1$-T_0. Resonant phase between L_d+L_μ and C_S:

Initial conditions: $u_S(0) = U_1$, $i_d(0) = i_\mu(0) = I_1$

Resonant angular frequency: $\omega_1 = \frac{1}{\sqrt{(L_d + L_\mu)C_S}}$

Characteristic impedance: $Z_1 = \sqrt{\frac{L_d + L_\mu}{C_S}}$

$$u_S(t) = U_g - (U_g - U_1)\cos(\omega_1 t) + Z_1 I_1 \sin(\omega_1 t) \quad (A.1)$$

$$i_d(t) = i_\mu(t) = I_1 \cos(\omega_1 t) + \left(\frac{U_g - U_1}{Z_1}\right)\sin(\omega_1 t) \quad (A.2)$$

2 - *Interval* $T_{12} = T_2$-T_1. Resonant phase between L_d and C_S:

Initial conditions: $u_S(0) = U_2$, $i_d(0) = i_\mu(0) = I_2$

Resonant angular frequency: $\omega_2 = \frac{1}{\sqrt{L_d C_S}}$

Characteristic impedance: $Z_2 = \sqrt{\frac{L_d}{C_S}}$

$$i_\mu(t) = I_2 + \frac{U_{op}}{L_\mu} t \quad (A.3)$$

$$u_S(t) = U_g - (1 + \beta\cos(\omega_2 t))U_{op} + Z_2 I_2 \sin(\omega_2 t) \quad (A.4)$$

$$i_d(t) = I_2 \cos(\omega_2 t) + \left(\frac{\beta U_{op}}{Z_2}\right)\sin(\omega_2 t) \quad (A.5)$$

3 - *Interval* $T_{23} = T_3$-T_2. Voltage u_S is clamped to zero, while i_μ follows (A.3):

Initial conditions: $i_d(0) = I_3$

$$i_d(t) = I_3 + \frac{U_g - U_{op}}{L_d} t \quad (A.6)$$

4 - *Interval* $T_{34} = T_3$-T_4. Resonant phase between L_d and C_S, while i_μ still follows (A.3):

Initial conditions: $u_S(0) = 0$, $i_d(0) = I_4$

$$u_S(t) = (U_g - U_{op})(1 - \cos(\omega_2 t)) + Z_2 I_4 \sin(\omega_2 t) \quad (A.7)$$

$$i_d(t) = I_4 \cos(\omega_2 t) + \left(\frac{U_g - U_{op}}{Z_2}\right)\sin(\omega_2 t) \quad (A.8)$$

5 - *Interval* $T_{45} = T_5$-T_4. Resonant phase between L_d and C_S+C_r so that $u_r = u_S$-U_g, while i_μ still follows (A.3):

Initial conditions: $u_S(0) = U_1$, $i_d(0) = I_5$

Resonant angular frequency: $\omega_3 = \frac{1}{\sqrt{L_d(C_S + C_r)}}$

Characteristic impedance: $Z_3 = \sqrt{\frac{L_d}{C_S + C_r}}$

$$u_S(t) = U_g - U_{op} + (U_{op} + U_1 - U_g)\cos(\omega_3 t) + Z_3 I_5 \sin(\omega_3 t) \quad (A.9)$$

$$i_d(t) = I_5 \cos(\omega_3 t) - \left(\frac{U_{op} + U_1 - U_g}{Z_3}\right)\sin(\omega_3 t) \quad (A.10)$$

6 - *Interval* $T_{56} = T_6$-T_5. Resonant phase between L_d+L_μ and C_S+C_r so that $u_r = u_S$-U_g:

Initial conditions: $u_S(0) = U_3$, $i_d(0) = i_\mu(0) = I_6$

Resonant angular frequency: $\omega_4 = \frac{1}{\sqrt{(L_d + L_\mu)(C_S + C_r)}}$

Characteristic impedance: $Z_4 = \sqrt{\frac{L_d + L_\mu}{C_S + C_r}}$

$$u_S(t) = U_g - U_{op} + (U_{op} + U_3 - U_g)\cos(\omega_4 t) + Z_4 I_6 \sin(\omega_4 t) \quad (A.11)$$

$$i_d(t) = i_\mu(t) = I_6 \cos(\omega_4 t) - \left(\frac{U_{op} + U_3 - U_g}{Z_4}\right)\sin(\omega_4 t) \quad (A.12)$$

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