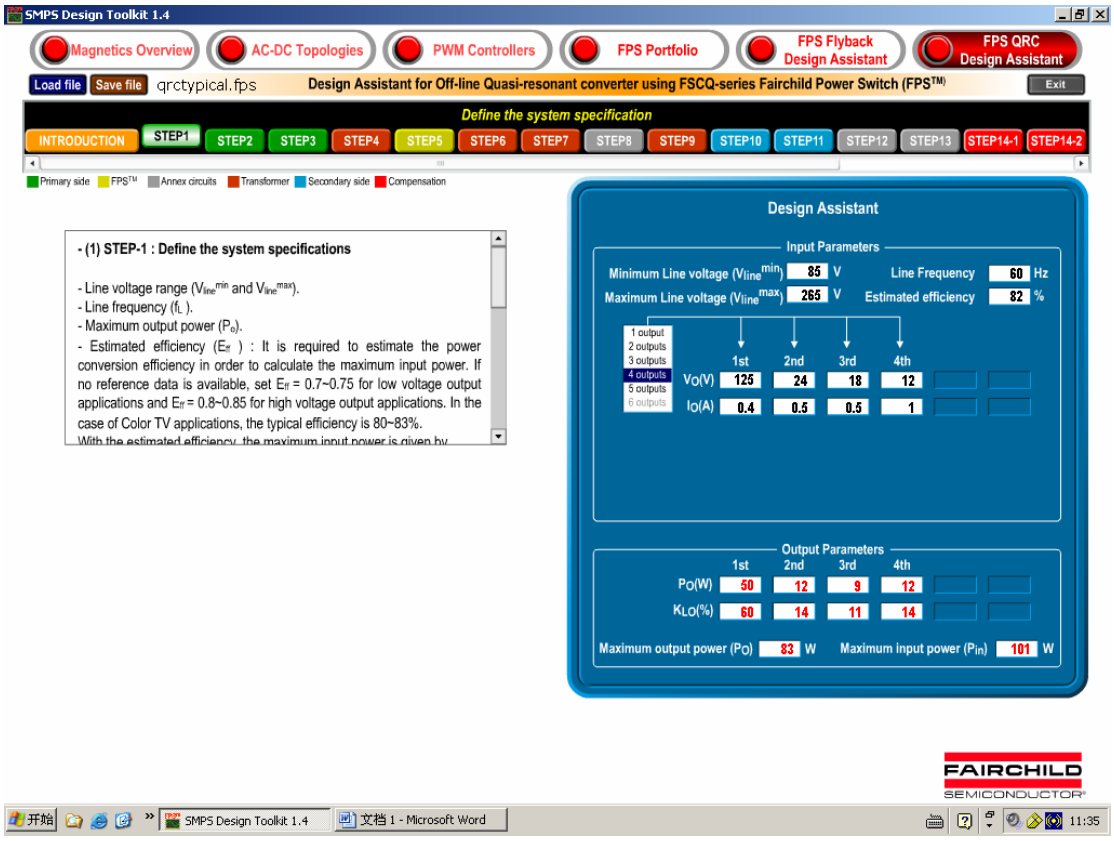

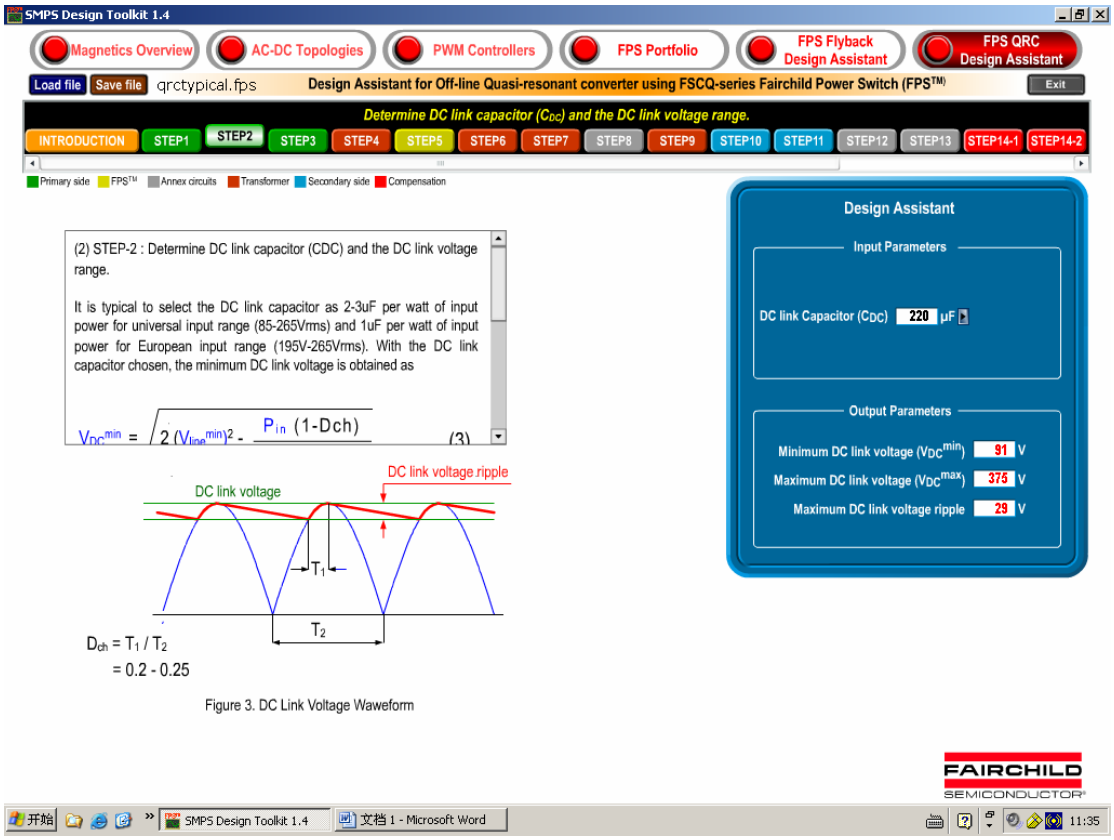

Figure 3. DC Link Voltage Waveform

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Determine the reflected output voltage (V_{RO})

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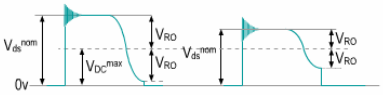
Primary side | FPS™ | Annex circuits | Transformer | Secondary side | Compensation

(3) STEP-3 : Determine the reflected output voltage (V_{RO})

Figure 4 shows the typical waveforms of the drain voltage of Quasi-resonant flyback converter. When the MOSFET is turned off, the DC link voltage (V_{DC}) together with the output voltage reflected to the primary (V_{RO}) are imposed on the MOSFET and the maximum nominal voltage across MOSFET (V_{ds}^{nom}) is given as

$$V_{ds}^{nom} = V_{dc}^{max} + V_{RO} \quad (5)$$



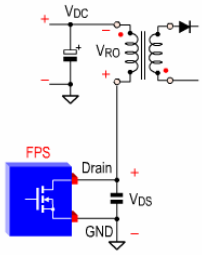


Figure 4. The typical waveform of MOSFET drain voltage

Design Assistant

Input Parameters

Output voltage reflected to primary (V_{RO}): 126

Output Parameters

Maximum nominal MOSFET voltage (V_{DS}^{nom}): 501

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Determine the transformer primary inductance (Lm)

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Primary side | FPS™ | Annex circuits | Transformer | Secondary side | Compensation

(4) STEP-4 : Determine the transformer primary side inductance (Lm)

Figure 5 shows the typical waveforms of MOSFET drain current, secondary diode current and the MOSFET drain voltage of a Quasi-resonant converter. During T_{OFF} , the current flows through the secondary side rectifier diode and the MOSFET drain voltage is clamped at (V_{DC} +V_{RO}). When the secondary side current reduces to zero, the drain voltage begins to drop by the resonance between the effective output capacitor of the MOSFET and the primary side inductance (L_m).

In order to minimize the switching loss, the FSCQ-series is designed to tur on the MOSFET when the drain voltage reaches its minimum voltage

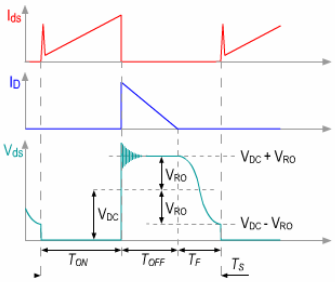

Figure 5. Typical waveforms of Quasi-resonant converter

Design Assistant

Input Parameters

Minimum Switching frequency (f_s^{min}): 24 KHz

Drain voltage falling time(T_F): 2.3 μS

Output Parameters

Maximum Duty cycle (D_{max}): 0.55

Primary side inductance (L_m): 514 μH

Maximum peak drain current (I_{ds}^{peak}): 4.05 A

RMS drain current (I_{ds}^{rms}): 1.73 A

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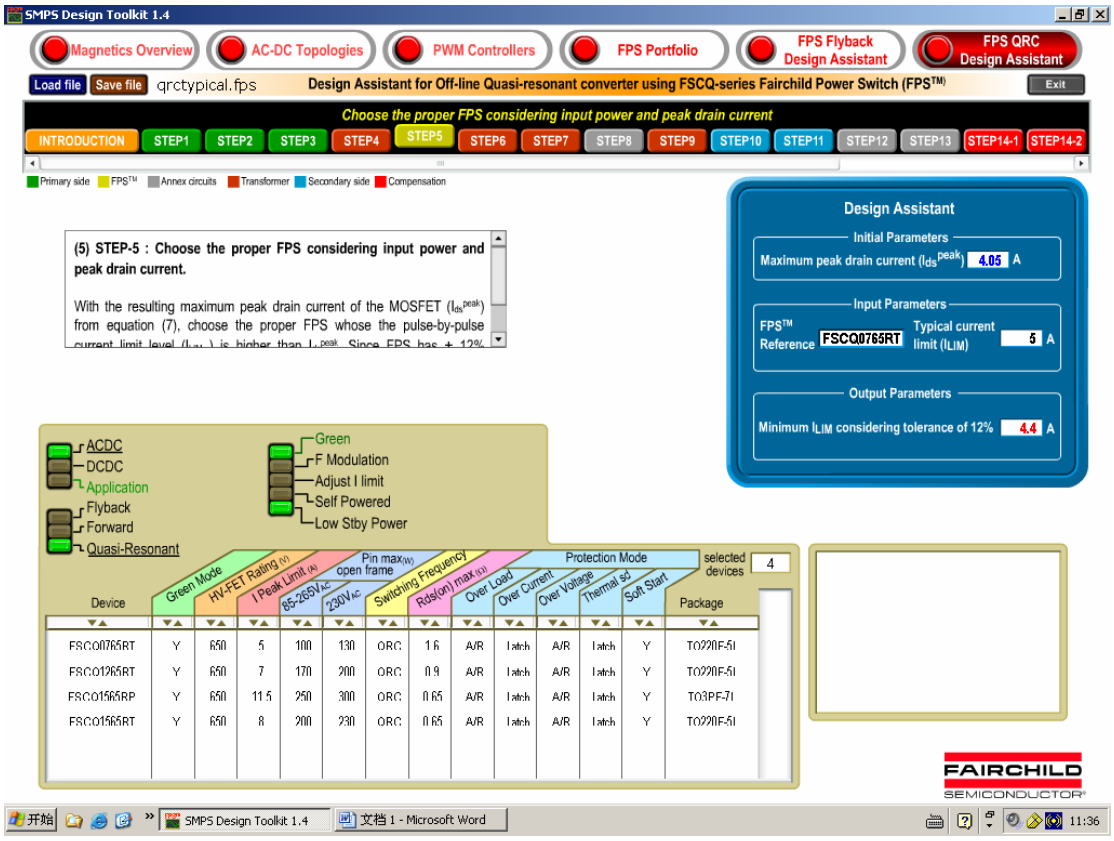

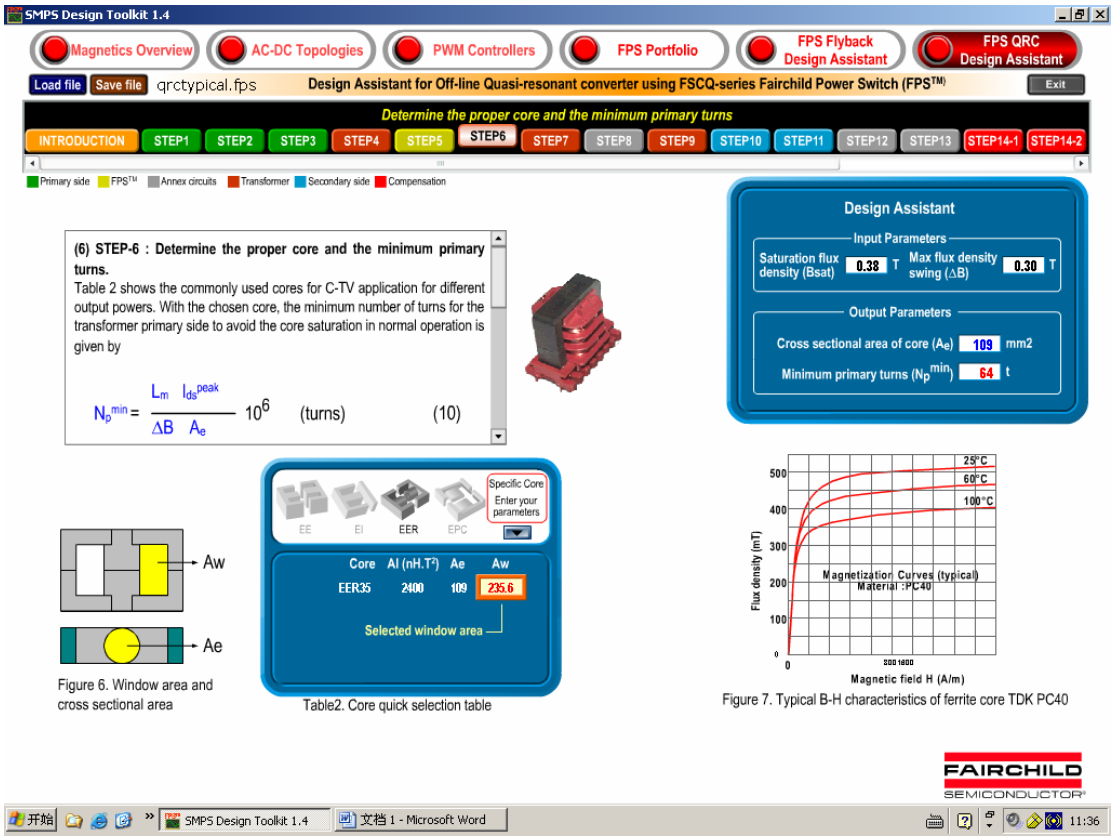

Figure 6. Window area and cross sectional area

Table2. Core quick selection table

Figure 7. Typical B-H characteristics of ferrite core TDK PC40

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Determine the number of turns for each output.

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Primary side | FPS™ | Annex circuits | Transformer | Secondary side | Compensation

(7) STEP-7 : Determine the number of turns for each output and Vcc auxiliary circuit

Figure 8 shows the simplified diagram of the transformer. It is assumed that V_{o1} is the reference output that is regulated by the feedback control in normal operation. It is also assumed that linear regulator is connected to V_{o2} to supply a stable voltage for MCU.
First, calculate the turns ratio (n) between the primary winding and reference output (V_{o1}) winding as a reference.

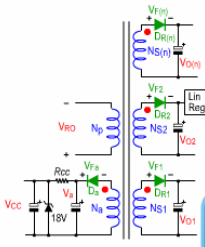

Figure 8. Simplified diagram of the transformer

Products	V_{RRM}(V)	I_F(A)	V_F(V)	T_{rr}(nS)	Package
UF4001	50	1	1	50	DO-41
UF4002	100	1	1	50	DO-41
UF4003	200	1	1	50	DO-41
UF4004	400	1	1	50	DO-41
UF4005	600	1	1,7	50	DO-41
UF4006	800	1	1,7	50	DO-41

Ultra Fast Recovery Diode

Table2. Fairchild diode quick selection table

Design Assistant

Initial Parameters — Minimum primary turns (Np^{min}): 64

		1st	2nd	3rd	4th
Outputs Vo(n)	V	125	24	18	12
Outputs Io(n)	A	0.4	0.5	0.5	1

Input Parameters

	diode Da	1st	2nd	3rd	4th
VF(n) V	1.2	1.2	1.2	1.2	1.2

Choose # of turns for 1st output: 64

Output Parameters — (Individual Windings option) — Ungapped AL value (AL): 2400 nH/T^2

	Va	1st	2nd	3rd	4th
# of turns t	20		13	10	7
Va^{normal} V	37.7	125	24.43	18.52	12.6
% error		0	1.8	2.9	5

Gap length (G); center pole gap: 1.034 mm — Primary turns (Np): 64 t

Stby mode: V_{02}^{stby} 8 V — Va^{stby} 13 V — Kdrop 0.365

Vcc drop resistor calculations: Iop 6 mA — Ciss 1840 pF — Vz 18 V — Icc 9 mA at fs 90 KHz — Rcc 1.5 KΩ must be < 2.19K — Pa= 259 mW

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Determine the startup resistor

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Primary side | FPS™ | Annex circuits | Transformer | Secondary side | Compensation

(8) STEP-8 : Determine the startup resistor

Figure 11 shows the typical circuit of Vcc winding for FSCQ-series. Initially, FPS consumes only startup current (max 50uA) before it begins switching. Therefore, the current supplied through the startup resistor (R_{str}) can charge the capacitors C_{a1} and C_{a2} while supplying startup current to FPS. When Vcc reaches start voltage of 15V (VSTART), FPS begins switching, and the current consumed by FPS increases. Then, the current required by FPS is supplied from the transformer auxiliary winding.

- Startup resistor (R_{str}) : The average of the minimum current supplied

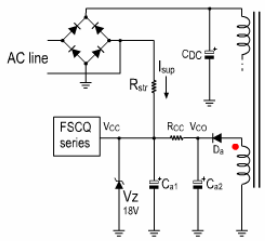

Figure 11. Startup resistor and Vcc auxiliary circuit

Design Assistant

Input Parameters

Maximum startup current of FPS (I_{start})	50	μA
Startup resistor (R_{str}) (must be < 620K)	240	KΩ
Effective Vcc capacitor (Ce)	20	μF

Output Parameters

Maximum dissipation in startup resistor (at V_{line}^{max} = 265V)	132	mW
Maximum startup time (T_{str}^{max}) (at V_{line}^{min} = 85V)	3.8	S

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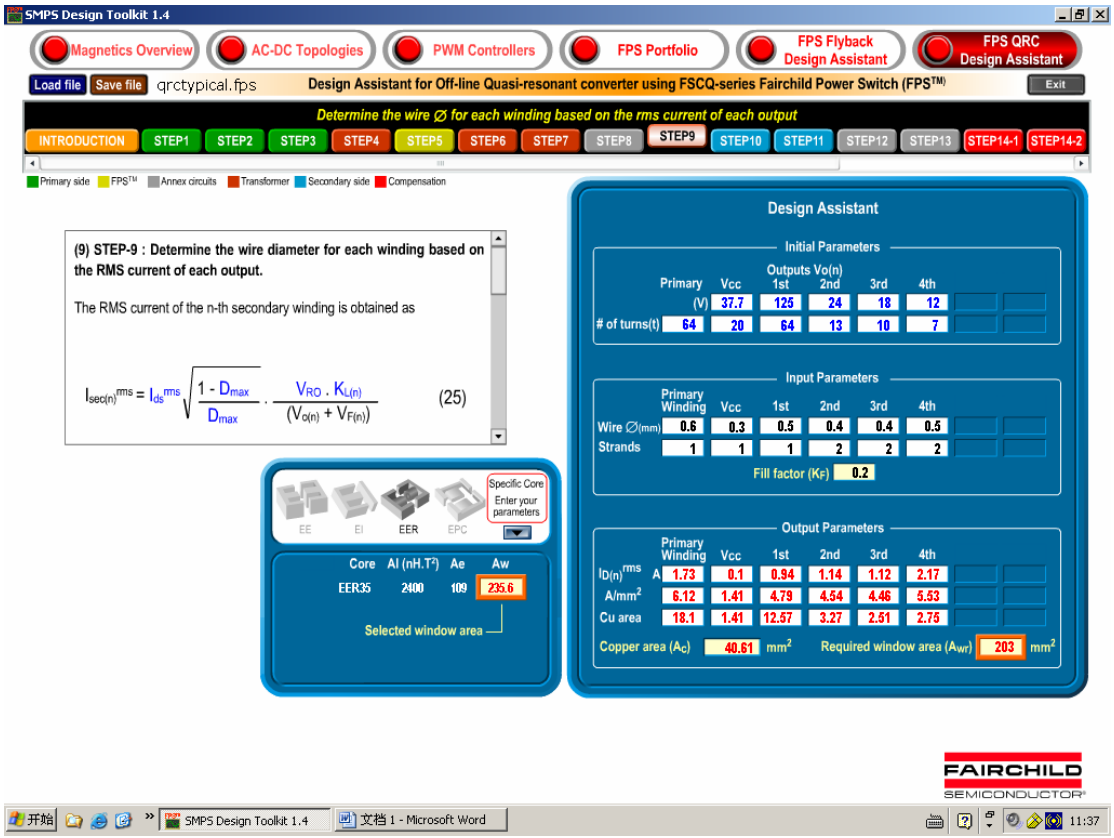
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Determine the wire ∅ for each winding based on the rms current of each output
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(9) STEP-9 : Determine the wire diameter for each winding based on the RMS current of each output.
The RMS current of the n-th secondary winding is obtained as
(25)
Design Assistant
Initial Parameters
Outputs Vo(n)
Primary
Vcc
1st
2nd
3rd
4th
(V)
37.7
125
24
18
12
# of turns(t)
64
20
64
13
10
7
Input Parameters
Primary Winding
Wire ∅(mm)
0.6
0.3
0.5
0.4
0.4
0.5
Strands
1
1
1
2
2
2
Fill factor (Kf)
0.2
Output Parameters
A
1.73
0.1
0.94
1.14
1.12
2.17
A/mm²
6.12
1.41
4.79
4.54
4.46
5.53
Cu area
18.1
1.41
12.57
3.27
2.51
2.75
Copper area (Ac)
40.61
mm²
Required window area (Awr)
203
mm²
Specific Core
Enter your parameters
EE
EI
EER
EPC
Core
Al (nH.T²)
Ae
Aw
EER35
2400
109
235.6
Selected window area
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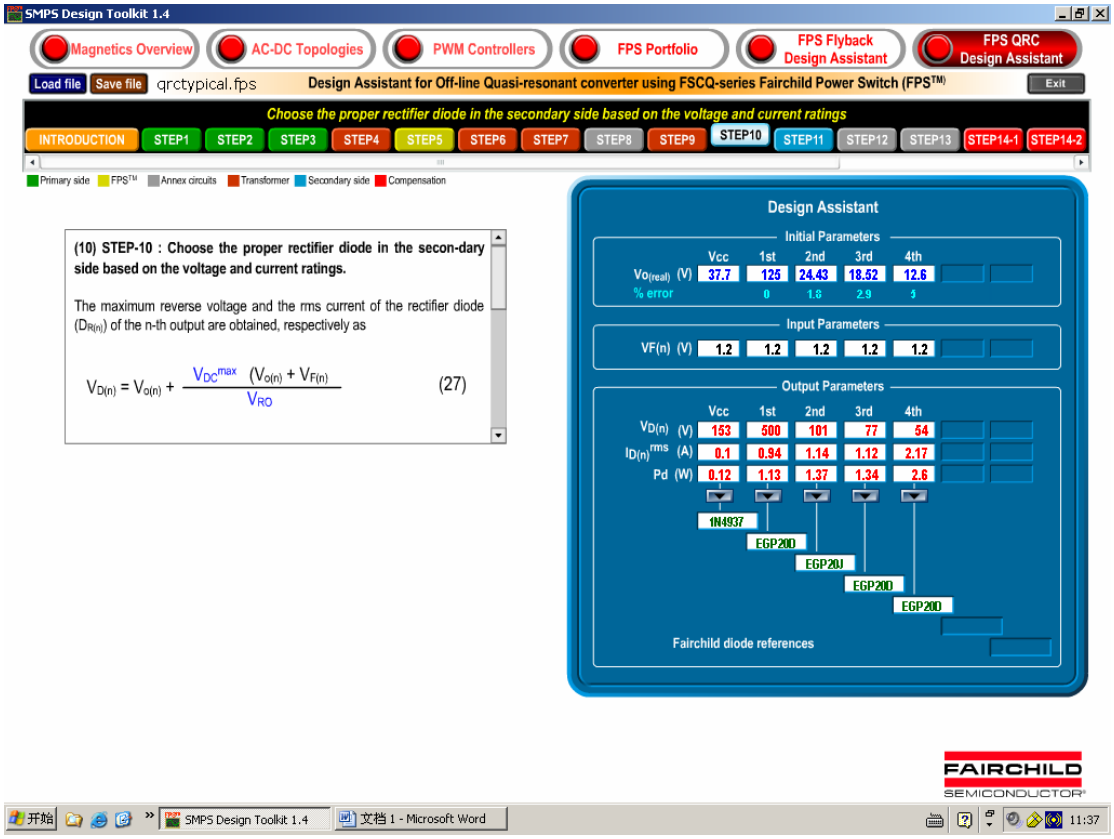
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Choose the proper rectifier diode in the secondary side based on the voltage and current ratings
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Primary side
FPS™
Annex circuits
Transformer
Secondary side
Compensation
(10) STEP-10 : Choose the proper rectifier diode in the secon-dary side based on the voltage and current ratings.
The maximum reverse voltage and the rms current of the rectifier diode ($D_{R(n)}$) of the n-th output are obtained, respectively as
(27)
Design Assistant
Initial Parameters
Vcc
1st
2nd
3rd
4th
Vo(real) (V)
37.7
125
24.43
18.52
12.6
% error
0
1.8
2.9
5
Input Parameters
VF(n) (V)
1.2
1.2
1.2
1.2
1.2
Output Parameters
VD(n) (V)
153
500
101
77
54
ID(n)rms (A)
0.1
0.94
1.14
1.12
2.17
Pd (W)
0.12
1.13
1.37
1.34
2.6
1N4937
EGP20D
EGP20J
EGP20G
EGP20D
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Determine the output capacitor considering the voltage and current ripple.

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Primary side | FPS™ | Annex circuits | Transformer | Secondary side | Compensation

(11) STEP-11 : Determine the output capacitor considering the voltage and current ripple.

The ripple current of the n-th output capacitor ($C_{o(n)}$) is obtained as

$$I_{cap(n)}^{rms} = \sqrt{(I_{D(n)}^{rms})^2 - I_{o(n)}^2} \qquad (31)$$

where $I_{o(n)}$ is the load current of the n-th output and $I_{D(n)}^{rms}$ is specified in

Design Assistant

Input Parameters

(Output Voltage)	125	24	18	12
	1st	2nd	3rd	4th
Output Capacitor(μF)	100	1000	1000	1000
ESR Output Capacitor(mΩ)	100	100	100	100

Output Parameters

	1st	2nd	3rd	4th
Capacitor ripple current (A)	0.85	1.02	1	1.93
Capacitor ripple voltage(V)	0.33	0.3	0.3	0.58
Capacitor ripple voltage(%)	0.3	1.2	1.7	4.8

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Design the synchronization network

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Primary side | FPS™ | Annex circuits | Transformer | Secondary side | Compensation

(12) STEP-12 : Design the synchronization network.

FSCQ-series employs a Quasi-resonant switching technique to minimize the switching noise and loss. In this technique, a capacitor (C_r) is added between the MOSFET drain and source as shown in Figure 12. The basic waveforms of a Quasi-resonant converter are shown in Figure 13. The external capacitor lowers the rising slope of drain voltage and therefore reduces the EMI caused by the MOSFET turn-off. In order to minimize the MOS-FET switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value as shown in Figure 13.

Design Assistant

Input Parameters

V_{sync}^{pk} 9 V (4.6 < V_{sync}^{pk} < 12V (Vovp))

R_{sy1} 1.5 KΩ

Output Parameters

R_{sy2} 0.47 KΩ

Output Capacitance (Cr) 0.94 nF

Sync capacitor (C_{sy}) 3.94 nF

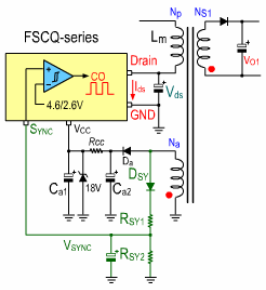

Figure 12. Synchronization circuit

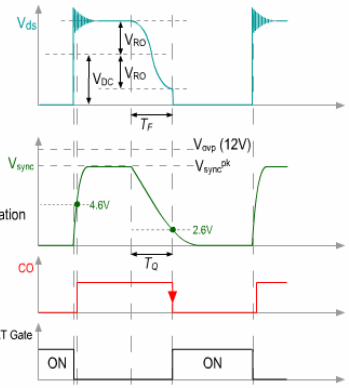

Figure 13. Synchronization waveforms

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Design voltage drop for the burst operation

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Primary side | FPS™ | Annex circuits | Transformer | Secondary side | Compensation

(13) STEP-13 : Design voltage drop circuit for the burst operation.

In order to minimize the power consumption in the standby mode, FSCQ-series employs burst operation. Once FPS enters into burst mode, all the output voltages and effective switching frequencies are reduced. Figure 14 shows the typical output voltage drop circuit for C-TV applications.
Under normal operation, the picture on signal is applied and the transistor Q_1 is turned on, which de-couples R_3 , D_Z and D_1 from the feedback network. Therefore, only V_{o1} is regulated by the feedback circuit in normal operation and is determined as

Design Assistant

Initial Parameters: V_{O2} in standby mode (V_{O2}^{stby}) 8 V

Output Parameters: Zener breakdown voltage, D_Z 5 V

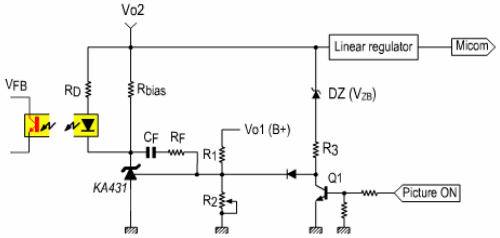

Figure 14. Typical feedback circuit to drop output voltage in standby mode

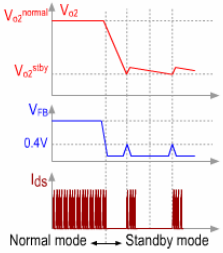

Figure 15. burst operation waveforms

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Design the Reference shunt / Opto-coupler DC supply

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Primary side | FPS™ | Annex circuits | Transformer | Secondary side | Compensation

When determining the feedback circuit component, there are some restrictions as follows.

(a) The voltage divider network of R 1 and R 2 should be designed to provide 2.5V to the reference pin of the KA431.
The relationship between R 1 and R 2 is given as

$$R2 = \frac{2.5\ R1}{Vo1 - 2.5} \qquad (37\text{-}1)$$

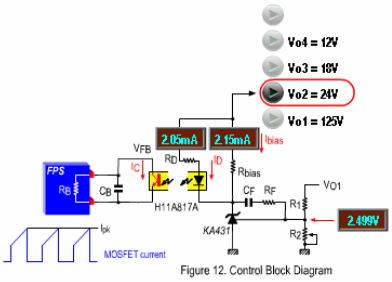


Figure 12. Control Block Diagram

Design Assistant

Input Parameters

Opto coupler resistor RD 10 KΩ | KA431 bias resistor Rbias 10 KΩ

Voltage divider resistors R1 100 KΩ, R2 2.04 KΩ | Feedback resistor RF 39 KΩ

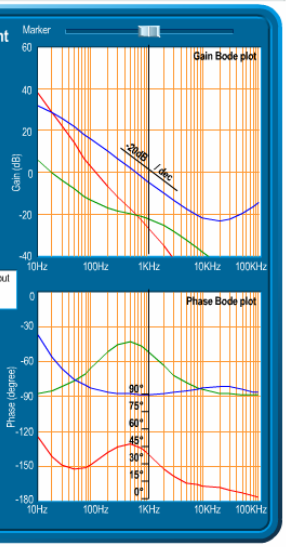
Feedback pin capacitor CB 47 nF

Feedback capacitor CF 22 nF

Control to output
Compensator
Compensated

Output Parameters

Control-to-ouput DC gain	49.94
Control-to-output zero	15915 Hz
Control-to-output RHP zero	21639 Hz
Control-to-output pole	13 Hz
Feedback integrator gain (fi)	20 Hz
Feedback zero (fz)	185 Hz
Feedback pole (fp)	1209 Hz



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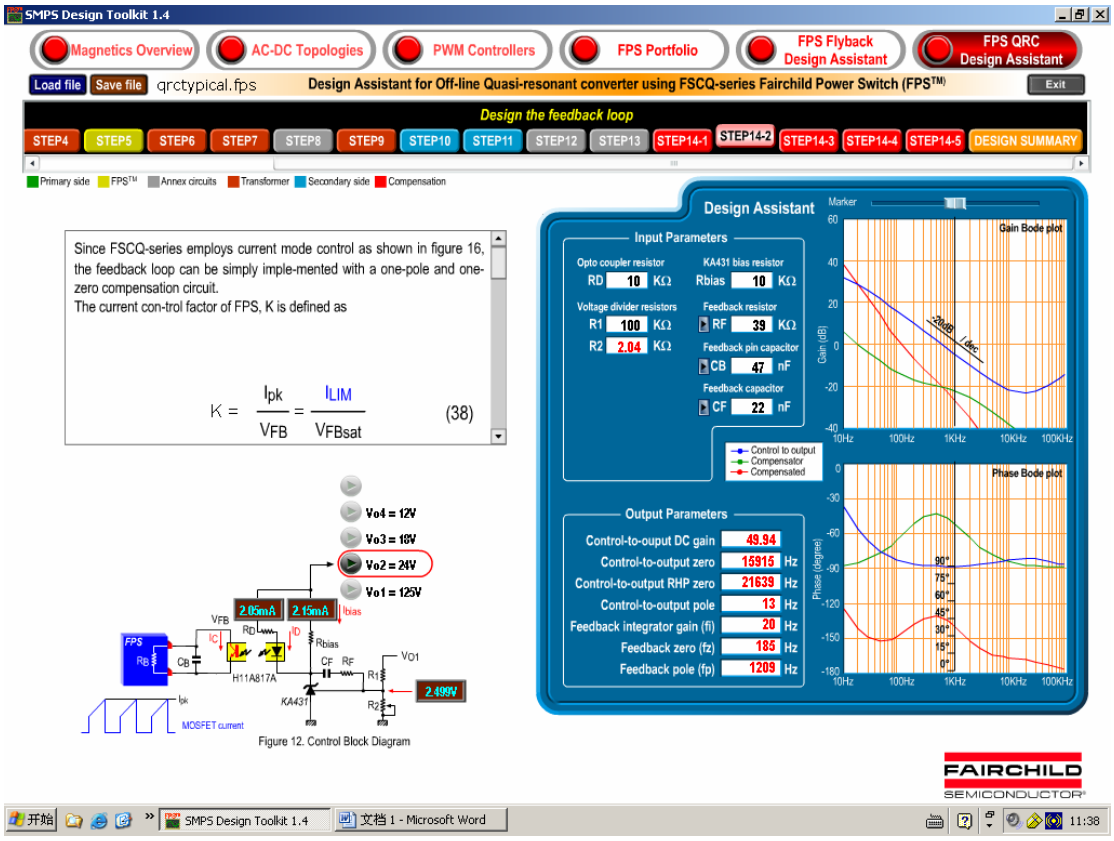

Figure 12. Control Block Diagram

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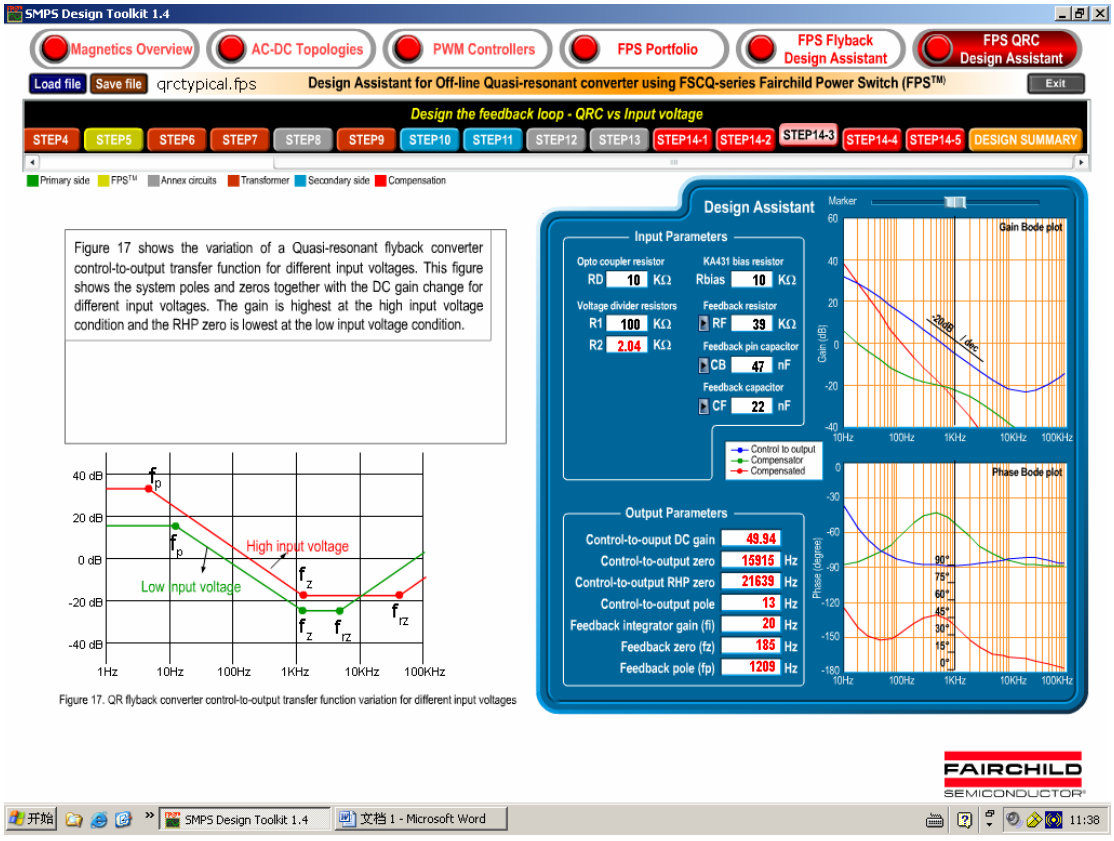

Figure 17. QR flyback converter control-to-output transfer function variation for different input voltages

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Magnetics Overview | AC-DC Topologies | PWM Controllers | FPS Portfolio | FPS Flyback Design Assistant | FPS QRC Design Assistant

Load file | Save file | qrctypical.fps | Design Assistant for Off-line Quasi-resonant converter using FSCQ-series Fairchild Power Switch (FPS™) | Exit

Design the feedback loop - QRC vs Load

STEP4 | STEP5 | STEP6 | STEP7 | STEP8 | STEP9 | STEP10 | STEP11 | STEP12 | STEP13 | STEP14-1 | STEP14-2 | STEP14-3 | STEP14-4 | STEP14-5 | DESIGN SUMMARY

Primary side | FPS™ | Annex circuits | Transformer | Secondary side | Compensation

Figure 18 shows the variation of a Quasi-resonant flyback converter control-to-output transfer function for different loads. This figure shows that the gain between f_p and f_z does not change for different loads and the RHP zero is lowest at the full load condition.

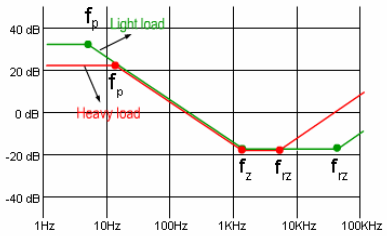


Figure 18. QR flyback converter control-to-output transfer function variation for different loads

Design Assistant

Input Parameters

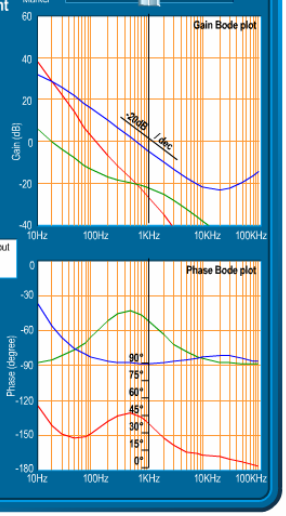
Opto coupler resistor RD 10 KΩ | KA431 bias resistor Rbias 10 KΩ

Voltage divider resistors R1 100 KΩ, R2 2.04 KΩ | Feedback resistor RF 39 KΩ | Feedback pin capacitor CB 47 nF | Feedback capacitor CF 22 nF

Control to output | Compensator | Compensated

Output Parameters

Control-to-ouput DC gain	49.94
Control-to-output zero	15915 Hz
Control-to-output RHP zero	21639 Hz
Control-to-output pole	13 Hz
Feedback integrator gain (fi)	20 Hz
Feedback zero (fz)	185 Hz
Feedback pole (fp)	1209 Hz



FAIRCHILD SEMICONDUCTOR

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SMPS Design Toolkit 1.4

Magnetics Overview | AC-DC Topologies | PWM Controllers | FPS Portfolio | FPS Flyback Design Assistant | FPS QRC Design Assistant

Load file | Save file | qrctypical.fps | Design Assistant for Off-line Quasi-resonant converter using FSCQ-series Fairchild Power Switch (FPS™) | Exit

Feedback Compensation

STEP4 | STEP5 | STEP6 | STEP7 | STEP8 | STEP9 | STEP10 | STEP11 | STEP12 | STEP13 | STEP14-1 | STEP14-2 | STEP14-3 | STEP14-4 | STEP14-5 | DESIGN SUMMARY

Primary side | FPS™ | Annex circuits | Transformer | Secondary side | Compensation

The feedback compensation network transfer function of Figure 16 is obtained as

$$G_{VC} = \frac{\hat{V}_{FB}}{\hat{V}_{O1}} = -\frac{w_i}{s}\,\frac{(1+s/w_{ZC})}{1+1/w_{PC}} \qquad (40)$$

where

$$w_i = \frac{R_B}{R_1 R_D C_F} \qquad w_{ZC} = \frac{1}{(R_F + R_1) C_F} \qquad w_{PC} = \frac{1}{R_B C_B}$$

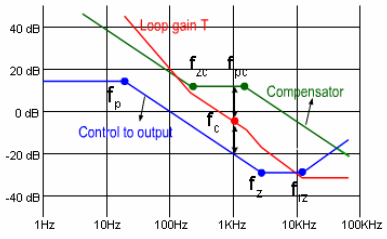


Figure 19. Compensator design

Design Assistant

Input Parameters

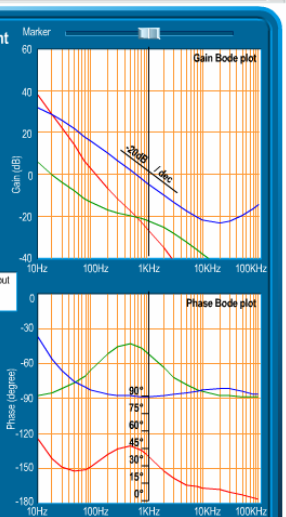
Opto coupler resistor RD 10 KΩ | KA431 bias resistor Rbias 10 KΩ

Voltage divider resistors R1 100 KΩ, R2 2.04 KΩ | Feedback resistor RF 39 KΩ | Feedback pin capacitor CB 47 nF | Feedback capacitor CF 22 nF

Control to output | Compensator | Compensated

Output Parameters

Control-to-ouput DC gain	49.94
Control-to-output zero	15915 Hz
Control-to-output RHP zero	21639 Hz
Control-to-output pole	13 Hz
Feedback integrator gain (fi)	20 Hz
Feedback zero (fz)	185 Hz
Feedback pole (fp)	1209 Hz



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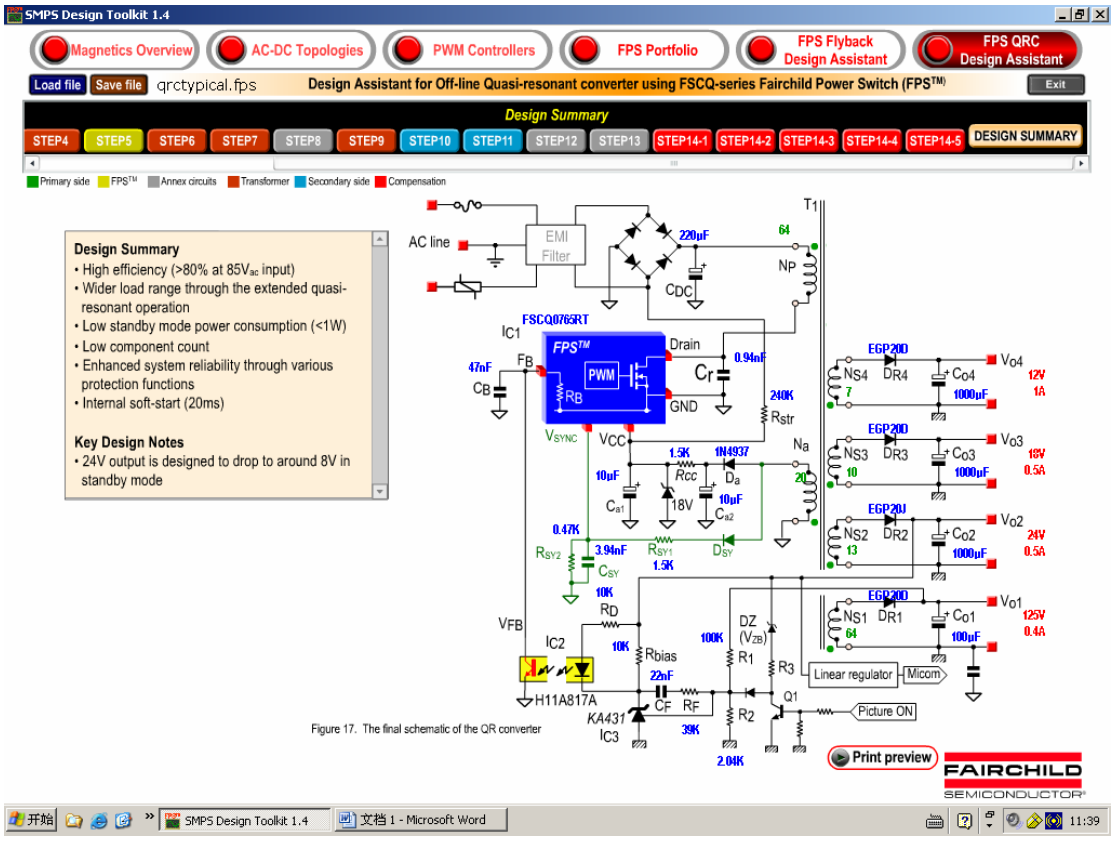

Figure 17. The final schematic of the QR converter