

SMP5 Design Toolkit 1.4

Magnetics Overview AC-DC Topologies PWM Controllers FPS Portfolio **FPS Flyback Design Assistant** FPS QRC Design Assistant

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Define the system specification

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Primary side FPS™ Annex circuits Transformer Secondary side Compensation

(1) STEP-1 : Define the system specifications

- Line voltage range (V_{line}^{min} and V_{line}^{max}).
- Line frequency (f.).
- Maximum output power (P_o).
- Estimated efficiency (E_r) : It is required to estimate the power conversion efficiency in order to calculate the maximum input power. If no reference data is available, set $E_r = 0.7-0.75$ for low voltage output applications and $E_r = 0.8-0.85$ for high voltage output applications. In the case of Color TV applications, the typical efficiency is 80-83%.
With the estimated efficiency, the maximum input power is given by

Design Assistant

Input Parameters

Minimum Line voltage (V_{line}^{min}) **85** V Line Frequency **60** Hz
 Maximum Line voltage (V_{line}^{max}) **265** V Estimated efficiency **82** %

1 output	1st	2nd	3rd	4th		
2 outputs						
3 outputs						
4 outputs	Vo(V)	125	24	18	12	
5 outputs						
6 outputs	Io(A)	0.4	0.5	0.5	1	

Output Parameters

	1st	2nd	3rd	4th		
Po(W)	50	12	9	12		
KLo(%)	60	14	11	14		

Maximum output power (P_o) **83** W Maximum Input power (P_{in}) **101** W

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Determine DC link capacitor (C_{DC}) and the DC link voltage range.

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(2) STEP-2 : Determine DC link capacitor (CDC) and the DC link voltage range.

It is typical to select the DC link capacitor as 2-3uF per watt of input power for universal input range (85-265Vrms) and 1uF per watt of input power for European input range (195V-265Vrms). With the DC link capacitor chosen, the minimum DC link voltage is obtained as

$$V_{DC}^{min} = \sqrt{2(V_{line}^{min})^2 - \frac{P_{in}}{1-D_{ch}}} \quad (3)$$

DC link voltage

DC link voltage ripple

$D_{ch} = T_1 / T_2 = 0.2 - 0.25$

Figure 3. DC Link Voltage Wawefrom

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Input Parameters

DC link Capacitor (C_{DC}) **220** μF

Output Parameters

Minimum DC link voltage (V_{DC}^{min}) **91** V
 Maximum DC link voltage (V_{DC}^{max}) **375** V
 Maximum DC link voltage ripple **29** V

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Determine the reflected output voltage (V_{RO})

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(3) STEP-3 : Determine the reflected output voltage (V_{RO})

Figure 4 shows the typical waveforms of the drain voltage of Quasi-resonant flyback converter. When the MOSFET is turned off, the DC link voltage (V_{DC}) together with the output voltage reflected to the primary (V_{RO}) are imposed on the MOSFET and the maximum nominal voltage across MOSFET (V_{ds}^{nom}) is given as

$$V_{ds}^{nom} = V_{dc}^{max} + V_{RO} \quad (5)$$

Figure 4. The typical waveform of MOSFET drain voltage

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Input Parameters

Output voltage reflected to primary (V_{RO}) **126**

Output Parameters

Maximum nominal MOSFET voltage (V_{ds}^{nom}) **501**

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Determine the transformer primary inductance (L_m)

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Primary side FPS™ Annex circuits Transformer Secondary side Compensation

(4) STEP-4 : Determine the transformer primary side inductance (L_m)

Figure 5 shows the typical waveforms of MOSFET drain current, secondary diode current and the MOSFET drain voltage of a Quasi-resonant converter. During T_{OFF} , the current flows through the secondary side rectifier diode and the MOSFET drain voltage is clamped at ($V_{DC} + V_{RO}$). When the secondary side current reduces to zero, the drain voltage begins to drop by the resonance between the effective output capacitor of the MOSFET and the primary side inductance (L_m). In order to minimize the switching loss, the FSCQ-series is designed to turn on the MOSFET when the drain voltage reaches its minimum voltage.

Figure 5. Typical waveforms of Quasi-resonant converter

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Input Parameters

Minimum Switching frequency (f_s^{min}) **24** KHz

Drain voltage falling time(T_F) **2.3** μ S

Output Parameters

Maximum Duty cycle (D_{max}) **0.55**

Primary side inductance (L_m) **514** μ H

Maximum peak drain current (I_{ds}^{peak}) **4.05** A

RMS drain current (I_{ds}^{rms}) **1.73** A

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Choose the proper FPS considering input power and peak drain current

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(5) STEP-5 : Choose the proper FPS considering input power and peak drain current.

With the resulting maximum peak drain current of the MOSFET ($I_{ds,peak}$) from equation (7), choose the proper FPS whose the pulse-by-pulse current limit level (I_{LIM}) is higher than $I_{ds,peak}$. Since FPS has +12%

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Initial Parameters
Maximum peak drain current ($I_{ds,peak}$) 4.05 A

Input Parameters
FPS™ Reference **FSCQ0765RT** Typical current limit (LIM) 5 A

Output Parameters
Minimum LIM considering tolerance of 12% 4.4 A

ACDC DCDC Application Flyback Forward Quasi-Resonant

Green HV-FET Rating (V) Peak Limit (A) 65-265Vdc 230Vdc Pin max(w) open frame Switching Frequency (kHz) Rds(on) max (V) Over Load Over Current Over Voltage Thermal SOFT Start Protection Mode selected devices 4

Device	Green Mode	HV-FET Rating (V)	Peak Limit (A)	65-265Vdc	230Vdc	Pin max(w) open frame	Switching Frequency (kHz)	Rds(on) max (V)	Over Load	Over Current	Over Voltage	Thermal SOFT Start	Protection Mode	selected devices
FSCQ0765RT	Y	650	5	100	130	ORC	1.6	A/R	Latch	A/R	Latch	Y	TO220F-5I	4
FSCQ1265RT	Y	650	7	170	200	ORC	0.9	A/R	Latch	A/R	Latch	Y	TO220F-5I	
FSCQ1565RP	Y	650	11.5	250	300	ORC	0.65	A/R	Latch	A/R	Latch	Y	TO3PF-7I	
FSCQ1565RT	Y	650	8	200	230	ORC	0.65	A/R	Latch	A/R	Latch	Y	TO220F-5I	

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Determine the proper core and the minimum primary turns

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Primary side FPS™ Annex circuits Transformer Secondary side Compensation

(6) STEP-6 : Determine the proper core and the minimum primary turns.

Table 2 shows the commonly used cores for C-TV application for different output powers. With the chosen core, the minimum number of turns for the transformer primary side to avoid the core saturation in normal operation is given by

$$N_p^{min} = \frac{L_m I_{ds,peak}}{\Delta B A_e} \cdot 10^6 \quad (\text{turns}) \quad (10)$$

Figure 6. Window area and cross sectional area

Table2. Core quick selection table

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Input Parameters
Saturation flux density (Bsat) 0.38 T Max flux density swing (ΔB) 0.30 T

Output Parameters
Cross sectional area of core (A_e) 109 mm²
Minimum primary turns (N_p^{min}) 64 t

EE EI EER EPC Specific Core Enter your parameters

Core Al (nH.T²) Ae Aw
EER35 2400 109 235.6
Selected window area

Figure 7. Typical B-H characteristics of ferrite core TDK PC40

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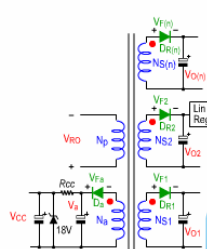
Determine the number of turns for each output.

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(7) STEP-7 : Determine the number of turns for each output and Vcc auxiliary circuit

Figure 8 shows the simplified diagram of the transformer. It is assumed that V_{o1} is the reference output that is regulated by the feedback control in normal operation. It is also assumed that linear regulator is connected to V_{o2} to supply a stable voltage for MCU. First, calculate the turns ratio (n) between the primary winding and reference output (V_{o1}) winding as a reference.



Products	V _{RRM} (V)	I _F (A)	V _F (V)	T _{rr} (nS)	Package
UF4001	50	1	1	50	DO-41
UF4002	100	1	1	50	DO-41
UF4003	200	1	1	50	DO-41
UF4004	400	1	1	50	DO-41
UF4005	600	1	1.7	50	DO-41
UF4006	800	1	1.7	50	DO-41

Ultra Fast Recovery Diode

Table2. Fairchild diode quick selection table

Stby mode

V_{o2}stby 8 V Kdrop 0.365

V_astby 13 V

Vcc drop resistor calculations

I_{op} 6 mA I_{cc} 9 mA at fs 90 KHz

C_{ISS} 1840 pF R_{CC} 1.5 KΩ must be < 2.19K

V_Z 18 V P_a 259 mW

Design Assistant

Initial Parameters

Minimum primary turns (N_p^{min}) 64

Outputs V_o(n) V 125 24 18 12

Outputs I_o(n) A 0.4 0.5 0.5 1

Input Parameters

diode D_a 1st 2nd 3rd 4th

V_F(n) V 1.2 1.2 1.2 1.2

Choose # of turns for 1st output 64

Output Parameters

(Individual Windings option)

Ungapped AL value (AL) 2400 nH/T²

of turns t 1st 2nd 3rd 4th

V_a normal v 37.7 125 24.43 18.52 12.6

% error 0 1.8 2.9 5

Gap length (G); center pole gap 1.034 mm Primary turns (N_p) 64 t

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Determine the startup resistor

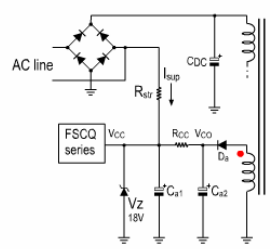
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Primary side FPS™ Annex circuits Transformer Secondary side Compensation

(8) STEP-8 : Determine the startup resistor

Figure 11 shows the typical circuit of Vcc winding for FSCQ-series. Initially, FPS consumes only startup current (max 50uA) before it begins switching. Therefore, the current supplied through the startup resistor (R_{st}) can charge the capacitors C_{a1} and C_{a2} while supplying startup current to FPS. When V_{cc} reaches start voltage of 15V (V_{START}), FPS begins switching, and the current consumed by FPS increases. Then, the current required by FPS is supplied from the transformer auxiliary winding.

Startup resistor (R_{st}) : The average of the minimum current supplied



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Input Parameters

Maximum startup current of FPS (I_{st}) 50 μA

Startup resistor (R_{st}) (must be < 620K) 240 KΩ

Effective Vcc capacitor (C_e) 20 μF

Output Parameters

Maximum dissipation in startup resistor 132 mW (at V_{line}^{max} = 263V)

Maximum startup time (T_{str}^{max}) 3.8 S (at V_{line}^{min} = 69V)

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Determine the wire Ø for each winding based on the rms current of each output

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Primary side FPS™ Annex circuits Transformer Secondary side Compensation

(9) STEP-9 : Determine the wire diameter for each winding based on the RMS current of each output.

The RMS current of the n-th secondary winding is obtained as

$$I_{sec(n)}^{rms} = I_{ds}^{rms} \sqrt{\frac{1 - D_{max}}{D_{max}}} \cdot \frac{V_{RO} \cdot K_{L(n)}}{(V_{o(n)} + V_{F(n)})} \quad (25)$$

EE EI EER EPC Specific Core Enter your parameters

Core Al (nH.T²) Ae Aw
EER35 2400 109 **235.6**

Selected window area

Design Assistant

Initial Parameters

	Primary	Vcc	Outputs Vo(n)	1st	2nd	3rd	4th
V (V)	37.7	125	24	18	12		
# of turns(t)	64	20	64	13	10	7	

Input Parameters

	Primary Winding	Vcc	1st	2nd	3rd	4th
Wire Ø(mm)	0.6	0.3	0.5	0.4	0.4	0.5
Strands	1	1	1	2	2	2

Fill factor (Kf) **0.2**

Output Parameters

	Primary Winding	Vcc	1st	2nd	3rd	4th
Id(n) rms A	1.73	0.1	0.94	1.14	1.12	2.17
A/mm²	6.12	1.41	4.79	4.54	4.46	5.53
Cu area	18.1	1.41	12.57	3.27	2.51	2.75
Copper area (Ac)	40.61 mm²		Required window area (Awr) 203 mm²			

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Choose the proper rectifier diode in the secondary side based on the voltage and current ratings

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Primary side FPS™ Annex circuits Transformer Secondary side Compensation

(10) STEP-10 : Choose the proper rectifier diode in the secondary side based on the voltage and current ratings.

The maximum reverse voltage and the rms current of the rectifier diode (D_{R(n)}) of the n-th output are obtained, respectively as

$$V_{D(n)} = V_{o(n)} + \frac{V_{DC}^{max}}{V_{RO}} (V_{o(n)} + V_{F(n)}) \quad (27)$$

Design Assistant

Initial Parameters

	Vcc	1st	2nd	3rd	4th
V _{o(reat)} (V)	37.7	125	24.43	18.52	12.6
% error	0	1.8	2.9	3	

Input Parameters

	VF(n) (V)	1st	2nd	3rd	4th
	1.2	1.2	1.2	1.2	1.2

Output Parameters

	Vcc	1st	2nd	3rd	4th
V _{D(n)} (V)	153	500	101	77	54
I _{D(n)} rms (A)	0.1	0.94	1.14	1.12	2.17
Pd (W)	0.12	1.13	1.37	1.34	2.6

1N4937 EGP200 EGP200 EGP200 EGP200

Fairchild diode references

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Determine the output capacitor considering the voltage and current ripple.

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Primary side FPS™ Annex circuits Transformer Secondary side Compensation

(11) STEP-11 : Determine the output capacitor considering the voltage and current ripple.

The ripple current of the n-th output capacitor ($C_{cap(n)}$) is obtained as

$$I_{cap(n)}^{rms} = \sqrt{(I_{o(n)}^{rms})^2 - I_{o(n)}^2} \quad (31)$$

where $I_{o(n)}$ is the load current of the n-th output and $I_{o(n)}^{rms}$ is specified in

Design Assistant

Input Parameters

(Output Voltage)	1st	2nd	3rd	4th
125	24	18	12	
Output Capacitor(μ F)	100	1000	1000	1000
ESR Output Capacitor(ms)	100	100	100	100

Output Parameters

	1st	2nd	3rd	4th
Capacitor ripple current (A)	0.85	1.02	1	1.93
Capacitor ripple voltage(V)	0.33	0.3	0.3	0.58
Capacitor ripple voltage(%)	0.3	1.2	1.7	4.8

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Design the synchronization network

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Primary side FPS™ Annex circuits Transformer Secondary side Compensation

(12) STEP-12 : Design the synchronization network.

FSCQ-series employs a Quasi-resonant switching technique to minimize the switching noise and loss. In this technique, a capacitor (C_s) is added between the MOSFET drain and source as shown in Figure 12. The basic waveforms of a Quasi-resonant converter are shown in Figure 13. The external capacitor lowers the rising slope of drain voltage and therefore reduces the EMI caused by the MOSFET turn-off. In order to minimize the MOS-FET switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value as shown in Figure 13.

Figure 12. Synchronization circuit

Figure 13. Synchronization waveforms

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Input Parameters

V_{sync_pk} 9 V $4.6 < V_{sync_pk} < 12V (V_{ovp})$

R_{sy1} 1.5 K Ω

Output Parameters

R_{sy2} 0.47 K Ω

Output Capacitance (C_r) 0.94 nF

Sync capacitor (C_{sy}) 3.94 nF

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Design voltage drop for the burst operation

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(13) STEP-13 : Design voltage drop circuit for the burst operation.

In order to minimize the power consumption in the standby mode, FSCQ-series employs burst operation. Once FPS enters into burst mode, all the output voltages and effective switching frequencies are reduced. Figure 14 shows the typical output voltage drop circuit for C-TV applications. Under normal operation, the picture on signal is applied and the transistor Q₁ is turned on, which de-couples R₃, D_z and D₁ from the feedback network. Therefore, only V_{o1} is regulated by the feedback circuit in normal operation and is determined as

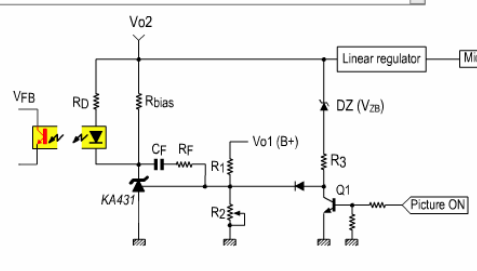


Figure 14. Typical feedback circuit to drop output voltage in standby mode

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Initial Parameters: V_{o2} In standby mode (V_{o2^{stby}}) 8 V

Output Parameters: Zener breakdown voltage, D_z 5 V

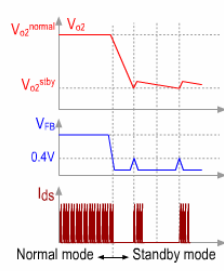


Figure 15. burst operation waveforms

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Design the Reference shunt / Opto-coupler DC supply

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Primary side FPS™ Annex circuits Transformer Secondary side Compensation

When determining the feedback circuit component, there are some restrictions as follows.

(a) The voltage divider network of R₁ and R₂ should be designed to provide 2.5V to the reference pin of the KA431. The relationship between R₁ and R₂ is given as

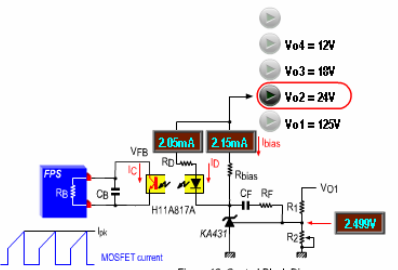
$$R_2 = \frac{2.5 R_1}{V_{o1} - 2.5} \quad (37-1)$$


Figure 12. Control Block Diagram

Design Assistant

Input Parameters

Opto coupler resistor RD 10 KΩ KA431 bias resistor Rbias 10 KΩ

Voltage divider resistors R1 100 KΩ Feedback resistor RF 39 KΩ

R2 2.04 KΩ Feedback pin capacitor CB 47 nF

Feedback capacitor CF 22 nF

Output Parameters

Control-to-output DC gain 49.34

Control-to-output zero 15915 Hz

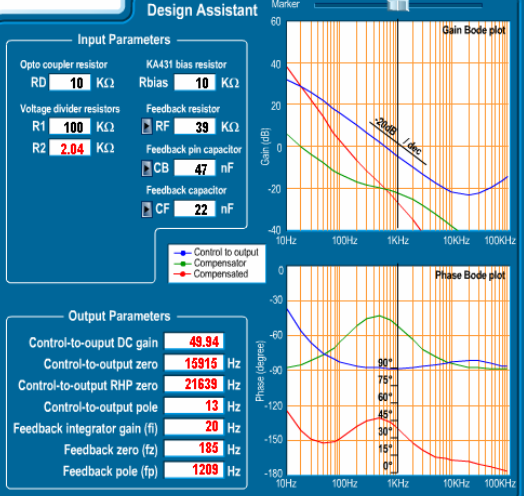
Control-to-output RHP zero 21639 Hz

Control-to-output pole 13 Hz

Feedback integrator gain (fi) 20

Feedback zero (fz) 185 Hz

Feedback pole (fp) 1209 Hz



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Design the feedback loop

STEP4 STEP5 STEP6 STEP7 STEP8 STEP9 STEP10 STEP11 STEP12 STEP13 STEP14-1 STEP14-2 STEP14-3 STEP14-4 STEP14-5 DESIGN SUMMARY

Primary side FPS™ Annex circuits Transformer Secondary side Compensation

Since FSCQ-series employs current mode control as shown in figure 16, the feedback loop can be simply implemented with a one-pole and one-zero compensation circuit. The current control factor of FPS, K is defined as

$$K = \frac{I_{pk}}{V_{FB}} = \frac{I_{LIM}}{V_{FBsat}} \quad (38)$$

Figure 12. Control Block Diagram

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Input Parameters

Opto coupler resistor RD 10 KΩ KA431 bias resistor Rbias 10 KΩ

Voltage divider resistors R1 100 KΩ Feedback resistor RF 39 KΩ

R2 2.04 KΩ Feedback pin capacitor CB 47 nF

Feedback capacitor CF 22 nF

Output Parameters

Control-to-output DC gain 49.34

Control-to-output zero 15915 Hz

Control-to-output RHP zero 21639 Hz

Control-to-output pole 13 Hz

Feedback integrator gain (fi) 20 Hz

Feedback zero (fz) 185 Hz

Feedback pole (fp) 1209 Hz

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SMPS Design Toolkit 1.4

Magnetics Overview AC-DC Topologies PWM Controllers FPS Portfolio FPS Flyback Design Assistant FPS QRC Design Assistant

Load file Save file qrcotypical.fps Design Assistant for Off-line Quasi-resonant converter using FSCQ-series Fairchild Power Switch (FPS™)

Design the feedback loop - QRC vs Input voltage

STEP4 STEP5 STEP6 STEP7 STEP8 STEP9 STEP10 STEP11 STEP12 STEP13 STEP14-1 STEP14-2 STEP14-3 STEP14-4 STEP14-5 DESIGN SUMMARY

Primary side FPS™ Annex circuits Transformer Secondary side Compensation

Figure 17 shows the variation of a Quasi-resonant flyback converter control-to-output transfer function for different input voltages. This figure shows the system poles and zeros together with the DC gain change for different input voltages. The gain is highest at the high input voltage condition and the RHP zero is lowest at the low input voltage condition.

Design Assistant

Input Parameters

Opto coupler resistor RD 10 KΩ KA431 bias resistor Rbias 10 KΩ

Voltage divider resistors R1 100 KΩ Feedback resistor RF 39 KΩ

R2 2.04 KΩ Feedback pin capacitor CB 47 nF

Feedback capacitor CF 22 nF

Output Parameters

Control-to-output DC gain 49.34

Control-to-output zero 15915 Hz

Control-to-output RHP zero 21639 Hz

Control-to-output pole 13 Hz

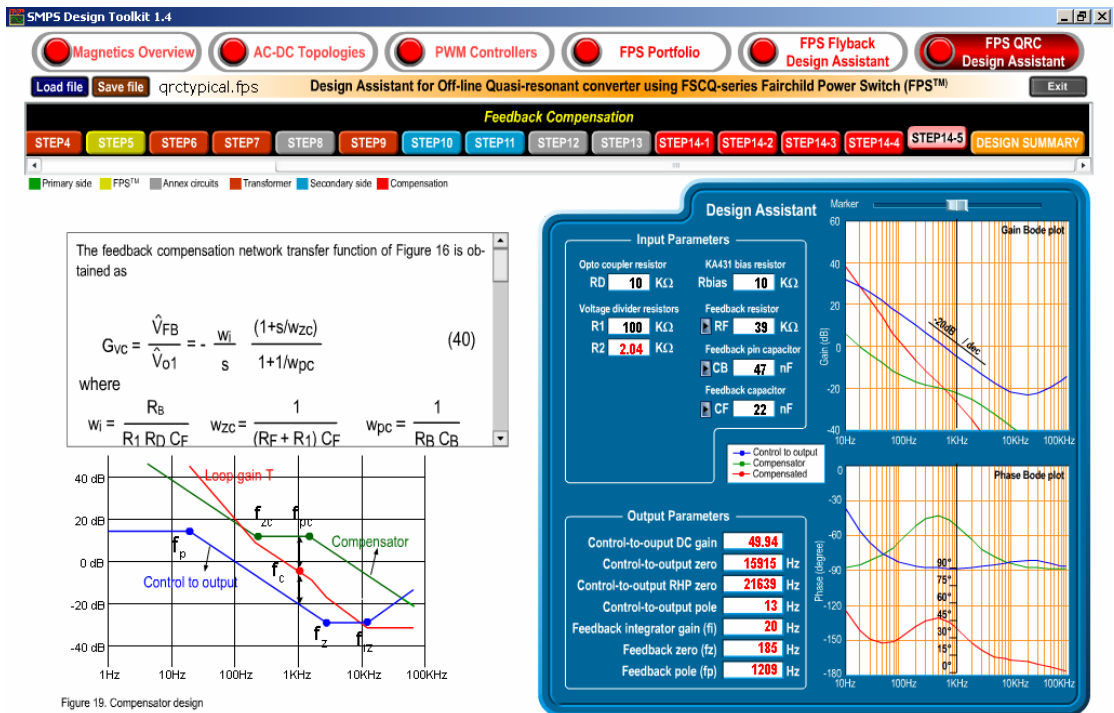
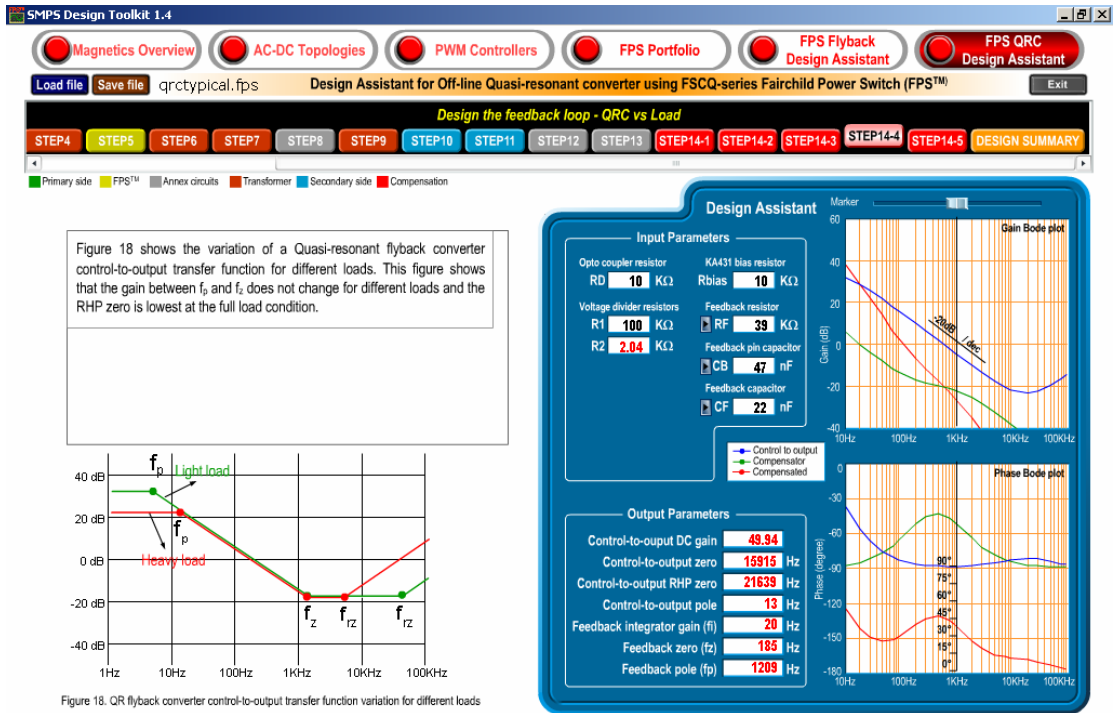
Feedback integrator gain (fi) 20 Hz

Feedback zero (fz) 185 Hz

Feedback pole (fp) 1209 Hz

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Design Summary

- High efficiency (>80% at 85V_{ac} input)
- Wider load range through the extended quasi-resonant operation
- Low standby mode power consumption (<1W)
- Low component count
- Enhanced system reliability through various protection functions
- Internal soft-start (20ms)

Key Design Notes

- 24V output is designed to drop to around 8V in standby mode

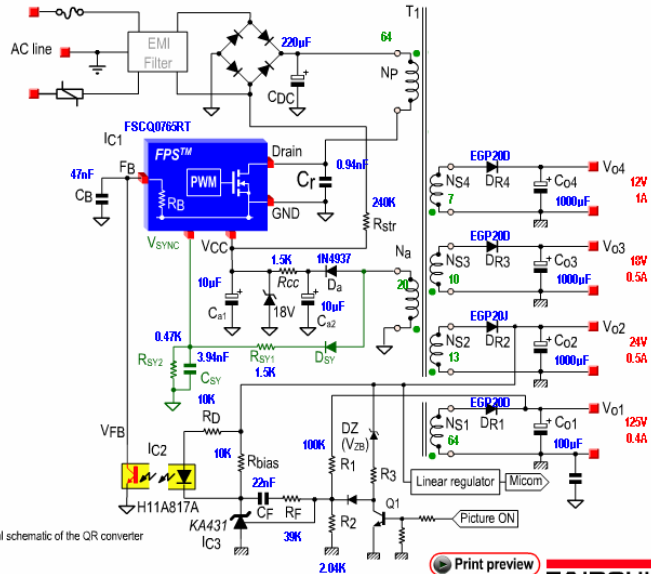


Figure 17. The final schematic of the QR converter