BATTERY PROTECTION IC for SINGLE-CELL PACK

S-8261 Series

The S-8261 series are lithium-ion/lithium polymer rechargeable battery protection ICs incorporating high-accuracy voltage detection circuit and delay circuit.
The S-8261 series are suitable for protection of single-cell lithium ion/lithium polymer battery packs from overcharge, overdischarge and overcurrent.

■ Features

(1) Internal high accuracy voltage detection circuit

- Overcharge detection voltage 3.9V to 4.4V (applicable in 5mV step)
  Accuracy : ±25mV (+25°C) and ±30mV (-5°C to +55°C)
- Overcharge hysteresis voltage 0.0V to 0.4V (*1) Accuracy : ±25mV

The overcharge hysteresis voltage can be selected from the range 0.0V to 0.4V in 50mV step.
*1: Overcharge release voltage = Overcharge detection voltage - Overcharge hysteresis voltage
(where overcharge release voltage<3.8V is prohibited.)

- Overdischarge detection voltage 2.0V to 3.0 V (10mV step) Accuracy : ±50mV
- Overdischarge hysteresis voltage 0.0V to 0.7 V (*2) Accuracy : ±50mV

The overdischarge hysteresis voltage can be selected from the range 0.0V to 0.7V in 100mV step.
*2: Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(where overdischarge release voltage>3.4V is prohibited.)

- Overcurrent 1 detection voltage 0.05V to 0.3V (10mV step) Accuracy : ±15mV
- Overcurrent 2 detection voltage 0. 5V (fixed) Accuracy : ±100mV

(2) High voltage device is used for charger connection pins
VM and CO pins: absolute maximum rating = 28V

(3) Delay times (overcharge: t_{CU}, overdischarge: t_{DL}, overcurrent 1: t_{IOV1}, overcurrent 2: t_{IOV2}) are generated by an internal circuit. No external capacitor is necessary. Accuracy : ±20%

(4) Three-step overcurrent detection circuit is included. (overcurrent 1, overcurrent 2, and load short-circuiting)

(5) Either charge function or charge inhibition function for 0V battery can be selected.

(6) Charger detection function and abnormal charge current detection function

- The overdischarge hysteresis is released by detecting negative voltage at the VM pin (-0.7V typ.). (Charger detection function)
- When the output voltage of the DO pin is high and the voltage at the VM pin is equal to or lower than the charger detection voltage (-0.7V typ.), the output voltage of the CO pin goes low. (Abnormal charge current detection function)

(7) Low current consumption

- Operation 3.5 μA typ. 7.0 μA max.
- Power-down 0.1 μA max.

(8) Wide operating temperature range: -40°C to +85°C

(9) Small package SOT-23-6 (6-pin) SNB(B) (6-pin)

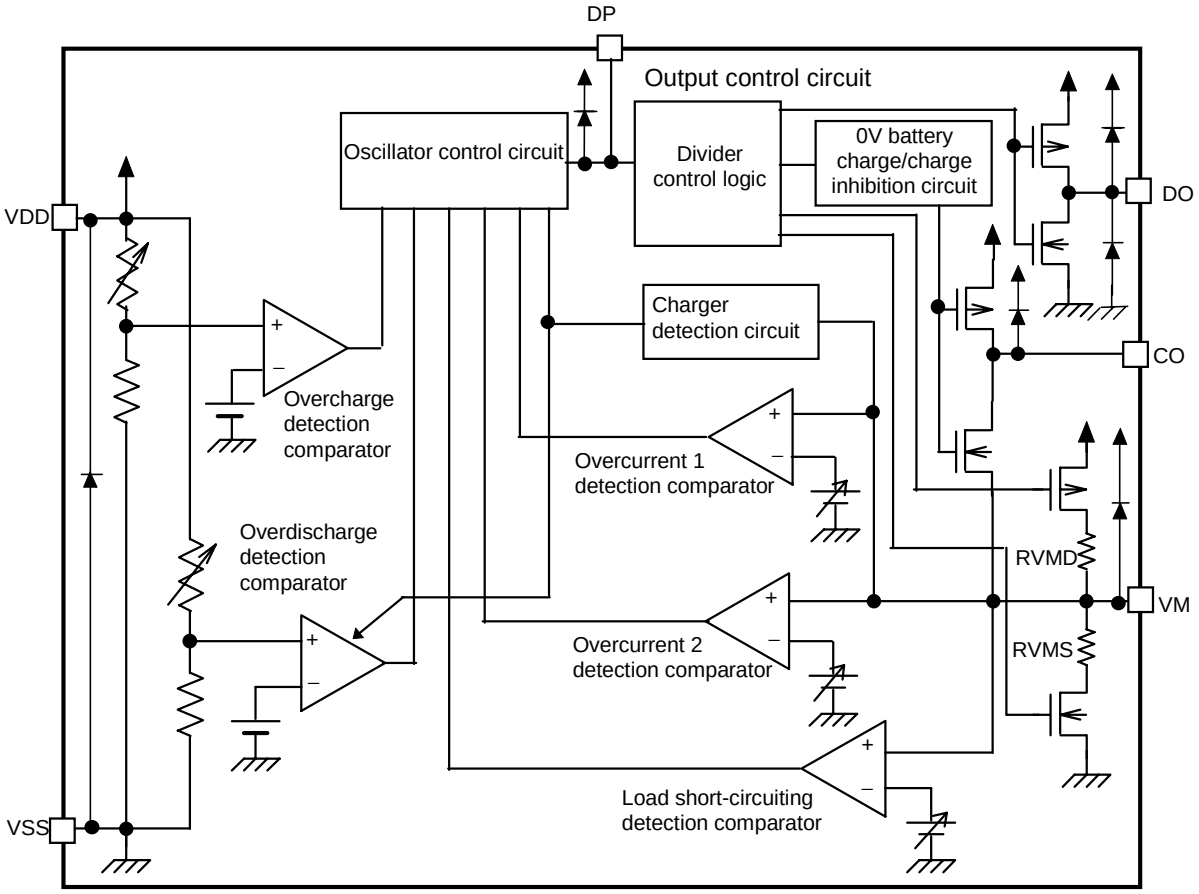
■ Applications

- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

■ Package

- 6-Pin SOT-23-6 (PKG drawing code : MP006-A)
- 6-Pin SNB(B) (PKG drawing code : BD006-A)

■ Block Diagram



Note: Diodes in the figure are parasitic diodes.

Figure 1 Block Diagram

■ Selection Guide

Naming of product model number

Model number: S-8261Axxyy – abbreviation code (3 letters) –zz

Symbol	Meaning	Description
xx	Serial code	Assigned from AA to ZZ in alphabetical order.
yy	Package form	MD:SOT-23-6 BD:SNB
zz	Tape direction	T2:SOT-23-6 TF:SNB

Model No.	Over-charge detection voltage	Over-charge release voltage	Over-discharge detection voltage	Over-discharge release voltage	Over-current 1 detection voltage	0V battery charge function
S-8261AAGMD-G2G -T2	4.28 V	0.2 V	2.3 V	2.3 V	0.16 V	Yes
S-8261AAHMD-G2H -T2	4.28 V	0.2 V	2.3 V	2.3 V	0.08 V	Yes
S-8261AAJMD-G2J -T2	4.325V	0.25V	2.5V	0.4V	0.15V	None

Model No.	Over-charge detection delay time	Over-discharge detection delay time	Over-current 1 detection delay time
S-8261AAGMD-G2G -T2	1.2 s	144 ms	9 ms
S-8261AAHMD-G2H -T2	1.2 s	144 ms	9 ms
S-8261AAJMD-G2J -T2	1.2 s	144 ms	9 ms

It is possible to change the detection voltages of the product other than above. The delay times can also be changed within the range listed bellow. For details, please contact our sales office.

Delay time	Symbol	Selection range			Remarks
Overcharge detection delay time	t_{CU}	0.15 s	**1.2 s**	4.6 s	Choose from the left.
Overdischarge detection delay time	t_{DL}	36 ms	**144 ms**	290 ms	Choose from the left.
Overcurrent 1 detection delay time	t_{IOV1}	4.5 ms	**9 ms**	18 ms	Choose from the left.

* Values surrounded by bold lines are used in standard products.

■ Pin Assignment

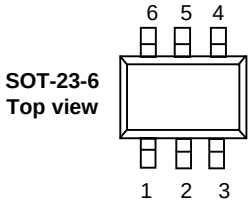


Figure 2

Pin No.	Symbol	Description
1	DO	FET gate control pin for discharge (CMOS output)
2	VM	Voltage detection pin between VM and VSS (Overcurrent detection pin)
3	CO	FET gate control pin for charge (CMOS output)
4	DP	Test pin for delay time measurement
5	VDD	Positive power input pin
6	VSS	Negative power input pin

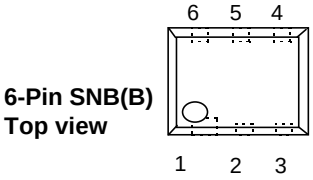


Figure 3

Pin No.	Symbol	Description
1	CO	FET gate control pin for charge (CMOS output)
2	VM	Voltage detection pin between VM and VSS (Overcurrent detection pin)
3	DO	FET gate control pin for discharge (CMOS output)
4	VSS	Negative power input pin
5	DP	Test pin for delay time measurement
6	VDD	Positive power input pin

■ Absolute Maximum Ratings

(Ta = 25°C unless otherwise specified)

Parameter		Symbol	Applied pin	Rating	Unit
Input voltage between VDD and VSS *		V_{DS}	VDD	V_{SS} -0.3 to V_{SS} +12	V
Input pin voltage for VM		V_{VM}	VM	V_{DD} -28 to V_{DD} +0.3	V
Output pin voltage for CO		V_{CO}	CO	V_M -0.3 to V_{DD} +0.3	V
Output pin voltage for DO		V_{DO}	DO	V_{SS} -0.3 to V_{DD} +0.3	V
Power dissipation	SOT-23-6	P_D	—	250	mW
	SNB(B)	P_D	—	90	mW
Operating temperature range		T_{opr}	—	-40 to +85	°C
Storage temperature range		T_{stg}	—	-55 to +125	°C

Note: Aithough the IC contains protection circuit against static electricity, excessive static electricity or voltage which exceeds the limit of the protection circuit should not be applied to.

* Do not apply pulse-like noise of μs order exceeding the above input voltage (V_{SS} + 12 V). The noise causes damage to the IC.

■ Electrical Characteristics (1) Except detection delay time (25°C)

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Remark	Min.	Typ.	Max.	Unit	Measure-ment circuit
DETECTION VOLTAGE								
Overcharge detection voltage V_{CU}=3.9V to 4.4V 5mV Step	V_{CU}	1	–	V_{CU} -0.025	V_{CU}	V_{CU} +0.025	V	1
			Ta= -5°C to 55°C(*1)	V_{CU} -0.030	V_{CU}	V_{CU} +0.030		
Overcharge hysteresis voltage V_{HC}=0.0V to 0.4V 50mV Step	V_{HC}	1	–	V_{HC} -0.025	V_{HC}	V_{HC} +0.025	V	1
Overdischarge detection voltage V_{DL}=2.0V to 3.0V 10mV Step	V_{DL}	2	–	V_{DL} -0.050	V_{DL}	V_{DL} +0.050	V	2
Overdischarge hysteresis voltage V_{HD}=0.0V to 0.7V 100mV Step	V_{HD}	2	–	V_{HD} -0.050	V_{HD}	V_{HD} +0.050	V	2
Overcurrent 1 detection voltage V_{IOV1}=0.05V to 0.3V 10mV Step	V_{IOV1}	3	–	V_{IOV1} -0.015	V_{IOV1}	V_{IOV1} +0.015	V	2
Overcurrent 2 detection voltage	V_{IOV2}	3	–	0.4	0.5	0.6	V	2
Load short-circuiting detection voltage	V_{SHORT}	3	–	0.9	1.2	1.5	V	2
Charger detection voltage	V_{CHA}	4	–	-1.0	-0.7	-0.4	V	2
INPUT VOLTAGE, OPERATION VOLTAGE								
Operation voltage between VDD and VSS	V_{DSOP1}	–	Internal circuit operating voltage	1.5	–	8	V	–
Operation voltage between VDD and VM	V_{DSOP2}	–	Internal circuit operating voltage	1.5	–	28	V	–
CURRENT CONSUMPTION								
Current consumption in normal operation	I_{OPE}	5	V_{DD}=3.5V, V_M=0V	1.0	3.5	7.0	µA	2
Current consumption at power down	I_{PDN}	5	V_{DD}=V_M =1.5V	–	–	0.1	µA	2
OUTPUT RESISTANCE								
CO pin H resistance	R_{COH}	7	V_{CO}=3.0V,V_{DD}=3.5V,V_M=0V	2.5	5	10	kΩ	4
CO pin L resistance	R_{COL}	7	V_{CO}=0.5V,V_{DD}=4.5V,V_M=0V	2.5	5	10	kΩ	4
DO pin H resistance	R_{DOH}	8	V_{DO}=3.0V,V_{DD}=3.5V,V_M=0V	2.5	5	10	kΩ	4
DO pin L resistance	R_{DOL}	8	V_{DO}=0.5V,V_{DD}=V_M=1.8V	2.5	5	10	kΩ	4
VM INTERNAL RESISTANCE								
Internal resistance between VM and VDD	R_{VMD}	6	V_{DD}=1.8V, V_M =0V	100	300	900	kΩ	3
Internal resistance between VM and VSS	R_{VMS}	6	V_{DD}= 3.5V, V_M =1.0V	10	20	40	kΩ	3
0V BATTERY CHARGING FUNCTION								
0V battery charge starting charger voltage	V_{0CHA}	11	Applied for 0V battery charge function	1.2	–	–	V	2
0V battery charge inhibition battery voltage	V_{0INH}	12	Applied for 0V battery charge inhibition function	–	–	0.5	V	2

(*1) : Since products are not screened at low and high temperature, the specification for this temperature range is guaranteened by design, not tested in production.

■ Electrical Characteristics (2) Except detection delay time (–40 to 85°C*1)

(Ta = –40 to 85°C*1 unless otherwise specified)

Parameter	Symbol	Condition	Remark	Min.	Typ.	Max.	Unit	Measure-ment circuit
DETECTION VOLTAGE								
Overcharge detection voltage V_{CU}=3.9V to 4.4V 5mV Step	V_{CU}	1	–	V_{CU} -0.055	V_{CU}	V_{CU} +0.040	V	1
Overcharge hysteresis voltage V_{HC}=0.0V to 0.4V 50mV Step	V_{HC}	1	–	V_{HC} -0.025	V_{HC}	V_{HC} +0.025	V	1
Overdischarge detection voltage V_{DL}=2.0V to 3.0V 10mV Step	V_{DL}	2	–	V_{DL} -0.080	V_{DL}	V_{DL} +0.080	V	2
Overdischarge hysteresis voltage V_{HD} =0.0V to 0.7V 100mV Step	V_{HD}	2	–	V_{HD} -0.050	V_{HD}	V_{HD} +0.050	V	2
Overcurrent 1 detection voltage V_{IOV1}=0.05V to 0.3V 10mV Step	V_{IOV1}	3	–	V_{IOV1} -0.021	V_{IOV1}	V_{IOV1} +0.021	V	2
Overcurrent 2 detection voltage	V_{IOV2}	3	–	0.37	0.5	0.63	V	2
Load short-circuiting detection voltage	V_{SHORT}	3	–	0.7	1.2	1.7	V	2
Charger detection voltage	V_{CHA}	4	–	-1.2	-0.7	-0.2	V	2
INPUT VOLTAGE, OPERATION VOLTAGE								
Operation voltage between VDD and VSS	V_{DSOP1}	–	Internal circuit operating voltage	1.5	–	8	V	–
Operation voltage between VDD and VM	V_{DSOP2}	–	Internal circuit operating voltage	1.5	–	28	V	–
CURRENT CONSUMPTION								
Current consumption in normal operation	I_{OPE}	5	V_{DD}=3.5V, V_M=0V	0.7	3.5	8.0	µA	2
Current consumption at power down	I_{PDN}	5	V_{DD}=V_M =1.5V	–	–	0.1	µA	2
OUTPUT RESISTANCE								
CO pin H resistance	R_{COH}	7	V_{CO}=3.0V,V_{DD}=3.5V,V_M=0V	1.2	5	15	kΩ	4
CO pin L resistance	R_{COL}	7	V_{CO}=0.5V,V_{DD}=4.5V,V_M=0V	1.2	5	15	kΩ	4
DO pin H resistance	R_{DOH}	8	V_{DO}=3.0V,V_{DD}=3.5V,V_M=0V	1.2	5	15	kΩ	4
DO pin L resistance	R_{DOL}	8	V_{DO}=0.5V,V_{DD}=V_M=1.8V	1.2	5	15	kΩ	4
VM INTERNAL RESISTANCE								
Internal resistance between VM and VDD	R_{VMD}	6	V_{DD}=1.8V, V_M=0V	78	300	1310	kΩ	3
Internal resistance between VM and VSS	R_{VMS}	6	V_{DD}=3.5V, V_M=1.0V	7.2	20	44	kΩ	3
0V BATTERY CHARGING FUNCTION								
0V battery charge starting charger voltage	V_{0CHA}	11	Applied for 0V battery charge function	1.7	–	–	V	2
0V battery charge inhibition battery voltage	V_{0INH}	12	Applied for 0V battery charge inhibition function	–	–	0.3	V	2

(*1) : Since products are not screened at low and high temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Electrical Characteristics (3) Detection delay time (25°C)

S-8261AAG, S-8261AAH, S-8261AAJ

Parameter	Symbol	Condition	Remark	Min.	Typ.	Max.	Unit	Measure-ment circuit
DELAY TIME								
Overcharge detection delay time	t_{CU}	9	–	0.96	1.2	1.4	s	5
Overdischarge detection delay time	t_{DL}	9	–	115	144	173	ms	5
Overcurrent 1 detection delay time	t_{IOV1}	10	–	7.2	9	11	ms	5
Overcurrent 2 detection delay time	t_{IOV2}	10	–	1.8	2.24	2.7	ms	5
Load short-circuiting detection delay time	t_{SHORT}	10	–	220	320	380	µs	5

■ Electrical Characteristics (4) Detection delay time (–40 to 85°C*1)

S-8261AAG, S-8261AAH, S-8261AAJ

Parameter	Symbol	Condition	Remark	Min.	Typ.	Max.	Unit	Measure-ment circuit
DELAY TIME								
Overcharge detection delay time	t_{CU}	9	–	0.7	1.2	2.0	s	5
Overdischarge detection delay time	t_{DL}	9	–	80	144	245	ms	5
Overcurrent 1 detection delay time	t_{IOV1}	10	–	5	9	15	ms	5
Overcurrent 2 detection delay time	t_{IOV2}	10	–	1.2	2.24	3.8	ms	5
Load short-circuiting detection delay time	t_{SHORT}	10	–	150	320	540	µs	5

(*1) : Since products are not screened at low and high temperature, the specification for this temperature range is guaranteened by design.

■ Measurement Circuits

Unless otherwise specified, the output voltage levels ″H″ and ″L″ at CO and DO pins are judged by the threshold voltage (1.0 V) of the N channel FET. Judge the CO pin level with respect to V_M and the DO pin level with respect to V_{SS}.

(1) Measurement Condition 1, Measurement Circuit 1

〈〈 Overcharge detection voltage, Overcharge hysteresis voltage〉〉

The overcharge detection voltage (V_{CU}) is defined by the voltage between VDD and VSS at which V_{CO} goes ″L″ from ″H″ when the voltage V1 is gradually increased from the starting condition V1=3.5V and V2=0V. The overcharge hysteresis voltage (V_{HC}) is then defined by the difference between the overcharge detection voltage (V_{CU}) and the voltage between VDD and VSS at which V_{CO} goes ″H″ from ″L″ when the voltage V1 is gradually decreased.

(2) Measurement Condition 2, Measurement Circuit 2

〈〈Overdischarge detection voltage, Overdischarge hysteresis voltage〉〉

The overdischarge detection voltage (V_{DL}) is defined by the voltage between VDD and VSS at which V_{DO} goes ″L″ from ″H″ when the voltage V1 is gradually decreased from the starting condition V1=3.5V and V2=0V. The overdischarge hysteresis voltage (V_{HD}) is then defined by the difference between the overdischarge detection voltage (V_{DL}) and the voltage between VDD and VSS at which V_{DO} goes ″H″ from ″L″ when the voltage V1 is gradually increased.

(3) Measurement Condition 3, Measurement Circuit 2

〈〈 Overcurrent 1 detection voltage, Overcurrent 2 detection voltage, Load short-circuiting detection voltage 〉〉

The overcurrent 1 detection voltage is defined by the voltage between VM and VSS whose delay time for changing V_{DO} from ″H″ to ″L″ lies between the minimum and the maximum value of the overcurrent 1 detection delay time when the voltage V2 is increased rapidly within 10µs from the starting condition V1=3.5V and V2=0V.

The overcurrent 2 detection voltage is defined by the voltage between VM and VSS whose delay time for changing V_{DO} from ″H″ to ″L″ lies between the minimum and the maximum value of the overcurrent 2 detection delay time when the voltage V2 is increased rapidly within 10µs from the starting condition V1=3.5V and V2=0V.

The load short-circuiting detection voltage is defined by the voltage between VM and VSS whose delay time for changing V_{DO} from ″H″ to ″L″ lies between the minimum and the maximum value of the load short-circuiting detection delay time when the voltage V2 is increased rapidly within 10µs from the starting condition V1=3.5V and V2=0V.

(4) Measurement Condition 4, Measurement Circuit 2

〈〈 Charger detection voltage, abnormal charge current detection voltage 〉〉

Set V1=1.8V and V2=0V. Increase V1 gradually until $V1=V_{DL}+(V_{HD}/2)$, then decrease V2 from 0 V gradually. The voltage between VM and VSS when V_{DO} goes ″H″ from ″L″ is the charger detection voltage (V_{CHA}). Charger detection voltage can be measured only in the product whose overdischarge hysteresis $V_{HD} \neq 0$.

Set V1=3.5V and V2=0V. Decrease V2 from 0 V gradually. The voltage between VM and VSS when V_{CO} goes ″L″ from ″H″ is the abnormal charge current detection voltage. The abnormal charge current detection voltage has the same value as the charger detection voltage (V_{CHA}) .

(5) Measurement Condition 5, Measurement Circuit 2
〈〈 Normal operation current consumption, Power-down current consumption〉〉

Set V1=3.5V and V2=0V under normal condition. The current I_{DD} flowing through VDD pin is the normal operation consumption current (I_{OPE}).
Set V1=V2=1.5V under overdischarge condition. The current I_{DD} flowing through VDD pin is the power-down current consumption (I_{PDN}).

(6) Measurement Condition 6, Measurement Circuit 3
〈〈 Internal resistance between VM and VDD, Internal resistance between VM and VSS 〉〉

Set V1=1.8V and V2=0V. The resistance between VM and VDD is the internal resistance (R_{VMD}) between VM and VDD.
Set V1=3.5V and V2=1.0V. The resistance between VM and VSS is the internal resistance (R_{VMS}) between VM and VSS

(7) Measurement Condition 7, Measurement Circuit 4
〈〈 CO pin H resistance, CO pin L resistance 〉〉

Set V1=3.5V, V2=0V and V3=3.0V. CO pin resistance is the CO pin H resistance (R_{COH}).
Set V1=4.5V, V2=0V and V3=0.5V. CO pin resistance is the CO pin L resistance (R_{COL}).

(8) Measurement Condition 8, Measurement Circuit 4
〈〈 DO pin H resistance, DO pin L resistance 〉〉

Set V1=3.5V, V2=0V and V4=3.0V. DO pin resistance is the DO pin H resistance (R_{DOH}).
Set V1=1.8V, V2=0V and V4=0.5V. DO pin resistance is the DO pin L resistance (R_{DOL}).

(9) Measurement Condition 9, Measurement Circuit 5
〈〈 Overcharge detection delay time, Overdischarge detection delay time 〉〉

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to change from "H" to "L" just after the V1 rapid increase within 10μs from the overcharge detection voltage (V_{CU}) - 0.2V to the overcharge detection voltage (V_{CU}) + 0.2V in the condition V2=0V.
The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to change from "H" to "L" just after the V1 rapid decrease within 10μs from the overdischarge detection voltage (V_{DL}) + 0.2V to the overdischarge detection voltage (V_{DL}) - 0.2V in the condition V2=0V.

(10) Measurement Condition 10, Measurement Circuit 5
〈〈 Overcurrent 1 detection delay time, Overcurrent 2 detection delay time, Load short-circuiting detection delay time, Abnormal charge current detection delay time 〉〉

Set V1=3.5V and V2=0V. Increase V2 from 0 V to 0.35 V momentarily (within 10 μs). The time needed for V_{DO} to go ″L″ is overcurrent 1 detection delay time (t_{IOV1}).
Set V1=3.5V and V2=0V. Increase V2 from 0 V to 0.7 V momentarily (within 10 μs). The time needed for V_{DO} to go ″L″ is overcurrent 2 detection delay time (t_{IOV2}).
Set V1=3.5V and V2=0V. Increase V2 from 0 V to 1.6 V momentarily (within 10 μs). The time needed for V_{DO} to go ″L″ is the load short-circuiting detection delay time (t_{SHORT}).
Set V1=3.5V and V2=0V. Decrease V2 from 0 V to -1.1 V momentarily (within 10 μs). The time needed for V_{CO} to go ″L″ is the abnormal charge current detection delay time. The abnormal charge current detection delay time has the same value as the overcharge detection delay time.

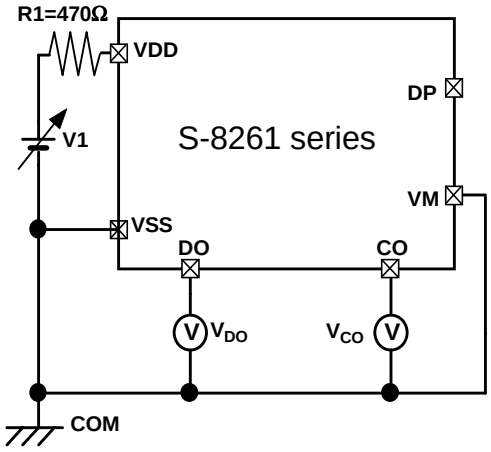
(11) Measurement Condition 11, Measurement Circuit 2 (Product with 0V battery charge function)
〈〈 0V battery charge starting charger voltage 〉〉

Set V1=V2=0V and decrease V2 gradually. The voltage between VDD and VM when V_{CO} goes "H" (V_M + 0.1 V or higher) is the 0V battery charge starting charger voltage (V_{0CHA}).

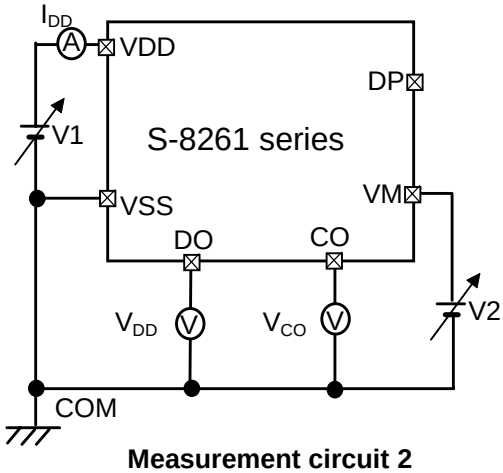
(12) Measurement Condition 12, Measurement Circuit 2 (Product with 0V battery charge inhibition function)

〈〈 0V battery charge inhibition battery voltage 〉〉

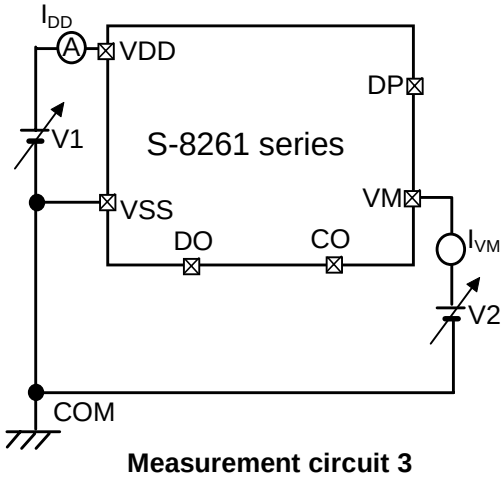
Set V1=0V and V2=-4V. Increase V1 gradually. The voltage between VDD and VSS when V_{CO} goes "H" (V_M + 0.1 V or higher) is the 0V battery charge inhibition battery voltage (V_{0INH}).



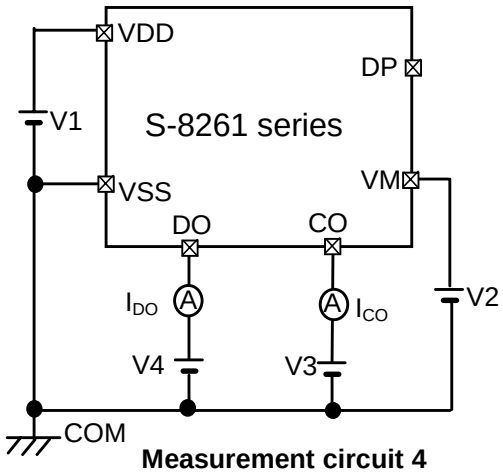
Mesurement circuit 1



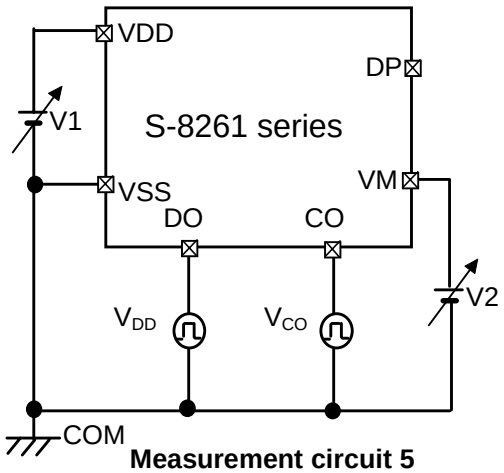
Measurement circuit 2



Measurement circuit 3



Measurement circuit 4



Measurement circuit 5

Fig. 4

■ Description of Operation

Normal condition

The S-8261 monitors the voltage of the battery connected between VDD and VSS pin and the voltage difference between VM and VSS pin to control charging and discharging. When the battery voltage is in the range from the overdischarge detection voltage (V_{DL}) to the overcharge detection voltage (V_{CU}), and the VM pin voltage is in the range from the charger detection voltage (V_{CHA}) to the overcurrent 1 detection voltage (V_{IOV1}), the IC turns both the charging and discharging control FETs on. This condition is called the normal condition, and in this condition charging and discharging can be carried out freely.

Note: When a battery is connected to the IC for the first time, the battery may not enter dischargeable state. In this case, set the VM pin voltage equal to the VSS voltage or connect a charger to enter the normal condition.

Overcurrent condition (Detection of Overcurrent 1, Overcurrent 2, and Load short-circuiting)

When the condition in which VM pin voltage is equal to or higher than the overcurrent detection voltage, condition which caused by the excess of discharging current over a specified value, continues longer than the overcharge detection delay time in a battery under the normal condition, the S-8261 turns the discharging control FET off to stop discharging. This condition is called the overcurrent condition.

Though the VM and VSS pins are shorted by the R_{VMS} resistor in the IC under the overcurrent condition, the VM pin voltage is pulled to the V_{DD} level by the load as long as the load is connected. The VM pin voltage returns to V_{SS} level when the load is released. The overcurrent condition returns to the normal condition when the impedance between the EB+ and EB- pin (see Figure 9) becomes higher than the automatic recoverable load resistance (see the equation [1] below), and the IC detects that the VM pin potential is lower than the overcurrent 1 detection voltage (V_{IOV1}).

Note: The automatic recoverable load resistance changes depending on the battery voltage and overcurrent 1 detection voltage settings.

Overcharge condition

When the battery voltage becomes higher than the overcharge detection voltage (V_{CU}) during charging under the normal condition and the detection continues for the overcharge detection delay time (t_{CU}) or longer, the S-8261 turns the charging control FET off to stop charging. This condition is called the overcharge condition.

The overcharge condition is released by the following two cases ((1) and (2)):

(1) When the battery voltage falls below the voltage difference, the overcharge detection voltage (V_{CL})– overcharge detection hysteresis voltage (V_{HC}), the S-8261 turns the charging control FET on and turns to the normal condition.

(2) When a load is connected and discharging starts, the S-8261 turns the charging control FET on and returns to the normal condition. The mechanism is : just after the load is connected and discharging starts, the discharging current flows through the parasitic diode in the charging control FET. At this moment VM pin potential increases momentarily V_f voltage of the parasitic diode from the VSS level. When the VM pin voltage goes higher than the overcurrent 1 detection voltage, and provided that the battery voltage goes under the overcharge detection voltage by the internal impedance, the S-8261 release the overcharge condition.

Note:

- If the battery is charged to a voltage higher than the overcharge detection voltage (V_{CU}) and the battery voltage does not fall below the overcharge detection voltage (V_{CU}) even when a heavy load is connected, the detection of overcurrent 1 ,overcurrent 2 and load short-circuiting does not work .Since an actual battery has the internal impedance of several dozens of mΩ, the battery voltage drops immediately after a heavy load which causes overcurrent is connected, and the detection of overcurrent 1, overcurrent 2 and load short-circuiting then works.

- When a charger is connected after the overcharge detection, the overcharge condition is not released even if the battery voltage is below the overcharge detection voltage V_{CL} . The overcharge condition is released when the VM pin voltage goes over the charger detection voltage V_{CHA} by removing the charger.

Overdischarge condition

When the battery voltage falls below the overdischarge detection voltage (V_{DL}) during discharging under the normal condition and the detection continues for the overdischarge detection delay time (t_{DL}) or longer, the S-8261 turns the discharging control FET off to stop discharging. This condition is called the overdischarge condition. When the discharging control FET turns off, the VM pin voltage is pulled up by the R_{VMD} resistor between VM and VDD in the IC. The voltage difference between VM and VDD then falls bellow 1.3V (typ.), the current consumption is reduced to the power-down current consumption (I_{PDN}). This condition is called the power-down condition.

The power-down condition is released when a charger is connected and the voltage difference between VM and VDD becomes 1.3 V (typ.) or higher. Moreover when the battery voltage becomes the overdischarge detection voltage (V_{DL}) or higher (see note), the S-8261 turns the discharging FET on and returns to the normal condition.

Charger detection

When a battery in the overdischarge condition is connected to a charger and provided that the VM pin voltage is lower than the charger detection voltage (V_{CHA}), the S-8261 releases the overdischarge condition and turns the discharging control FET on as the battery voltage becomes equal to or higher than the overdischarge detection voltage (V_{DL}) since the charger detection function works. This action is called charger detection.

When a battery in the overdischarge condition is connected to a charger and provided that the VM pin voltage is not lower than the charger detection voltage (V_{CHA}), the S-8261 releases the overdischarge condition when the battery voltage reaches the overdischarge detection voltage (V_{DL}) + overdischarge hysteresis (V_{HD}) or higher.

Abnormal charge current detection

If the VM pin voltage falls below the charger detection voltage (V_{CHA}) during charging under normal condition and it continues for the overcharge detection delay time (t_{CU}) or longer, the charging control FET turns off and charging stops. This action is called the abnormal charge current detection.

Abnormal charge current detection works when the DO pin voltage is “H” and the VM pin voltage falls below the charger detection voltage (V_{CHA}). Consequently, if an abnormal charge current flows to an over-discharged battery, the S-82611 turns the charging control FET off and stops charging after the battery voltage becomes higher than the overdischarge detection voltage which make the DO pin voltage “H”, and still after the overcharge detection delay time (t_{CU}) elapses.

Abnormal charge current detection is released when the voltage difference between VM pin and VSS pin becomes less than charger detection voltage V_{CHA}.

Delay circuits

The detection delay times are generated by dividing the approximate 3.5 kHz clock with a counter.

Note

- The detection delay time for overcurrent 2 and load and short-circuiting start when the overcurrent 1 is detected. As soon as the overcurrent 2 or load short-circuiting is detected over the detection delay time for overcurrent 2 or load short-circuiting after the detection of overcurrent 1, the S-8261 turns the discharging control FET off.

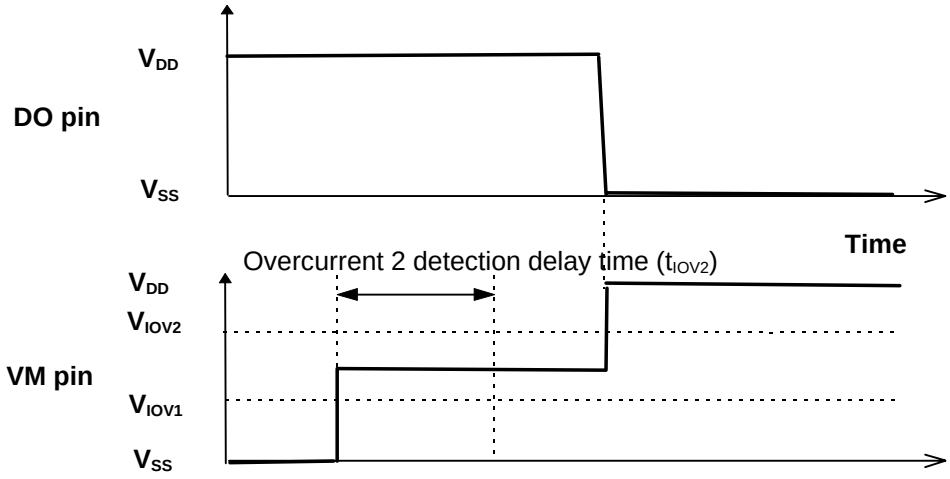


Figure 5

- When the overcurrent is detected and it continues for longer than the overdischarge detection delay time without releasing the load, the condition changes to the power-down condition when the battery voltage falls below the overdischarge detection voltage.
- When the battery voltage falls below the overdischarge detection voltage due to the overcurrent, the S-8261 turns the discharging control FET off by the overcurrent detection. And in this case the recovery of the battery voltage is so slow that the battery voltage after the overdischarge detection delay time is still lower than the overdischarge detection voltage, the S-8261 transits to the power-down condition.

DP pin

The DP pin is a test pin for delay time measurement and it should be open in the actual application. If a capacitor whose capacitance is larger than 100pF or a resister whose resistance is larger than 100kΩ is connected to this pin, error may occur in the delay time.

0V battery charge function (*1) (*2)

This function is used to recharge the connected battery whose voltage is 0V due to the self-discharge. When the 0V battery charge starting charger voltage (V_{0CHA}) or higher is applied between EB+ and EB- pins by connecting a charger, the charging control FET gate is fixed to VDD pin voltage. When the voltage between the gate and source of the charging control FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging control FET turns on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than the overdischarge release voltage V_{DU}, the S-8261 enters the normal condition.

0V battery charge inhibition function (*1)

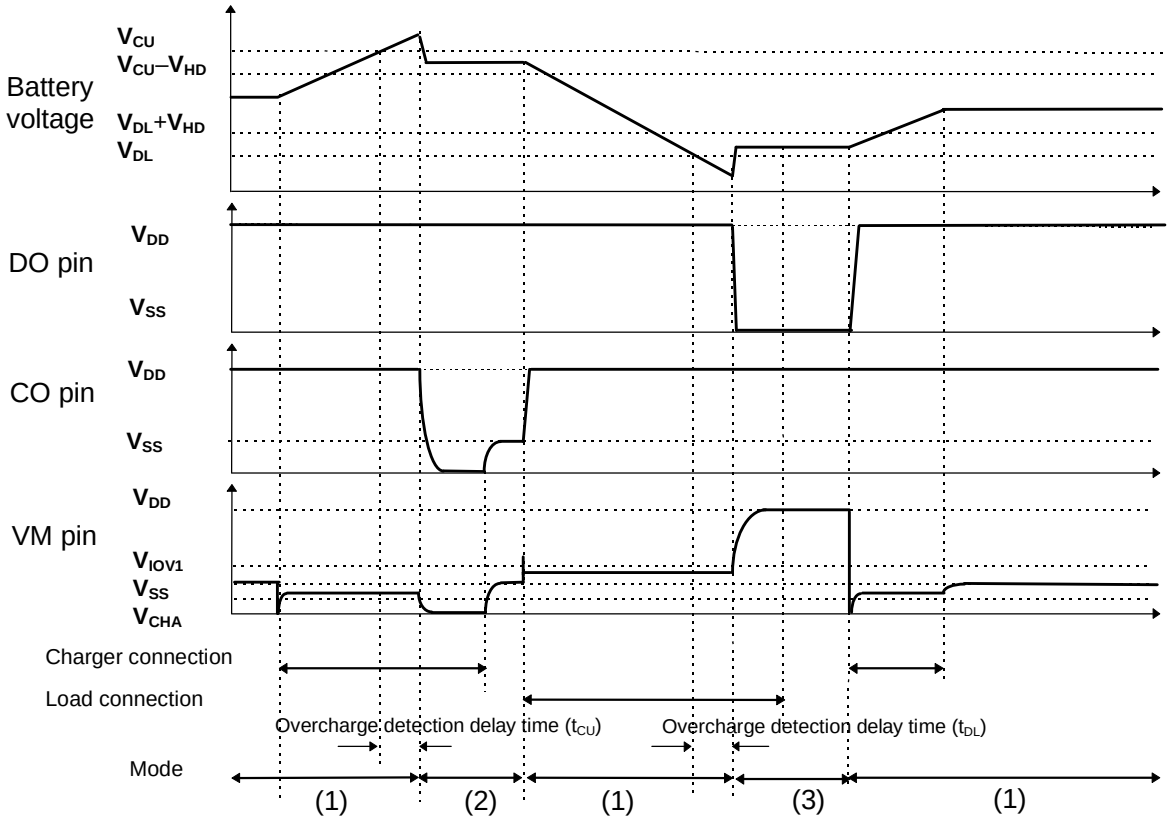
This function inhibits the recharging when a battery which is short-circuited (0 V) internally is connected. When the battery voltage is 0.6 V (typ.) or lower, the charging control FET gate is fixed to EB- pin voltage to inhibit charging. When the battery voltage is the 0V battery charge inhibition battery voltage (V_{0INH}) or higher, charging can be performed.

(*1) Some battery providers do not recommend charging for completely self-discharged battery. Please ask battery providers before determining the 0V battery charge function.

(*2) The 0V battery charge function has higher priority than the abnormal charge current detection function. Consequently, a product with the 0V battery charge function charges a battery forcedly and abnormal charge current cannot be detected when the battery voltage is low.

■ Operation Timing Chart

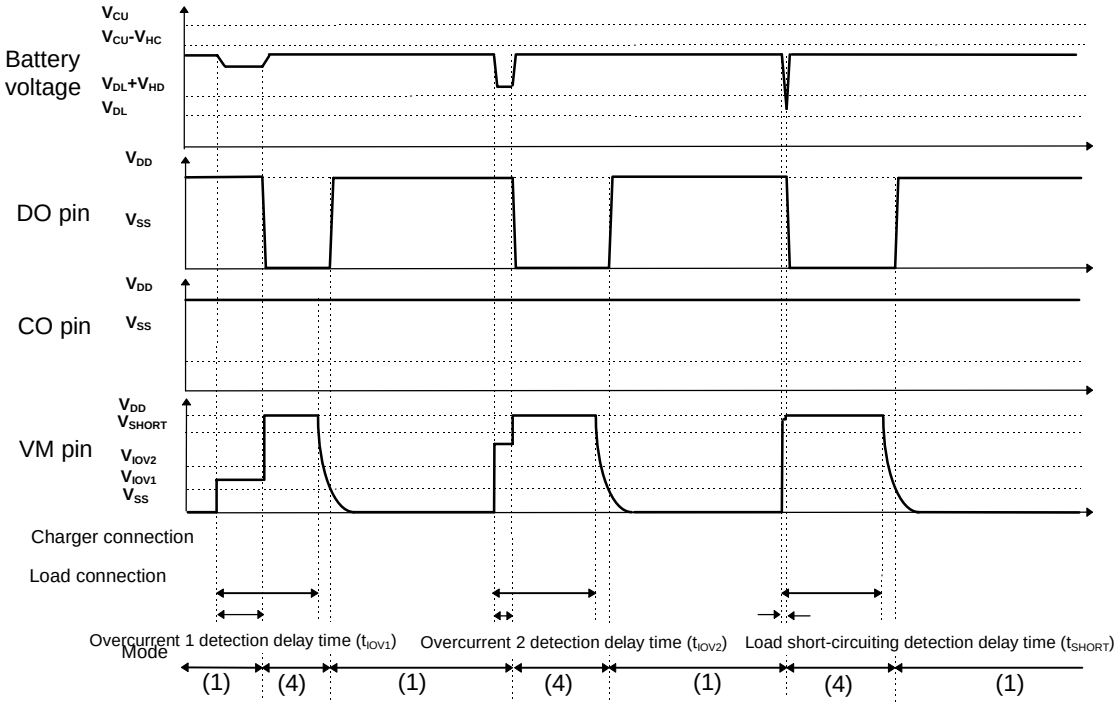
1.Overcharge and overdischarge detection



Note: (1) Normal condition, (2) Overcharge condition, (3) Overdischarge condition, (4) Overcurrent condition
The charger is supposed to charge with constant current.

Figure 6

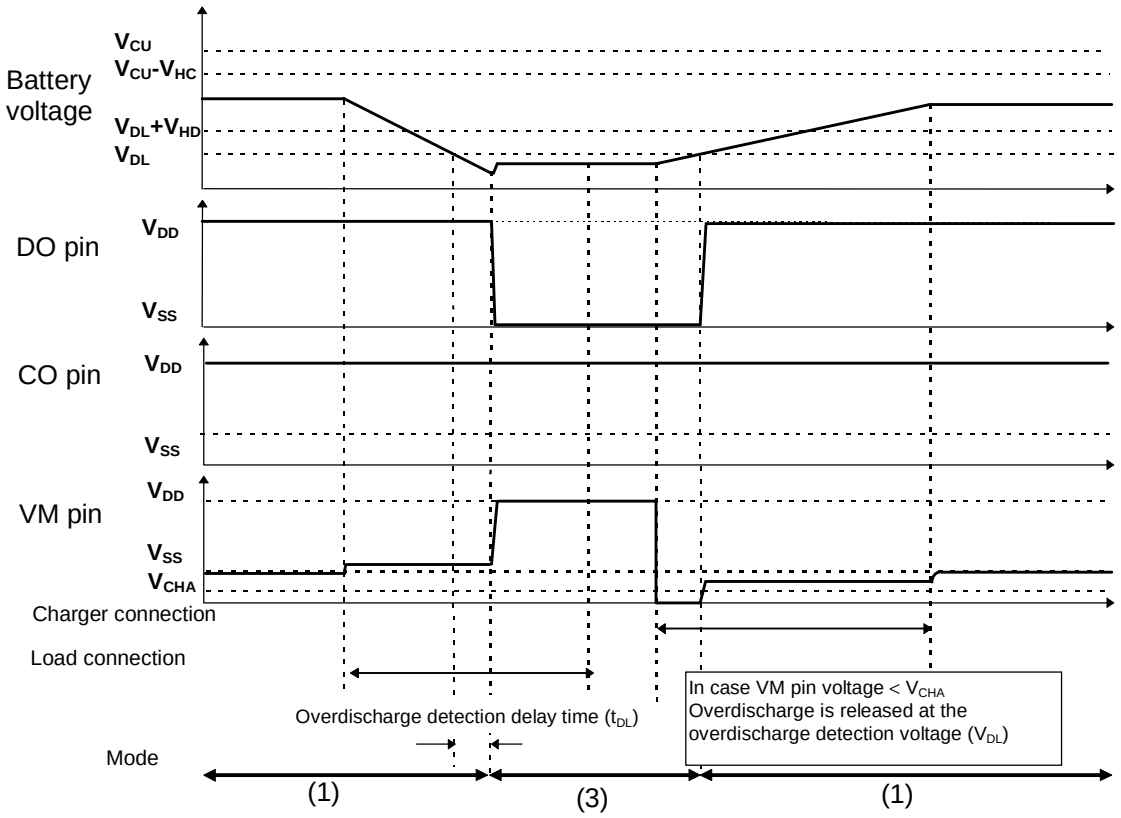
2.Overcurrent detection



Note: (1) Normal condition, (2) Overcharge condition, (3) Overdischarge condition, (4) Overcurrent condition
The charger is supposed to charge with constant current.

Figure 7

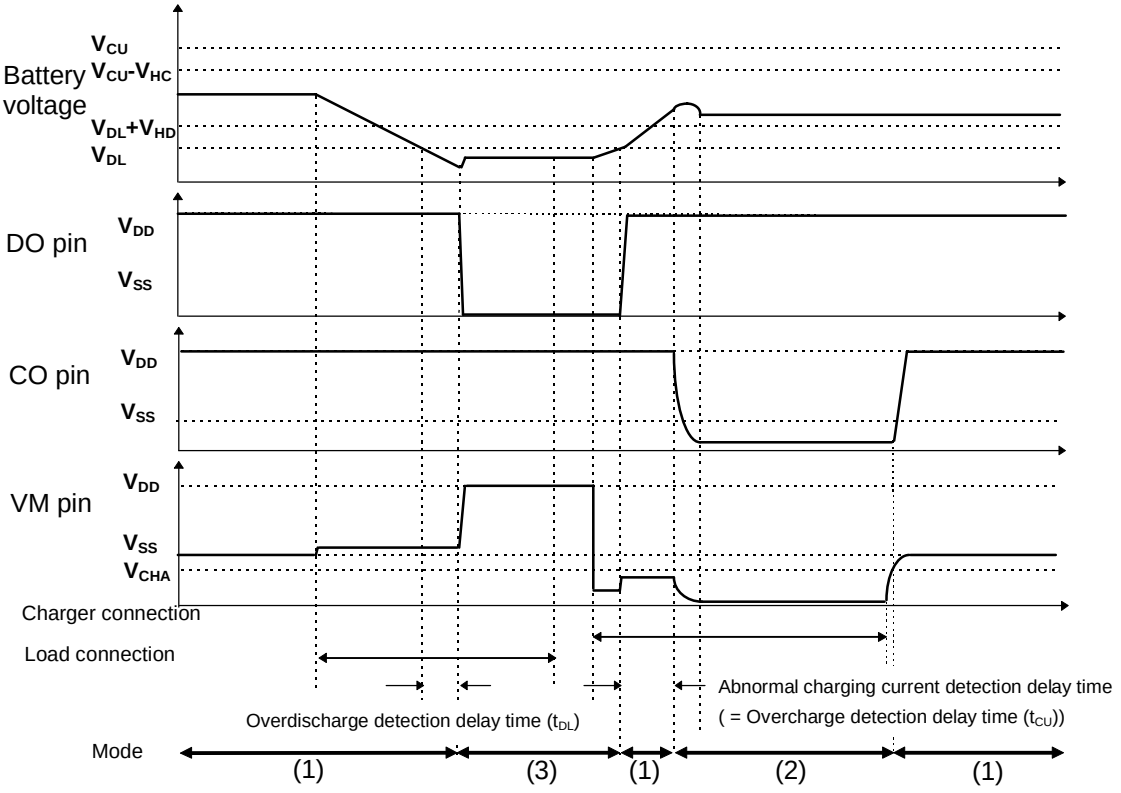
3.Charger detection



Note: (1) Normal condition, (2) Overcharge condition, (3) Overdischarge condition, (4) Overcurrent condition
The charger is supposed to charge with constant current.

Figure 8

4.Abnormal charge current detection



Note: (1) Normal condition, (2) Overcharge condition, (3) Overdischarge condition, (4) Overcurrent condition
The charger is supposed to charge with constant current.

Figure 9

■ An Example for Battery Protection IC Connection

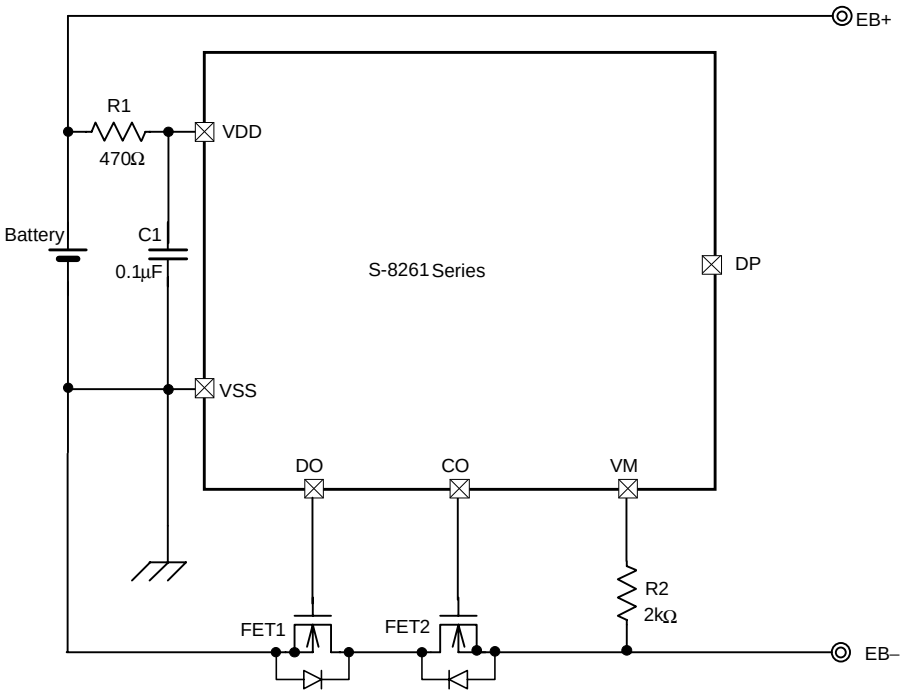


Figure 10

Table 1 Constant for external components

Symbol	Parts	Purpose	Recommend	min.	max.	Remarks
FET1	N channel MOSFET	Charge control	-----	-----	-----	*1) 0.4 V ≤ Threshold voltage ≤ overdischarge detection voltage Gate to source withstand voltage ≥ Charger voltage
FET2	N channel MOSFET	Discharge control	-----	-----	-----	*1) 0.4 V ≤ Threshold voltage ≤ overdischarge detection voltage Gate to source withstand voltage ≥ Charger voltage
R1	Resistor	ESD protection For power fluctuation	470Ω	300Ω	1kΩ	*2) Set resistance so that 2 × R1 ≤ R2.
C1	Capacitor	For power fluctuation	0.1μF	0.022μF	1.0 μF	*3) Install a capacitor of 0.022 μF or higher between VDD and VSS.
R2	Resistor	Protection for reverse connection of a charger	2kΩ	300Ω	4kΩ	*4) To prevent current when a charger is reversely connected. Select a larger resistance within the range from 300Ω to 4kΩ.

*1) If an FET with a threshold voltage of 0.4 V or lower is used, the FET may not cut the charging current.
If an FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stoped before overdischarge is detected.
If the withstand voltage between the gate and source is lower than the charger voltage, the FET may destroy.

*2) If R1 has a high resistance, the voltage between VDD and VSS may exceed the absolute maximum rating when a charger is connected reversely since the current flows from the charger to the IC.
Insert a resistor of 300Ω or higher as R1 for ESD protection.
If R1 has a high resistance, the overcharge detection voltage increases by IC current consumption.

*3) If a capacitor of less than 0.022 μF is installed as C1, DO may oscillate when load short-circuiting is detected.
Be sure to install a capacitor of 0.022 μF or higher as C1.

*4) If R2 has a resistance higher than 4kΩ, the charging current may not be cut when a high-voltage charger is connected.

Note:

- The DP pin should be open.
- The above connection diagram and constants do not guarantee proper operation. Evaluate upon actual application and determine constants properly.

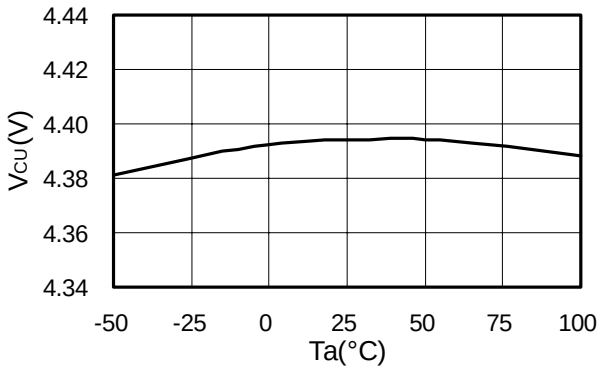
■ Precautions

- Pay attention to the operating conditions for input/output voltage and load current so that the loss in the IC does not exceed the permissible loss (power dissipation) of the package.
- Seiko Instruments Inc. shall not be responsible for any patent infringement by products including the S-8261 series in connection with the method of using the S-8261 series in such products, the product specifications or the country of destination thereof.

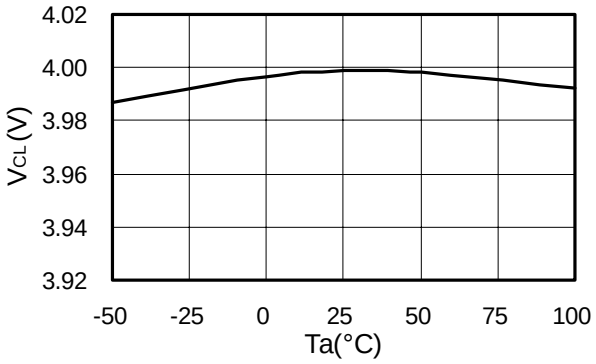
■ Characteristics (typical characteristics)

1. Detection/release voltage temperature characteristics

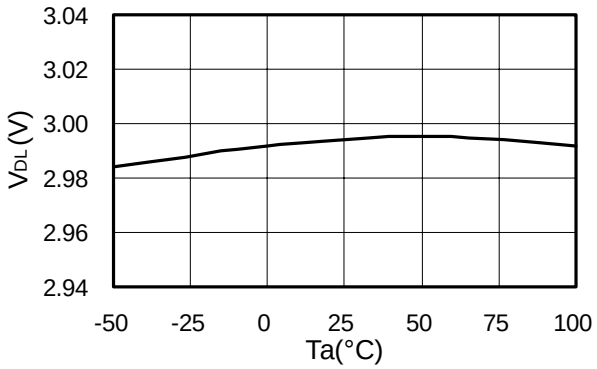
Overcharge detection voltage vs.temperature



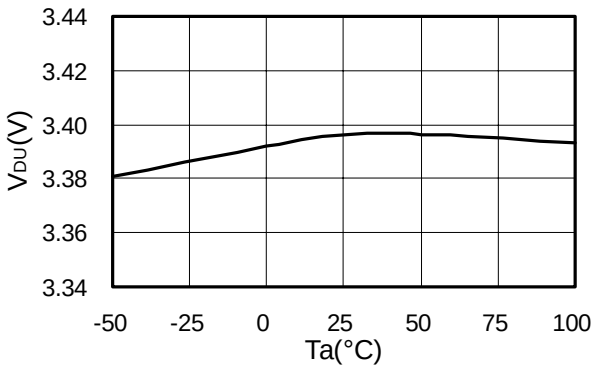
Overcharge release voltage vs.temperature



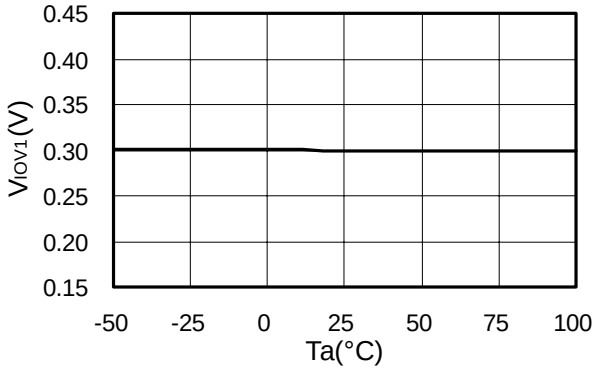
Overdischarge detection voltage vs.temperature



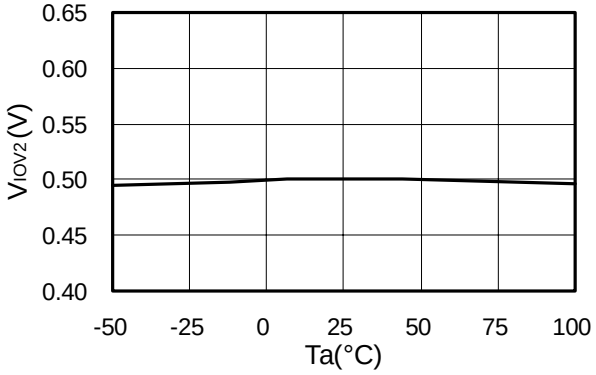
Overdischarge release voltage vs.temperature



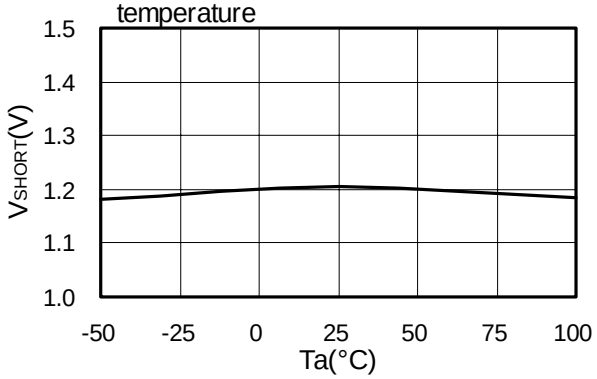
Overcurrent1 detection voltage vs.temperature



Overcurrent 2 detection voltage vs.temperature

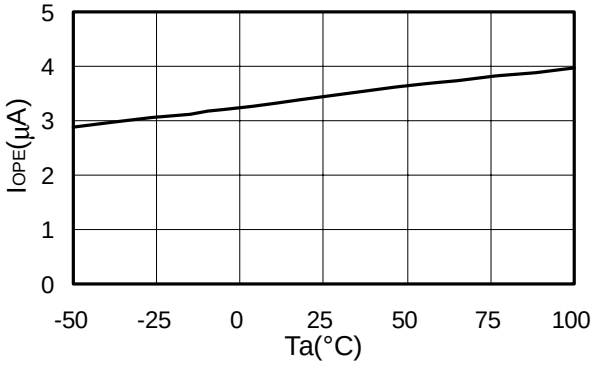


Load short-circuiting detection voltage vs. temperature

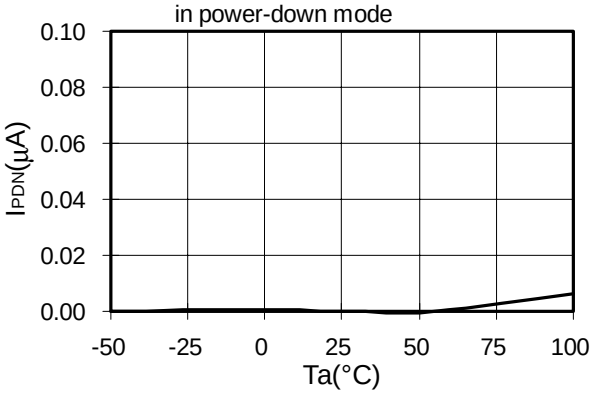


2. Current consumption temperature characteristics

Current consumption vs.temperature in normal mode

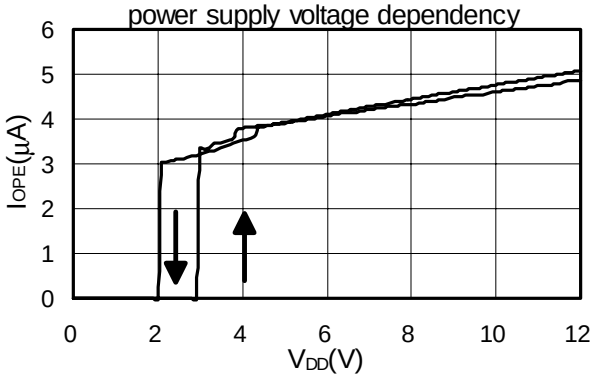


Current consumption vs.temperature in power-down mode



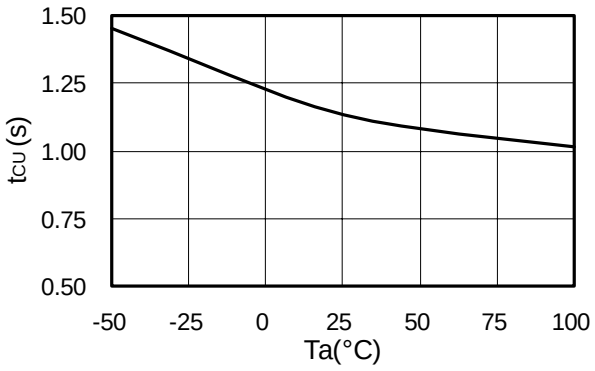
3. Current consumption power voltage characteristics (Ta=25°C)

Current consumption power supply voltage dependency

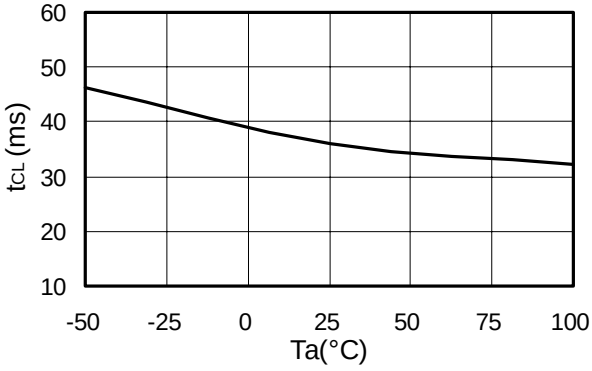


4. Detection/release delay time temperature characteristics

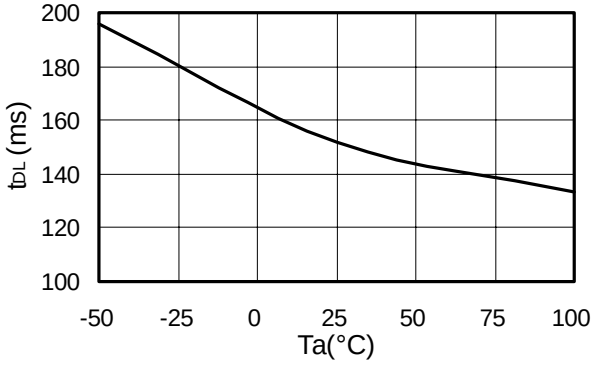
Overcharge detection delay time vs. temperature



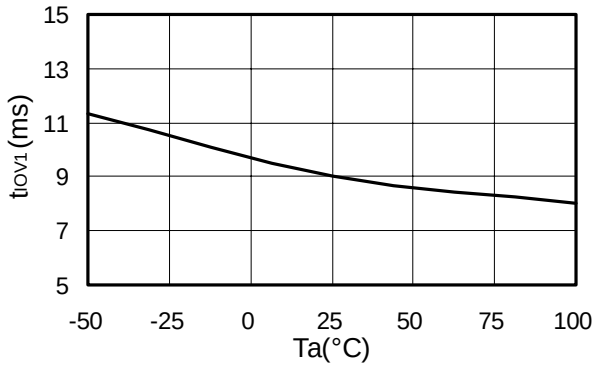
Overcharge release delay time vs. temperature



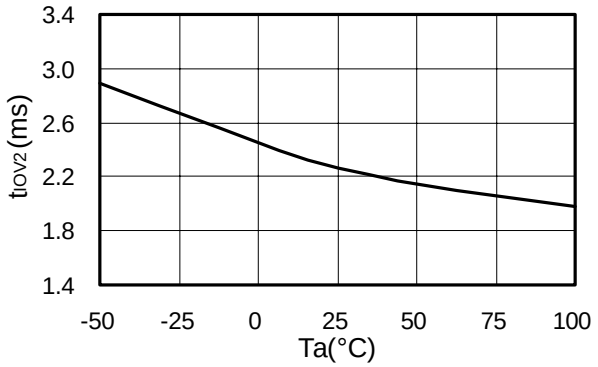
Overdischarge detection delay time vs. temperature



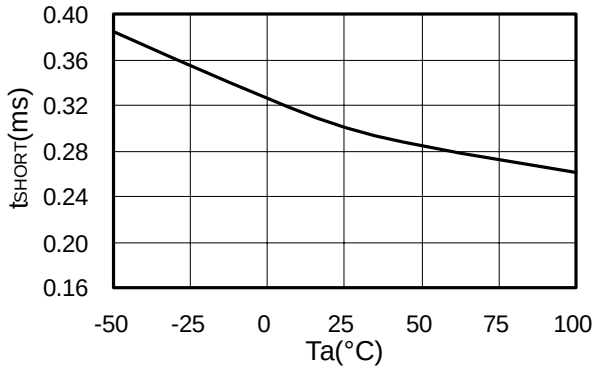
Overcurrent 1 detection delay time vs. temperature



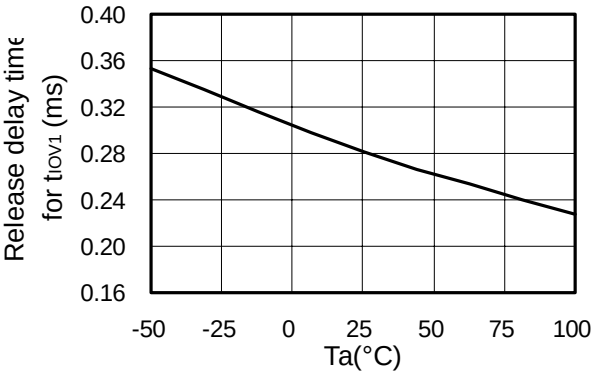
Overcurrent 2 detection delay time vs. temperature



Load short-circuiting delay time vs. temperature

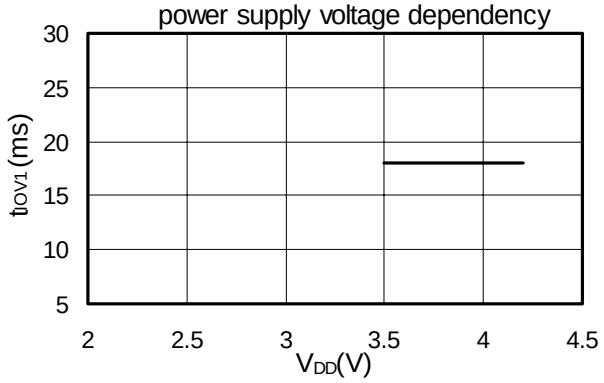


Overcurrent 1 release delay time vs. temperature

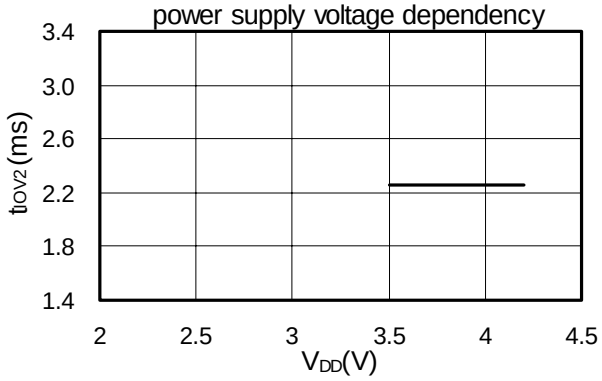


5. Delay time power-voltage characteristics(Ta=25°C)

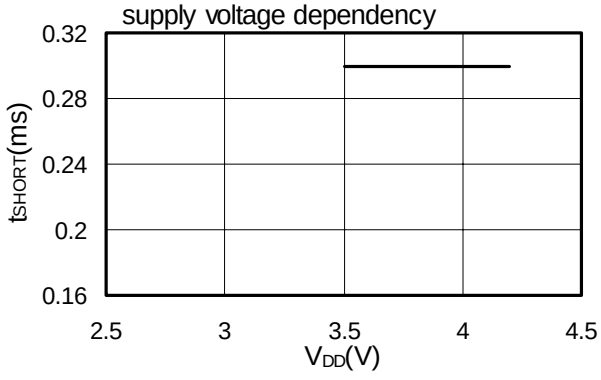
Overcurrent 1 detection delay time vs. power supply voltage dependency



Overcurrent 2 detection delay time vs. power supply voltage dependency



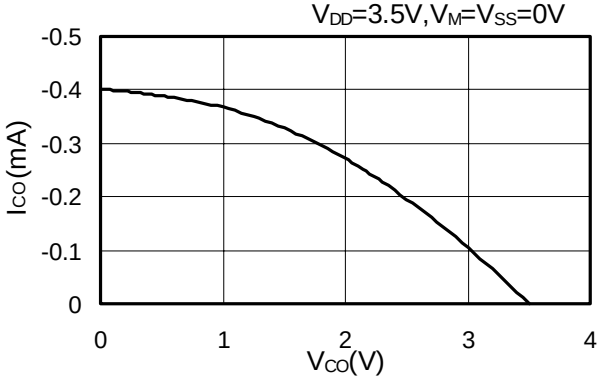
Load short-circuiting delay time vs. power supply voltage dependency



6.CO pin/DO pin output current characteristics(Ta=25°C)

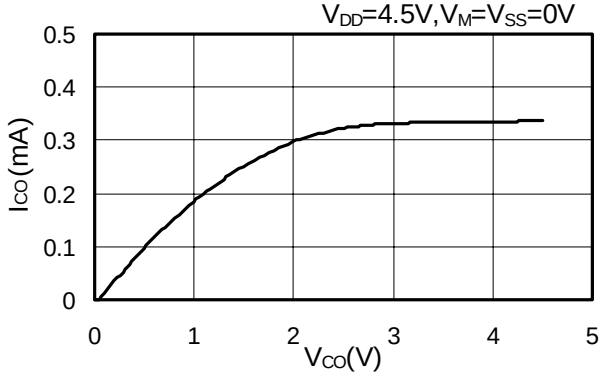
CO pin source current characteristics

V_{DD}=3.5V,V_M=V_{SS}=0V



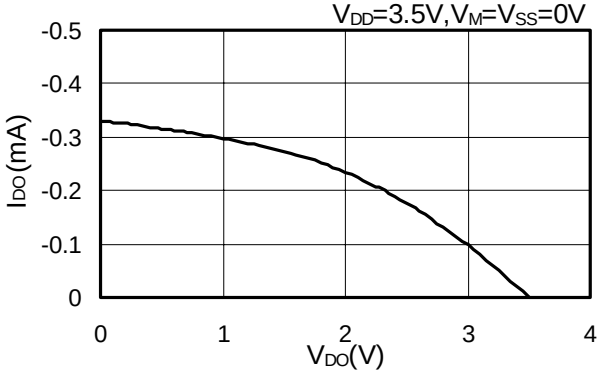
CO pin sink current characteristics

V_{DD}=4.5V,V_M=V_{SS}=0V



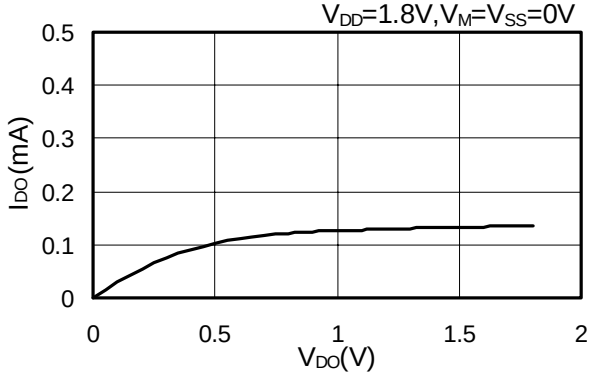
DO pin source current characteristics

V_{DD}=3.5V,V_M=V_{SS}=0V



DO pin sink current characteristics

V_{DD}=1.8V,V_M=V_{SS}=0V

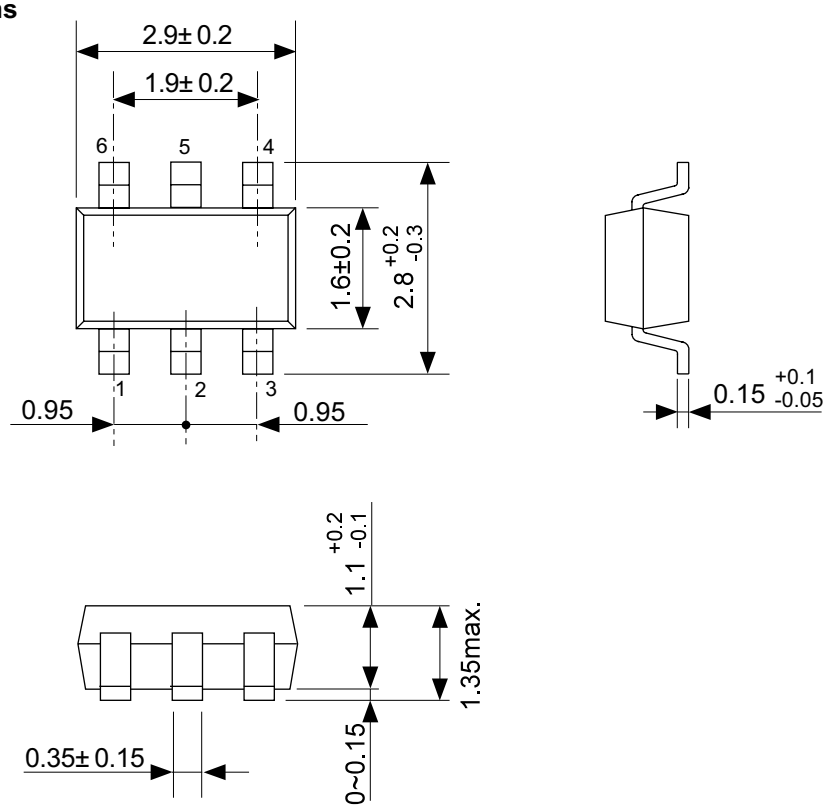


SOT-23-6

MP006-A 010322

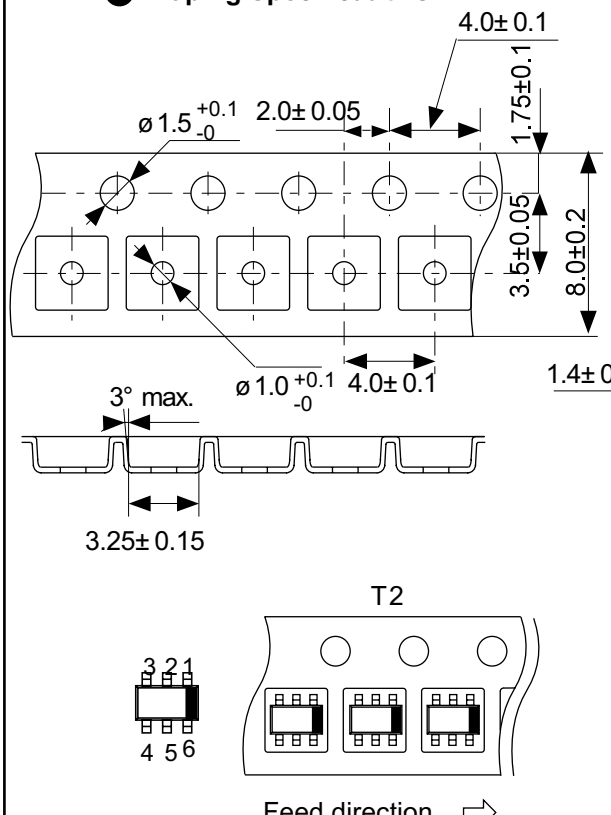
Unit : mm

Dimensions

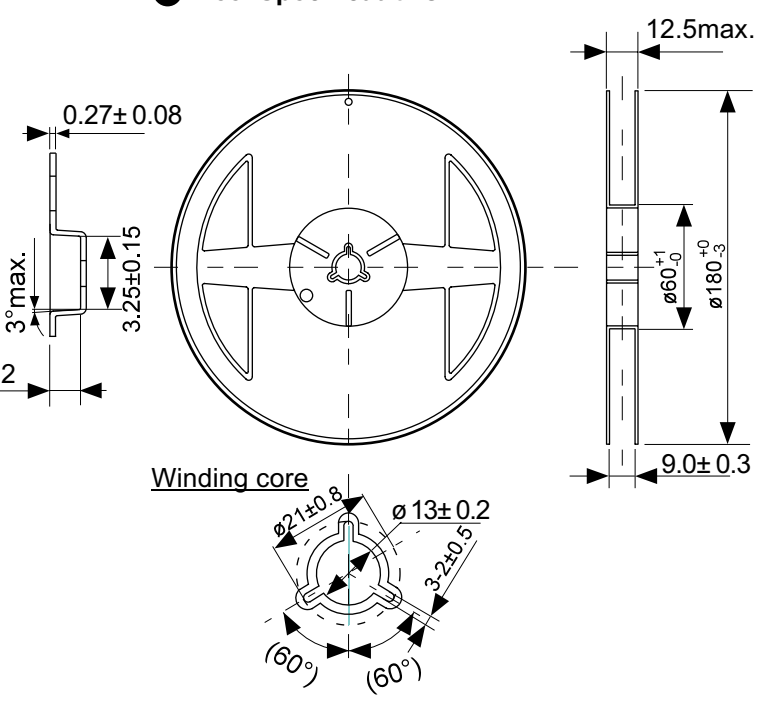


No.MP006-A-P-SD-1.0

Taping Specifications



Reel Specifications

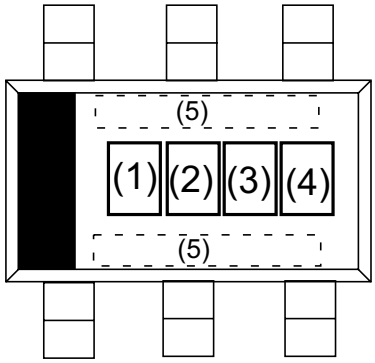


MP006-A-C-SD-1.0

MP006-A-R-SD-1.0

SOT-23-6

● **Markings**

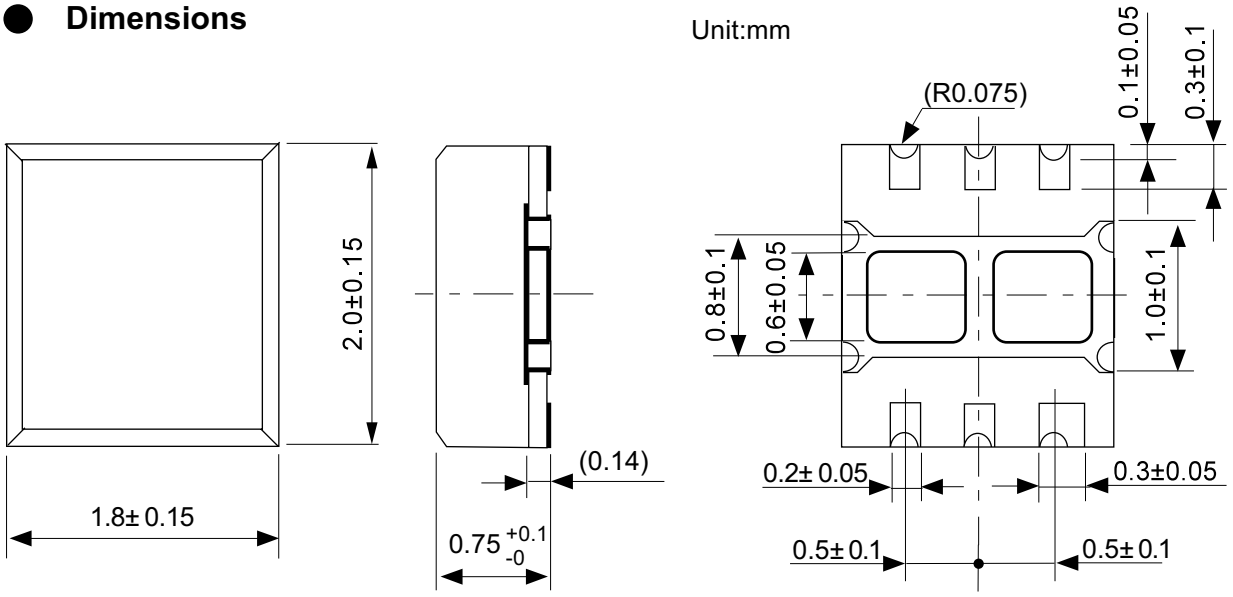


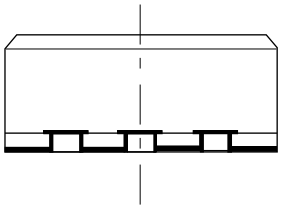
(1)~(3) : Product name (abbreviation)
(4) : Month of assembly
(5) : Dot on one side (Year and week of assembly)

■ SNB6B[1820]

● Dimensions

Unit:mm





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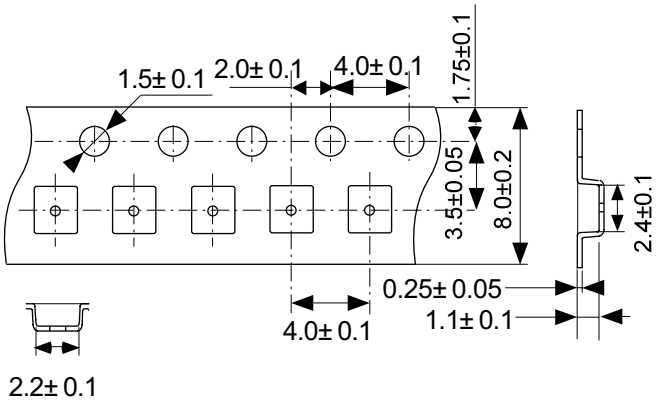
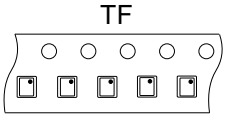
● Taping Specifications

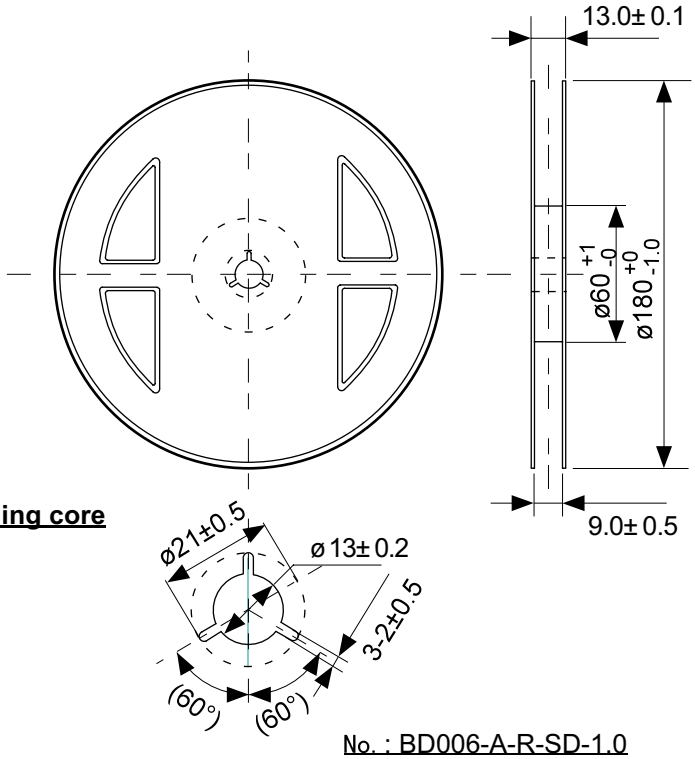




Feed direction ⇨

No. : BD006-A-C-SD-1.0

● Reel Specifications



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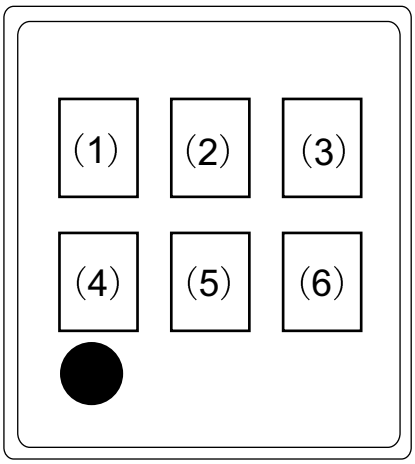
■ Markings

● SNB6B[1820]



(1) ~ (3) : Product name

(4) ~ (6) : Lot No.

● Pin #1 index mark area

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