PERFORMANCE LIMITS OF SWITCHED-CAPACITOR DC-DC CONVERTERS

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Abstract - **Theoretical performance limits of two-phase switched-capacitor (SC) dc-dc converters are discussed in this paper. For a given number of capacitors k, the complete set of attainable dc conversion ratios is found. The maximum step-up or step-down ratio is given by the k^{th} Fibonacci number, while the bound on the number of switches required in any SC circuit is $3k-2$. Practical implications, illustrated by several SC converter examples, include savings in the number of components required for a given application, and the ability to construct SC converters that can maintain the output voltage regulation and high conversion efficiency over a wide range of input voltage variations. Limits found for the output resistance and efficiency can be used for selection and comparison of SC converters.**

1 Introduction

Power converters consisting only of switches and capacitors have long been known and used, mostly as diode-capacitor voltage multipliers [1]-[4]. Switched-capacitor (SC) dc-dc converters, such as the examples shown in Figs. 1 and 2, have recently received renewed interest [5]-[9].

Compared to power converters with both inductive and capacitive energy storage, SC dc-dc converters have several advantageous properties. They use no magnetic components, and are well suited for monolithic integration. Operation down to zero load is possible with no need for dummy loads or complex control techniques. When completely unloaded, the SC converter output voltage assumes a value uniquely determined by the converter topology. Furthermore, by reducing the switching (clock) frequency, the total power losses can be reduced down to zero, while preserving good no-load output-voltage regulation. This is ideally suited for battery-operated applications with power management, where the power converter must operate at almost zero load.

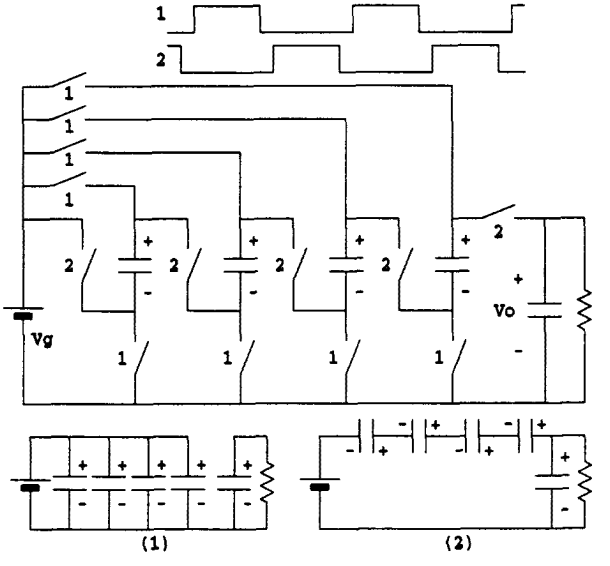

Figure 1: An SC converter with five capacitors and the ideal step-up conversion ratio $M_i = V_o/V_g = 5$.

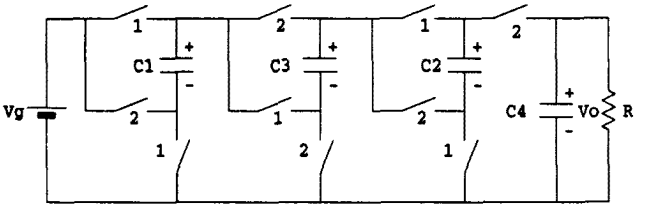

Figure 2: An SC converter with four capacitors and the ideal step-up conversion ratio $M_i = V_o/V_g = 5$.

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A problem with SC converters is that it is difficult to ensure good output voltage regulation in the presence of wide load variations, and in particular in the presence of input voltage variations. Continuous voltage regulation can be achieved, but at the expense of degrading the converter efficiency [7, 8]. Even with ideal components, SC converter has a non-zero output resistance, and losses in the SC power stage increase with load. Because of practical limitations on the size of capacitors and switches, applications of SC converters are limited mainly to low [5, 6], and medium power levels of several tens of watts [9]. Switched-capacitor converters also find applications in combination with switch-mode inductive-capacitive converters [10, 11, 12].

Fig. 1 shows a well-known SC converter that steps up the input voltage. The converter has 5 capacitors and 13 switches. The switches are controlled by a two-phase, non-overlapping clock as shown in Fig. 1. The phase when a switch is on is indicated as phase 1 or phase 2. In a practical implementation, some of the switches may be replaced by diodes. When the switches 1 are on, all capacitors except the output capacitor across the load R are placed in parallel with the input voltage source V_g. When the switches 2 are on, the capacitors placed in series with V_g deliver charge to the output. When the converter is unloaded, the steady-state capacitor voltages are dc only and, by inspection, $V_o = 5V_g$.

It is interesting that the same conversion ratio can be obtained with only 4 capacitors and 10 switches, as shown in Fig. 2. A practical application of this SC converter has been described in [5].

The variety of SC configurations, as illustrated by the examples of Figs. 1 and 2, prompted the investigation of theoretical limits for attainable conversion ratios for a given number of elements. It is the main objective of this paper is to establish these limits two-phase switched-capacitor (SC) dc-dc converters using tools of linear algebra and graph theory. These tools can also be used for systematic synthesis of SC DC-DC converters. However, instead of attempting to enumerate all possible SC topologies, we enumerate the set of attainable conversion ratios. Practical implications of the presented theoretical results are also discussed.

Section 2 of the paper shows how the ideal conversion ratio of an unloaded SC converter can be found efficiently using the incremental one-graph formulation [11]. The incremental one-graph formulation is also used as a tool to derive other properties of SC converters. The main results on the realizable conversion ratios, and about the number of switches needed for implementation are presented in Section 3. Limits for the SC converter output resistance and efficiency are discussed in Section 4. Contributions of the paper are summarized in Section 5.

2 Ideal Voltage Conversion Ratio

The ideal dc conversion ratio, $M_i = V_o/V_g$, when the converter is unloaded, can be obtained from a description of the converter topology. The example of Fig. 2 is used to illustrate the discussion. The two switched networks of this converter, corresponding to the two clock phases, are shown in Fig. 3.

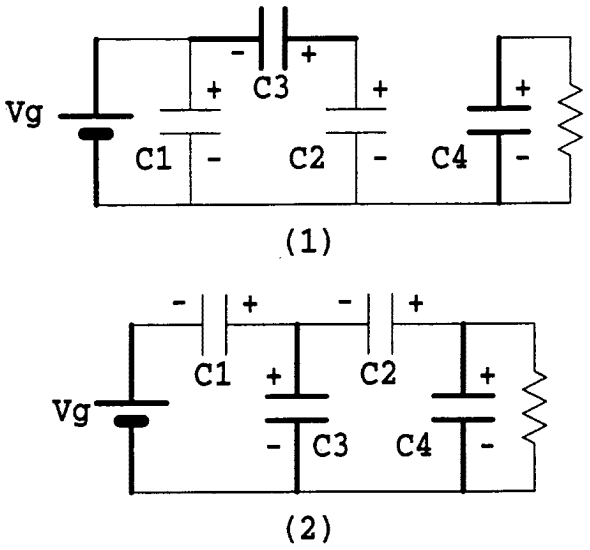

Figure 3: The two switched networks of the SC converter in Fig. 2, corresponding to the clock phases 1 and 2. Twig branches are highlighted.

For an unloaded SC converter, the conversion ratio takes the form

$$M_i = V_o/V_g = P/Q\,, \tag{1}$$

where P and Q are integer values that depend only on how the capacitors are interconnected in the two switched networks. Dependencies on the values of capacitances, esr and switch resistances, switching frequency, clock duty ratios, etc., are removed and the problem of finding the *ideal conversion ratio* reduces to pure topological aspect.

To find a general expression for the ideal conversion ratio, it is convenient to choose the fundamental loop matrices to describe the capacitor interconnections in the two switched networks. The total number of elements is $k+1$, k capacitors and one dc voltage source V_g. In each switched network ($j = 1, 2$) we have $k_t(j)$ capacitor twigs that form a tree together with the source V_g twig, while $k_l(j) = k - k_t(j)$ capacitor branches are links. One can write $k_l(j)$ independent voltage-loop equations for each of the two networks. To get unique solution for k capacitor voltages, we need a total of k independent equations, so that the two switched networks must satisfy:

$$k_l(1) + k_l(2) = k_t(1) + k_t(2) = k\,. \tag{2}$$

In the example of Fig. 3, where the twig branches are highlighted in the switched networks, we have $k_l = 2$ capacitor links and $k_t = 2$ capacitor twigs in each of the two networks. Now we consider the system of two fundamental-loop matrices: $\mathbf{B_f}(1)$, for the network in phase 1, and $\mathbf{B_f}(2)$ for the network in phase 2. The dimensions of the matrix $\mathbf{B_f}(j)$ are $k_l(j) \times (k+1)$. If we order the elements as: $k_l(j)$ capacitor links first, $k_t(j)$ capacitor twigs next, and the V_g twig last, we

have the fundamental loop matrix for each of the two networks in the form

$$\mathbf{B_f}(j) = \left[\begin{array}{ccc} \mathbf{U}(j) & \mathbf{B_t}(j) & \mathbf{b}(j) \end{array} \right], \tag{3}$$

where $\mathbf{U}(j)$ is a $k_l(j) \times k_l(j)$ identity matrix, $\mathbf{B_t}(j)$ is a $k_l(j) \times k_t(j)$ matrix of twig-capacitor connection coefficients, and the coefficients in the $\mathbf{b}(j)$ vector show the connections of V_g. Finally, the combined system of KVL equations becomes

$$\mathbf{B} \left[\begin{array}{c} \mathbf{v_C} \\ V_g \end{array} \right] = 0, \tag{4}$$

where $\mathbf{B} = \left[\begin{array}{cc} \mathbf{B_f}(1) & \mathbf{B_f}(2) \end{array} \right]^T$ is the system matrix, and $\mathbf{v_C}$ is the vector of capacitor voltages. For any given SC network, the system (4) can be solved for all capacitor voltages in terms of V_g, as in [2]. Instead, we apply the efficient method of solving (4) based on the *incremental representation* of loop equations that combines the two-graph formulation into incremental one-graph formulation [11]. In this formulation, link voltages are eliminated from (4) so that the resulting smaller system can be solved for twig voltages.

As an example, consider the case when k is even, and the number of twigs is the same in both switched networks, so that $k_t(1) = k_t(2) = k_l(1) = k_l(2) = k/2$. The system (4) becomes

$$\left[\begin{array}{ccc} \mathbf{U} & \mathbf{B_t}(1) & \mathbf{b}(1) \\ \mathbf{U} & \mathbf{B_t}(2) & \mathbf{b}(2) \end{array} \right] \left[\begin{array}{c} \mathbf{v_{cl}} \\ \mathbf{v_{ct}} \\ V_g \end{array} \right] = 0, \tag{5}$$

where $\mathbf{v_{cl}}$ and $\mathbf{v_{ct}}$ are the vectors of capacitor link and the capacitor twig voltages, respectively. In the incremental one-graph form, the system becomes

$$\left[\begin{array}{cc} \Delta\mathbf{B_t} & \Delta\mathbf{b} \end{array} \right] \left[\begin{array}{c} \mathbf{v_{ct}} \\ V_g \end{array} \right] = 0, \tag{6}$$

where

$$\Delta\mathbf{B_t} = \mathbf{B_t}(1) - \mathbf{B_t}(2), \tag{7}$$

$$\Delta\mathbf{b} = \mathbf{b}(1) - \mathbf{b}(2). \tag{8}$$

Note that the system is of order $k/2 \times (k/2+1)$ and yields all capacitor twig voltages $\mathbf{v_{ct}}$ in terms of V_g,

$$\mathbf{v_{ct}} = -(\Delta\mathbf{B_t})^{-1} \Delta\mathbf{b}\, V_g \tag{9}$$

In the example of Figs. 2, and 3, we have:

$$\mathbf{v_{ct}} = \left[\begin{array}{c} v_{c3} \\ v_{c4} \end{array} \right] = -\left[\begin{array}{cc} 1 & 0 \\ -2 & 1 \end{array} \right]^{-1} \left[\begin{array}{c} -2 \\ -1 \end{array} \right] V_g = \left[\begin{array}{c} 2 \\ 5 \end{array} \right] V_g. \tag{10}$$

Since $V_o = v_{c4}$, we conclude that the converter of Fig. 2 has indeed the ideal conversion ratio equal to $M_i = 5$.

The incremental one-graph formulation for degenerate switch-mode converters (such as switched-capacitor converters) plays the role of averaging for nondegenerate converters consisting of switches, inductors and capacitors [11]. The formulation significantly reduces the size of the system to be solved, and it also serves as a tool for deriving other converter properties, as discussed next.

3 Bounds on Synthesis

With the efficient tool for finding the ideal dc conversion ratio, we can enumerate all possible SC converter networks for a given number of capacitors k, in search for a particular desired conversion function. However, the brute-force synthesis method can only be applied for small k because the size of the problem quickly increases beyond available computational resources when the number of capacitors k increases.

Instead, we tackled the problems of finding the theoretical limits on the realizable conversion ratios for a given number of capacitors k, and for the number of switches needed for realization. The results are given in the following:

Theorem 1. (Bounds on Voltage Ratio). *The realizable conversion ratio of a two-phase switched-capacitor dc-dc converter with a single dc voltage source V_g is given by a common fraction in the form*

$$M_i(k) = \frac{V_o}{V_g} = \frac{P[k]}{Q[k]}, \tag{11}$$

where $P[k]$ and $Q[k]$ are integers that satisfy inequalities

$$Max[Abs[P[k]],\ Abs[Q[k]]] \leq F_k, \tag{12}$$

$$Min[Abs[P[k]],\ Abs[Q[k]]] \geq 1, \tag{13}$$

k is the total number of capacitors, and F_k is the k-th Fibonacci number.

A formal proof can be found in [13]. Some elements of the proof are given here to aid understanding origins of the limits found in Theorem 1. First, from Eq. (9), it is clear that all possible $P[k]$ or $Q[k]$ in $M_i = P[k]/Q[k]$ can be found as all possible values of the determinant $\det[\Delta\mathbf{B_t}]$ of the incremental loop matrix defined by Eq. (7), subject to the constraint that matrices $\mathbf{B_t}(j)$ with elements -1, 0, or 1, correspond to realizable networks. The realizability constraint calls for regular matrices, which is equivalent here to the condition of unimodularity of $\mathbf{B_t}(j)$, i.e., to the requirement that all minors (determinants of square submatrices) of $\mathbf{B_t}(j)$ can only be equal to -1, 0, or 1.

Assume that we have an even number of capacitors k, and that $k_t = k_l = k/2$. Starting with

$$\Delta\mathbf{B_t} = \left[\begin{array}{cc} \mathbf{U} & -\mathbf{U} \end{array} \right] \left[\begin{array}{c} \mathbf{B_t}(1) \\ \mathbf{B_t}(2) \end{array} \right], \tag{14}$$

the determinant $\det[\Delta\mathbf{B_t}]$ of the product is expanded using the *Binet-Cauchy formula* into a sum of products of minors over all $k_t \times k_t$ submatrices. In the sum, there are $\left(\begin{array}{c} 2k_t \\ k_t \end{array} \right)$ components. Take, for example, the case with $k = 4$ capacitors, with $k_l = k_t = 2$:

$$\det[\Delta\mathbf{B_t}] = \det \left[\left[\begin{array}{cc|cc} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \end{array} \right] \left[\begin{array}{cc} 1 & 0 \\ b_{23}(1) & 1 \\ \hline -1 & b_{14}(2) \\ 0 & -1 \end{array} \right] \right], \tag{15}$$

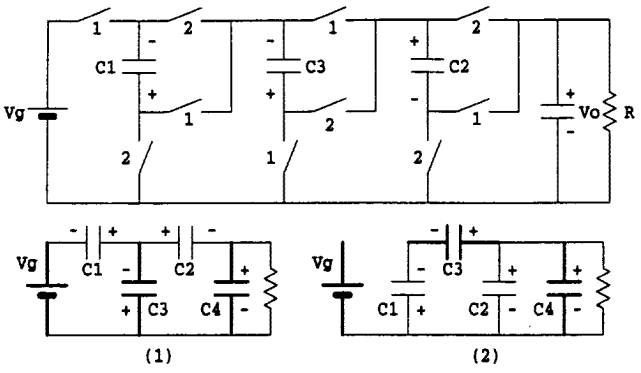

Figure 4: An SC converter with $k = 4$ capacitors and the ideal conversion ratio $M_i = V_o/V_g = 1/5$. Twig branches are highlighted.

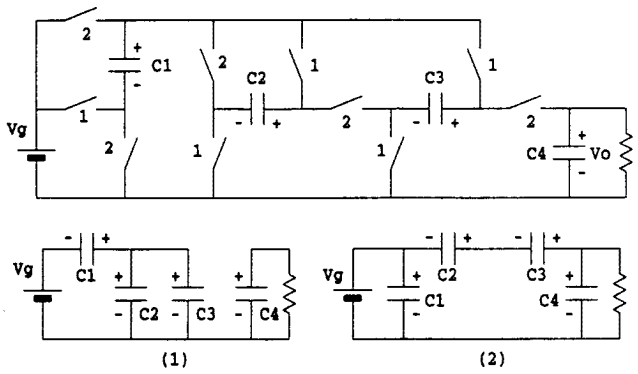

Figure 5: Another SC converter with $k = 4$ capacitors and the ideal conversion ratio $M_i = V_o/V_g = 5$.

where the form of $\mathbf{B_t}(1)$ and $\mathbf{B_t}(2)$ is selected to maximize $\det[\mathbf{\Delta B_t}]$, preserve unimodularity, and leave the largest number of elements undetermined. In this case, $b_{23}(1)$ and $b_{14}(2)$ are arbitrary. The sum of products in the Binet-Cauchy formula has 6 terms, 2 of which are equal to zero, and 3 of which are equal to 1:

$$\det[\mathbf{\Delta B_t}] = 3 + \det\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \det\begin{bmatrix} b_{23}(1) & 1 \\ -1 & b_{14}(2) \end{bmatrix}. \tag{16}$$

The maximum value of 5 is for $b_{23}(1) \cdot b_{14}(2) = 1$. The incremental loop matrix corresponding to the maximum possible $\det[\mathbf{\Delta B_t}][k = 4] = 5$ is given by:

$$\mathbf{\Delta B_t}[k = 4] = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} - \begin{bmatrix} -1 & 1 \\ 0 & -1 \end{bmatrix} = \begin{bmatrix} 2 & -1 \\ 1 & 2 \end{bmatrix}. \tag{17}$$

An SC converter corresponding to this case is shown in Fig. 4. It can be recognized as the step-down version of the converter in Fig. 2, with the ideal conversion ratio equal to $M_i = V_o/V_g = 1/5$.

For even k, proceeding in the same manner, and by expanding the determinants in terms of cofactors of the first column, a recursive formula is found for the maximum determinant values,

$$\begin{aligned} \det[\mathbf{\Delta B_t}[k]] &= 2\det[\mathbf{\Delta B_t}[k-2]] + \det[\mathbf{\Delta B_t}[k-4]] + \\ &\quad + \ldots + \det[\mathbf{\Delta B_t}[k=2]] + 1\,. \end{aligned} \tag{18}$$

A similar formula is found for k odd, so that in general

$$\det[\mathbf{\Delta B_t}[k]] = \det[\mathbf{\Delta B_t}[k-1]] + \det[\mathbf{\Delta B_t}[k-2]]\,, \tag{19}$$

which gives the maximum limit for the attainable conversion ratio in Theorem 1. It is then shown how *any* voltage ratio constrained by Theorem 1 is realizable.

A by-product of the proof of Theorem 1 is the following:

Theorem 2: (The Number of Switches Required). *The number of switches n_s required to realize the maximum attainable voltage ratio $M_{max}(k)$ with k capacitors is given by*

$$n_s[M_{max}(k)] = 3k - 2\,. \tag{20}$$

This is also the bound on the number of switches required for any SC circuit configuration with k switches. A procedure has been developed to determine the number of switches required for any converter directly from the incremental one-graph formulation [13].

3.1 Practical implications

Theorem 1 states that the maximum (absolute value) attainable conversion ratio (step-up or step-down) of two-phase SC dc-dc converter is given by *Fibonacci number*, i.e., by the recursive definition:

$$M_{max}(0) = F_0 = 1\,, \tag{21}$$

$$M_{max}(1) = F_1 = 1\,, \tag{22}$$

$$M_{max}(k) = F_k = F_{k-2} + F_{k-1}\,, \quad \text{for } k > 1\,. \tag{23}$$

This gives the sequence:

$$1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, \ldots \tag{24}$$

where each number is the sum of the previous two. Note that, as k increases, significantly higher conversion ratios are available than with well known SC converters with $M_i(k) = k$ [8, 9]. For example, for $k = 5$ and $n_s = 13$, the (step-up or step-down) conversion ratio $M_i = 8$ can be obtained, compared to $M_i = 5$ of the converter in Fig. 1. Conversely, for a specified conversion ratio, a converter with M_{max} requires less capacitors and switches, as illustrated by the examples in Fig. 1 and Fig. 2.

The example of Fig. 2 has the maximum possible step-up conversion ratio $M_i = 5$, and the number of switches equal to 10, as predicted by Theorem 2. The Fibonacci realization of Fig. 2 is canonical because one can easily construct the Fibonacci SC converter for any k by adding more stages in the same pattern. It is interesting, however, that the SC configuration with the maximum conversion ratio is not unique. For example, Fig. 5 shows another 4-capacitor converter with the ideal conversion ratio equal to 5. A disadvantage of the Fibonacci converters is that the capacitors do not carry the

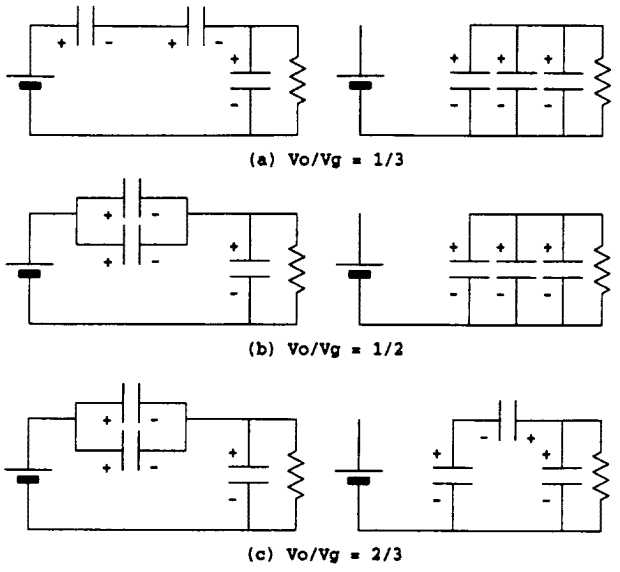

Figure 6: Switched circuits corresponding to the ideal step-down conversion ratios: (a) $M_i = 1/3$, (b) $M_i = 1/2$, and (c) $M_i = 2/3$, achievable with 3 capacitors.

same dc voltages. The capacitor voltages in a given Fibonacci converter also follow the Fibonacci sequence.

Another important practical implication of Theorem 1 is that it specifies the *complete* set of realizable conversion ratios for a given number of capacitors. For example, for $k = 2$, the set consists of 1/2, 1 and 2, plus conversion ratios with negative sign. For $k = 4$, neglecting sign, we have 19 distinct realizable ratios: 1/5, 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 1, 5/4, 4/3, 3/2, 5/3, 2, 5/2, 3, 4, and 5.

The availability of a number of distinct conversion ratios gives a possibility to achieve active output voltage regulation in the presence of wide input voltage variations, without compromising conversion efficiency. The idea is to on-line select the SC configuration so that the output voltage is closest to the nominal value for a given input voltage.

As an example, Fig. 6 shows the switched circuits corresponding to the three step-down conversion ratios 1/3, 1/2, and 2/3 with $k = 3$ capacitors. The three configurations can be combined into SC dc-dc converter as shown in Fig. 7. The configurations are coded by two logic-level signals A and B, and the appropriate control signals for the switches are indicated. A feedforward scheme can easily be constructed where the control code AB is generated by sensing the input voltage V_g. Neglecting load variations, the converter of Fig. 7 can maintain the output voltage within $\pm 10\%$ for about 3-to-1 range of input voltages. Unlike with other control schemes for SC converters, the conversion efficiency is not directly affected. In a monolithic implementation, the increased number of switches and the control complexity may not be a strong disadvantage.

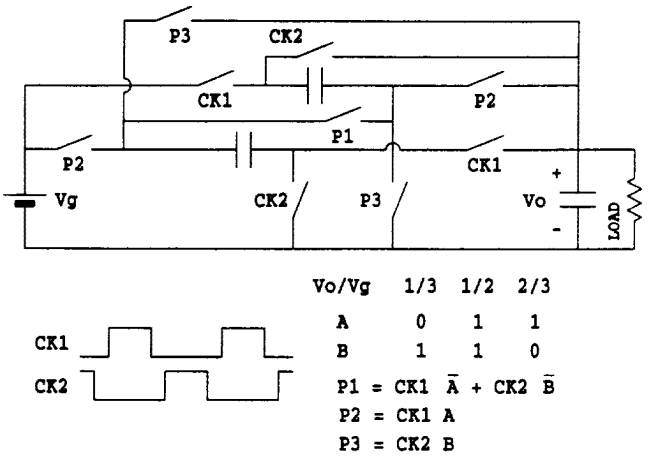

Figure 7: An SC converter with 3 capacitors and adjustable step-down conversion ratio.

4 Output Resistance and Efficiency

With a non-zero load at the output of an SC converter, the steady-state output voltage (in absolute value) is lower than the ideal unloaded value $V_o = M_i V_g$. This is because all capacitors in the converter are periodically charged and discharged in order to supply the output current to the load. As a result, capacitor voltages now have an ac ripple component. Energy is lost on the capacitor esr's and the switch on-resistances during each charge transfer to or from a capacitor. The energy loss is smaller if the ac components in capacitor voltages are smaller.

In general, precise knowledge of all network parasitics is necessary in order to estimate the converter power losses and efficiency. Depending on the values of network "parasitic" time constants τ_i with respect to the switching period T_s, we can distinguish three different cases, and identify three possible analysis methods.

If $\tau_i >> T_s$, the capacitor voltage ripples are approximately linear, and the method of state-space averaging can be applied to determine the converter steady-state and dynamic responses [8, 12]. As τ_i becomes closer to T_s, the ripple nonlinearity can no longer be neglected. The method of modified state-space averaging can be used to handle this case [9, 14]. Finally, if $\tau_i << T_s$, the charge/discharge transients are completed within each clock cycle. In this limiting case, the converter efficiency and the converter output resistance reach the best possible limits. These limits can be used for initial SC converter comparison and selection, and can be derived directly from the converter topological description, as in [2]. The results depend on capacitance values and the switching frequency $f_s = 1/T_s$, but the exact knowledge of the network parasitic resistances is not required, as long as the condition $\tau_i << T_s$ is satisfied.

A DC model for SC converters is shown in Fig. 8. The model consists of an ideal dc transformer with the turns ratio $1 : M_i$, and the output resistance R_o. To determine the output

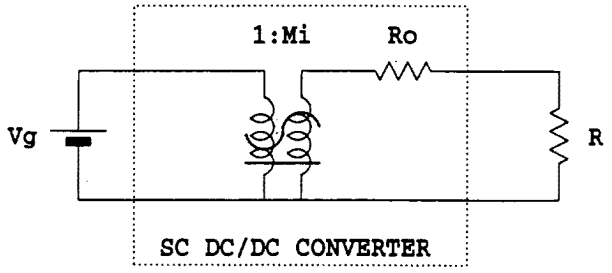

Figure 8: A DC model.

resistance, we consider the SC network with $V_g = 0$ and with an ideal test voltage source V_o applied between the output terminals. The output resistance is then determined from

$$R_o = -\frac{V_o}{q/T_s}, \tag{25}$$

where q is the charge supplied to the source V_o during one switching period, in steady state. Fig. 9 shows the two switched networks corresponding to the example of Figs. 2 and 3, and the setup described above. The goal is to find $q = q(1) + q(2)$. The charge vectors in the two switched networks are given by:

$$\mathbf{q}(1) = \left[\begin{array}{ccccc} q_1 & q_2 & \cdots & q_{k-1} & q(1) \end{array}\right]^T, \tag{26}$$

$$\mathbf{q}(2) = \left[\begin{array}{ccccc} -q_1 & -q_2 & \cdots & -q_{k-1} & q(2) \end{array}\right]^T, \tag{27}$$

Next, the two sets of fundamental cut-set equations,

$$\left[\begin{array}{cc} -\mathbf{B_t}^T(j) & \mathbf{U}(j) \end{array}\right] \mathbf{q}(j) = 0, \tag{28}$$

can be solved for charges $\mathbf{q}(1)$ in terms of the total charge $q = q(1) + q(2)$ through the generator V_o,

$$\mathbf{q}(1) = \mathbf{a}\, q. \tag{29}$$

In the example of Fig. 9, $\mathbf{a}^T = \left[\begin{array}{cccc} 2 & 1 & -1 & 0 \end{array}\right]$. Finally, the fundamental-loop equations,

$$\left[\begin{array}{cc} \mathbf{U}(1) & \mathbf{B_t}(1) \\ \mathbf{U}(2) & \mathbf{B_t}(2) \end{array}\right] \mathbf{v_C} + \left[\begin{array}{cc} \mathbf{U}(1) & \mathbf{B_t}(1) \\ \mathbf{0} & \mathbf{0} \end{array}\right] \left[\begin{array}{c} \frac{a_1}{C_1} \\ \vdots \\ \frac{a_{k-1}}{C_{k-1}} \\ 0 \end{array}\right] q = 0 \tag{30}$$

are solved for q as a function of V_o, to obtain the output resistance R_o from Eq. (25). If all capacitances have the same value C, the output resistance takes the form:

$$R_o = \frac{p}{q}\frac{T_s}{C}, \tag{31}$$

where p and q are positive integers that depend only on the converter topology. For the SC converter example of Fig. 2, we get $R_o = 6T_s/C$. The converter of Fig. 1 has $R_o = 4T_s/C$,

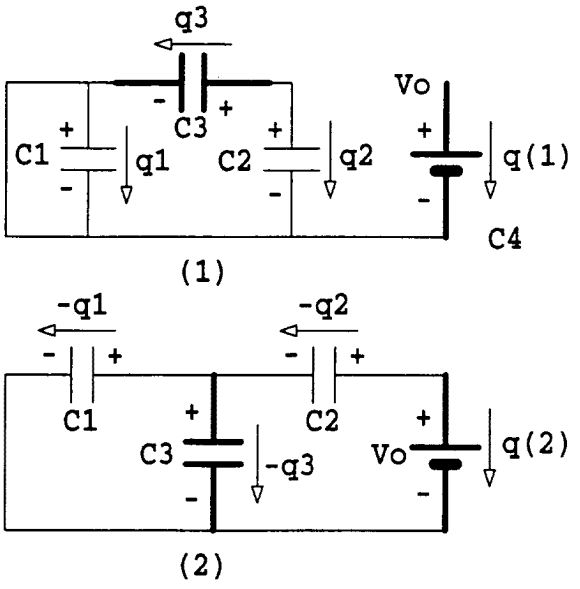

Figure 9: The networks for finding the output resistance $R_o = -V_oT_s/(q(1)+q(2))$ in the SC converter example of Fig. 2. The twig branches are highlighted as in Fig. 3. Note that V_g is set to zero.

but it has one more capacitor and three more switches. From the model of Fig. 8 it follows that the step-down versions of the converters in Figs. 1 and 2, have the output resistances $R_o = 6T_s/25C$, and $R_o = 4T_s/25C$, respectively.

The above procedure can be used to determine the lower limit for the output resistance of any SC converter, for a given switching frequency f_s. It is important to note that the limit for output resistance is reached if $\tau_i << T_s$. Unfortunately, the output resistance cannot be reduced arbitrarily by increasing the switching frequency. Fig. 10 compares the theoretical limit $6T_s/C$ with values obtained by simulation, for a range of ratios $R_{on}C/T_s$ in the example of Fig. 2. R_{on} is the switch on-resistance. The numerical values are $R_{on} = 2\Omega$ and $C = 1\mu F$, and the switching frequency is varied between $f_s = 1/T_s = 5$KHz and $f_s = 250$kHz. The converter output resistance follows the limit for low $R_{on}C/T_s$, but then levels off at about $R_o = 100\Omega$.

An upper limit for the SC power-stage efficiency η can be determined from the model of Fig. 8,

$$\eta = \frac{V_oI_o}{V_gI_g} = \frac{V_o}{V_g}\frac{1}{M_i} = \frac{1}{1 + R_o/R} \tag{32}$$

As expected, the best possible SC power-stage efficiency (for a given switching frequency) decreases with increasing load current.

5 Conclusions

The main result of the paper is the set of realizability conditions on dc conversion ratio of two-phase switched-capacitor dc-dc converters (Theorems 1 and 2). Incremental one-graph

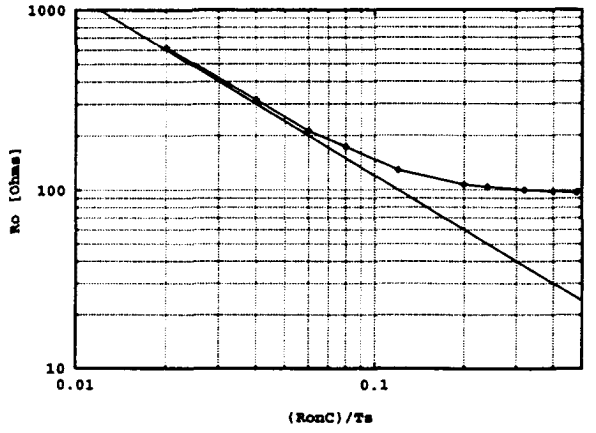

Figure 10: Output resistance limit $R_o = 6/CT_s$, and the R_o values found by simulation of the SC converter in Fig. 2, as functions of $R_{on}C/T_s$, $R_{on} = 2\Omega$, $C = 1\mu$F.

formulation is used to determine efficiently the dc conversion ratio of any SC converter, and also as a tool to derive the general SC converter properties.

For a given number of capacitors k, the maximum attainable conversion ratio is given by the k^{th} Fibonacci number. The number of switches required for the Fibonacci realization is also determined, and is equal to $3k - 2$. Fibonacci SC converters offer the highest possible step-up or step-down dc conversion ratio for a given number of components in a two-phase converter, but the capacitor voltages are unequal.

The fact that a range of distinct dc conversion ratios is available with a given number of capacitors can be utilized to construct SC converters with on-line adjustable voltage gain. Such converters can maintain output voltage regulation and high conversion efficiency over a wide range of input voltage variations. Feedforward or feedback control techniques can be applied.

It is shown how limits on the SC converter output resistance and efficiency can also be found from the converter topological description. These results can be used for initial comparison and selection of the converter best suited for a given application.

References

[1] J. S. Brugler, "Theoretical performance of voltage multiplier circuits," IEEE Journal of Solid-State Circuits, June 1971.

[2] P. M. Lin, L. O. Chua, "Topological generation and analysis of voltage multiplier circuits," IEEE Trans. on Circuits and Systems, CAS-24, No. 10, October 1977.

[3] L. Malesani, R. Piovan, "Theoretical performance of capacitor-diode voltage multiplier fed by a current source," IEEE Trans. on Power Electronics, Vol. 8, No. 2, April 1993.

[4] A. Lamantia, P. G. Maranesi, L. Radrizzani, "Small-signal model of the Cockcroft-Walton voltage multiplier," IEEE Trans. on Power Electronics, Vol. 9, No. 1, January 1994.

[5] F. Ueno, T. Inuoe, I. Oota, and I. Harada, "Emergency power supply for small computer systems," IEEE ISCAS, 1991, pp. 1065-1068.

[6] F. Ueno, T. Inuoe, I. Oota, and I. Harada, "Power supply for electroluminescence aiming integrated circuits," IEEE ISCAS, 1992, pp. 1057-1060.

[7] S. V. Cheong, H. Chung, and A. Ionovici: Inductorless DC-to-DC Converter with High Power Density, IEEE Tran. on Industrial Electronics, Vol.41, No.2, April 1994.

[8] K. D. T. Ngo, R. Webster, "Steady-state analysis and design of a switched-capacitor DC-DC converter," IEEE PESC, 1992 Record.

[9] W. S. Harris, K. D. T. Ngo, "Operation and design of a switched-capacitor DC-DC converter with improved power rating," IEEE APEC, 1994.

[10] T. Umeno, et.al. "A new approach to low ripple-noise switching converters on the basis of switched-capacitor converters," IEEE ISCAS, 1991, pp. 1077-1080.

[11] M. S. Makowski, "On topological assumptions on PWM converters – a re-examination," IEEE PESC, 1993 Record.

[12] D. Zhou, A. Pietkiewicz, S. Ćuk, "A three-switch high-voltage converter," IEEE APEC, 1995 Proc., pp. 283-289.

[13] M. S. Makowski, "On Topological Synthesis of PWM DC-DC Power Converters, Ph.D. Thesis, Technical University of Gdańsk, Poland, November 1994.

[14] R. J. Dirkman, "Generalized state-space averaging," IEEE PESC, 1983 Record, pp. 283-294.