technical note

Philips Magnetic Products

25 Watt DC/DC converter using integrated Planar Magnetics

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25 Watt DC/DC converter using integrated Planar Magnetics

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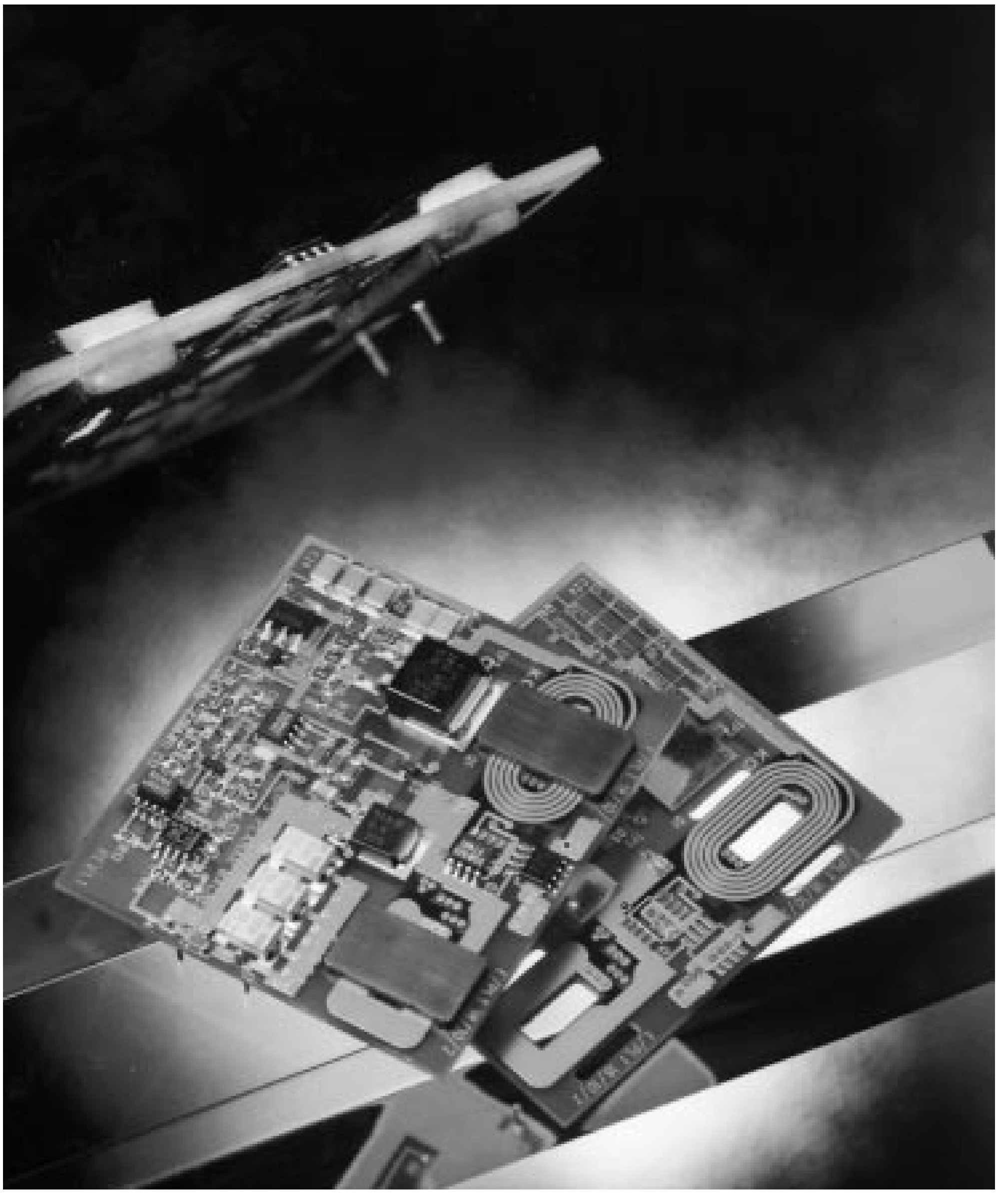


25 Watt DC/DC converter using integrated Planar Magnetics
(designed in cooperation with PEI Technologies, Ireland)

Introduction

Planar magnetics are an attractive alternative to conventional core shapes when a low profile of magnetic devices is required. Basically this is a construction method of inductive components whose windings are fabricated using printed circuit tracks or copper stampings separated by insulating sheets, or constructed from multilayer circuit boards. These windings are placed in low profile ferrite EE-or E/PLT-core combinations. Planar devices can be constructed as stand alone components or integrated into a multilayer board with slots cut to accept the ferrite E-core (fig.1).

The aim of this demonstration board is to demonstrate the capability of Philips' planar E cores (see Data Handbook MA01). One of these cores is used in the design of a high frequency 25 W DC/DC converter. A 6 layer PCB is used to facilitate the integration of the transformer and output inductor windings into the multilayer PCB structure.
The board demonstrates the advantages over standard wire wound solutions in terms of cost, size, simplicity and reliability. It will also show that the electrical performance of the converter is excellent.

Features such as input filtering, output voltage and long term short circuit protection have been omitted from the design as the use of planar magnetics does not have an impact on these features.

The chosen topology is the forward converter with resonant reset. A basic description of the operation of a forward converter can be found in most textbooks on switch-mode power supplies.

Converter description

The schematic for the forward converter with resonant reset is shown on page 10. This converter design differs from a standard design in two ways:

- It employs a resonant reset technique to reset the power transformer, T1

- It uses synchronous rectifiers Q2 and Q3, low voltage, low Rds (on) MOSFETS on the secondary side of the transformer for rectification.

In a standard forward converter a separate winding can be used to reset the transformer to ensure the flux returns to zero on each cycle. The resonant reset technique allows for the elimination of this winding which is an attractive benefit when using planar magnetics. Reset is achieved during the off time by imposing a resonant voltage on the primary winding using parasitic circuit elements.

The frequency of this resonance is approximately equal to:

$$f_{res} \approx \frac{1}{2\pi\sqrt{L_p \cdot C_{Q1}}}$$

where L_p is the transformer primary inductance and C_{Q1} is the MOSFET parasitic capacitance.

The advantage of this technique is that it iseasy to implement at low cost. The disadvantage is that it is a lossy solution compared to soft switching techniques. This loss is not dramatic at voltages lower than 100V, and will lead to a decrease in efficiency of approximately 1% at 48V input and 2% at 72V input voltage.

The second difference in comparison with a conventional converter is the implementation of synchronous rectification. This is cost competitive with Schottky diodes at a current rating of less than 10A.

At 48V input, synchronous rectification will increase the efficiency by approximately 3% to 6% depending on the Rds (on) of the MOSFETS used and the switching frequency. Low Rds(on) MOSFETS increase efficiency but are more expensive.

Increased frequency will reduce the efficiency of the synchronous rectifiers due to the charging of the input capacitance once every cycle.

To keep the circuit simple and low cost. the synchronous rectifiers are self driven. This means that they are driven directly with the voltage from the transformer secondary. This is not the most efficient solution particularly when the ‘dead’ time is large as at high input voltage.
To counteract this, diode D1 is added in parallel to Q3. This diode will conduct during the ‘dead’ time.

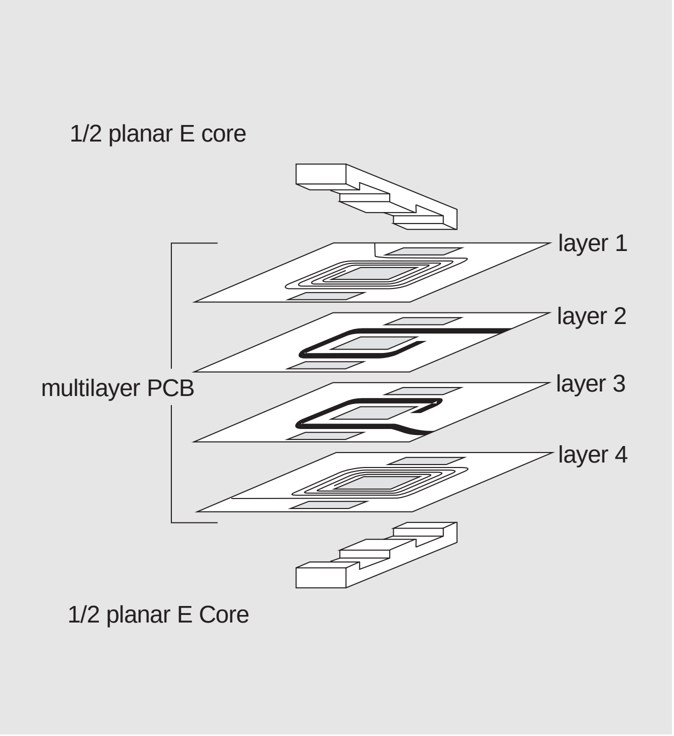


Fig. 1 Exploded view of a PCB transformer

Converter specification

Low-profile DC/DC converter (25 W)
Featuring:
-planar ferrite E cores
-multilayer FR4 printed circuit board(6layers)
-integrated windings for transformer and output choke.

Input voltage	36-72V
Max input current (no load)	50 mA
Max input current (full load)	620 mA
Output voltage	5VDC ± 1%
Output current (min)	0 A
Output current (max)	5 A
Output ripple and noise	50 mVpp
Efficiency	85 % typ
Line regulation	± 0.1 %
Load regulation	± 1 %
Isolation voltage	500 VDC
Switching frequency	420 kHz
Operating temperature-	25 °C to50 °C

All Specifications are typical at nominal line voltage(48V), full load and 25 °C unless otherwise stated.

Input capacitor required for operation: 10 μF , 100V.

Pin	Pin connection
J1	Vin +
J2	Vin -
J3	+ Output
J4	- Output

Dimensions: 60 × 57 × 6 mm

Performance of the converter

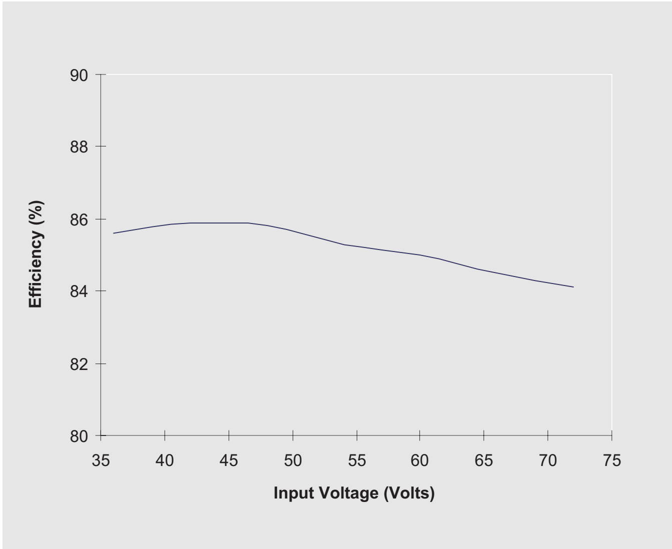


Fig.2 Efficiency as a function of input voltage at full load

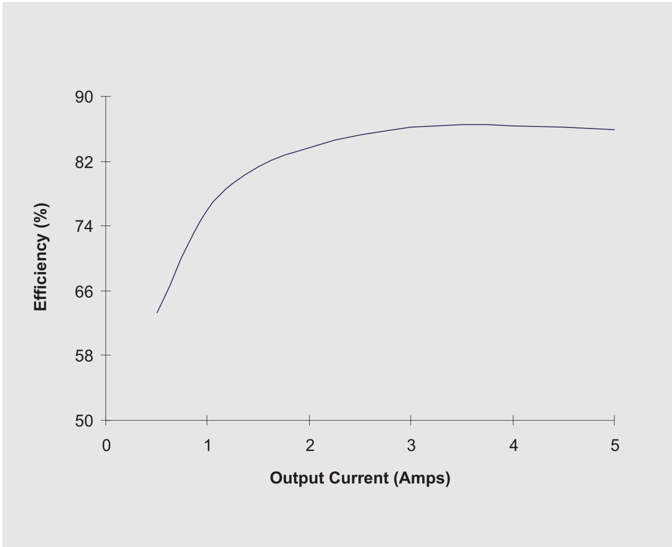


Fig.3 *Efficiency as a function of output current (V_{in}=48V)*

Oscillograms

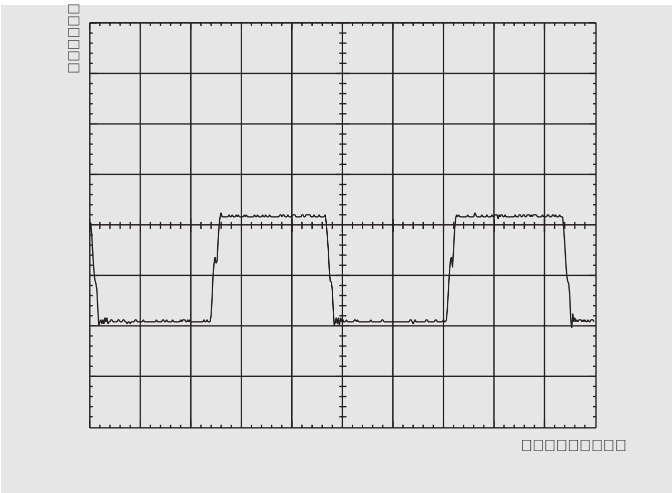


Fig.4 Primary MOSFET (Q1) gate voltage(TP6)

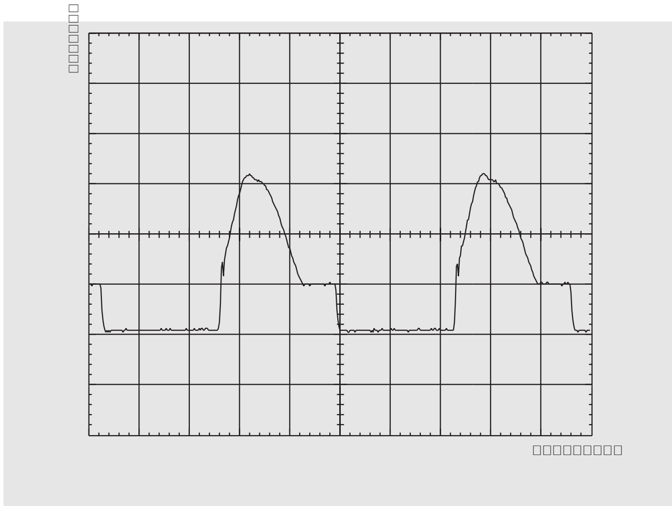


Fig.5 Primary MOSFET (Q1) drain voltage(TP2)

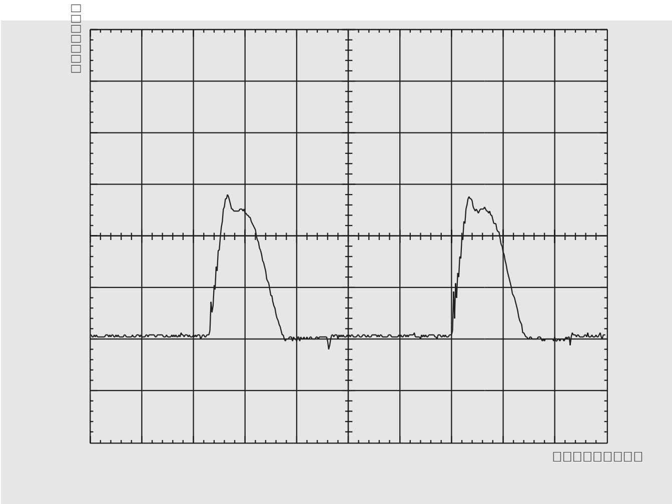


Fig.6 Synchronous rectifier (Q2) drain voltage (TP3)

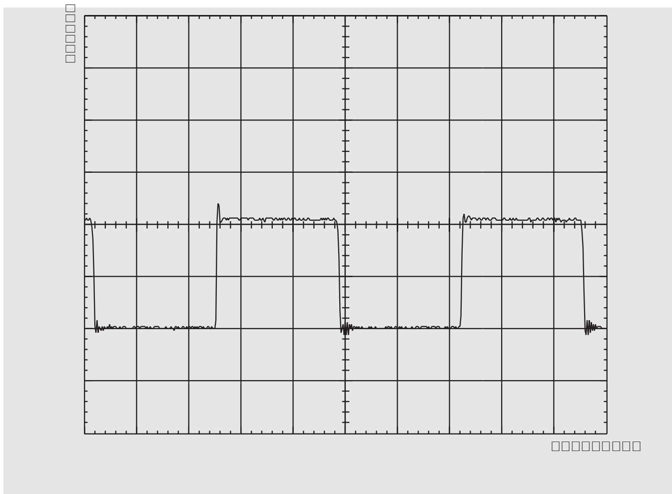


Fig.7 Synchronous rectifier (Q3) drain voltage (TP4)

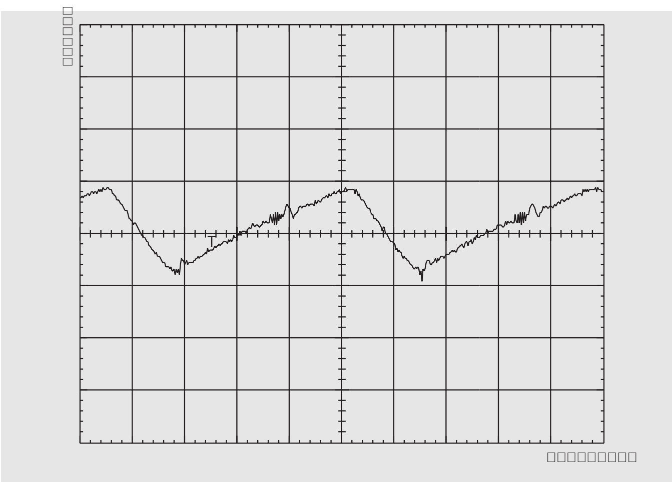


Fig.8 Control IC oscillator (TP5)

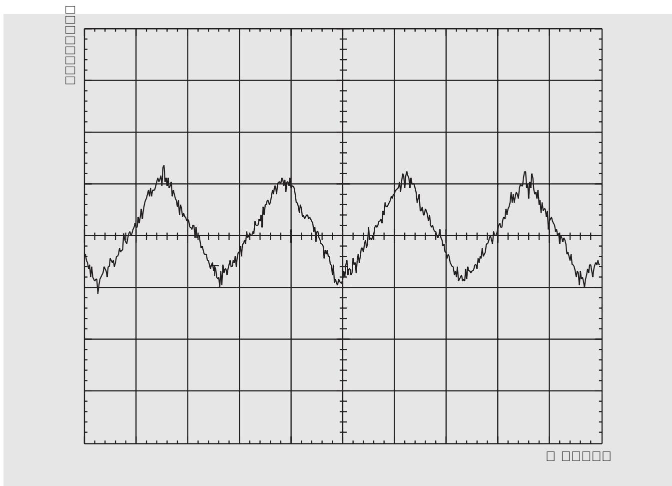


Fig.9 Output voltage ripple and noise (bandwidth 20 Mhz)

Design of planar magnetics

Transformer design (T1)
In designing the power transformer the optimisation of a number of design parameters has been investigated. These are discussed here.

The primary to secondary turns ratio should be approximately 4.5:1 to guarantee a secondary voltage of 5V at a minimum input voltage of 36V using a forward converter operating at a maximum duty cycle of 70%. Three turns ratios have been investigated (4:1, 4.5:1, 5:1) in order to determine the minimum transformer losses. The number of primary turns has been selected on the basis of a trade off between minimising core losses and copper losses. Consideration was also given to being able to accommodate the transformer windings in a 6-layer PCB construction. Hence three values of primary turns were investigated (5, 8 and 9 turns).

Copper losses in the transformer have been calculated for DC only, which appears to be accurate enough for this application. Methods to predict AC losses will be treated in a.seperate application note on the winding design for planar transformers.

Ferrite core: E18/4/10-3F3 + PLT18/10/2-3F3

Turns ratio	9:2	8:2	5:1
Track width (mm)			
primary	1.0	1.0	2.0
secondary	4.5	4.5	4.5
Number of PCB layers			
primary	3 or 4	3 or 4	3 or 4
econdary	2	2	1
auxiliary	1 or 2	1 or 2	1 or 2
Total	6 to 8	6 to 8	5 to 7
DC resistance (mΩ)			
primary	110	110	30
secondary	6	6	3
Primary inductance (µH)	243	192	75

table1

Note 1: 2 oz copper (70 µm) is used in all cases.

The primary windings can be split in such a manner that the secondary is embedded between two primary windings. This technique, known as sandwiching or interleaving, reduces leakage inductance.

Transformer losses
Losses in the ferrite core and windings are estimated for a switching frequency of 400 kHz and an output current of 5 A.

Turns ratio	9:2	8:2	5:1
Primary current	0.8	0.85	0.75
Primary resistance	0.11	0.11	0.03
Primary loss	0.07	0.08	0.017
Secondary current	3.61	3.39	3.77
Secondary resistance	0.006	0.006	0.003
Secondary loss	0.08	0.07	0.043
Total copper loss	0.15	0.15	0.06
Core loss	0.56	0.77	2.1
Total losses (W)	0.71	0.91	2.15

table 2

The lowest overall losses are predicted for the turns tatio of 9:2, which is chosen for the design.

Optimisation of switching frequency
The choice of a switching frequency close to 400 kHz follows from an estimation of the total loss balance between semiconductors and magnetics. A higher frequency increases the loss in the switches, but ferrite losses are lower. A higher frequency also reduces the ripple current in the output inductor.

f (kHz)	Vin (V))	Semicond. losses (W)	Magnetics losses (W)	Total (W)
300	36	2.11	1.34	3.45
	48	2.38	1.27	3.65
	72	3.19	1.19	4.38
400	36	2.13	1.20	3.33
	48	2.52	1.13	3.65
	72	3.58	1.05	4.63
500	36	2.33	1.16	3.49
	48	2.67	1.09	3.76
	72	3.98	1.01	4.99
600	36	2.61	1.22	3.83
	48	2.84	1.15	3.99
	72	4.39	1.07	5.46
700	36	3.05	1.22	4.27
	48	3.01	1.15	4.16
	72	4.81	1.07	5.88

table 3

Design of planar inductor (L1)

The peak-to-peak ripple current in the output inductor is designed to be approximately 20% of the full load output current for the nominal input voltage of 48V.

The inductance to achieve this can be calculated from the formula:

$$L = \frac{V_{sec} \cdot t_{on}}{\Delta I} = \frac{10.66 \; \cdot \; 1.38\ \mu s}{1} = 14.7\ \mu H$$

where

V_{sec} = Peak secondary voltage = Ns /Np . Vin

= 2/9 . 48 V = 10.66 V

t_{on} = Primary MOSFET on time = $1.38 \cdot 10^{-6}$s

ΔI = Inductor ripple current

So ideally the inductance value should be 14.7 μH.
With 5 turns this means an inductance per turn of:
However, a check on the flux density shows that with a peak current of 5.5 A this is too high, since:

$$A_L = \frac{L}{N^2} = \frac{14.7 \cdot 10^{-6}}{25} = 588\ nH$$

Using the standard core E18/4-3F3-A315-P, a check on the flux density shows that with a peak current of 5.5A, the maximum value is:

$$B_{max} = \frac{N \cdot I_p \cdot A_L}{A_e} = \frac{5 \cdot 5.5 \cdot 588 \cdot 10^{-9}}{39.5 \cdot 10^{-6}} = 409\ mT$$

where

Ip = Peak inductor current

B. = Maximum flux density

N = Number of turns

A_L = Inductance per turn

A_e = Cross sectional area of core

This maximum flux density of 388 mT is excessive for 3F3 material. To reduce the maximum flux density using the same core, the air-gap needs to be increased. Consequently, the maximum flux density is set to 300 mT. Using this figure and working backwards to calculate the required A_L with N=5 turns and Ip=5.5 A gives:

$$A_L = \frac{B \cdot A_e}{N \cdot I_p} = \frac{0.3 \cdot 39.5 \cdot 10^{-6}}{5 \cdot 5.5} = 431\ nH$$

$$L = A_L \cdot N^2 = 431 \cdot 10^{-9} \cdot 25 = 10.8\ \mu H$$

The increased ripple current will cause an increase in ΔB which will lead to somewhat higher losses in the output inductor.

Output capacitor design

Output ripple voltage is calculated using the formula:

$$\Delta Vo = \frac{1}{C} \int dI_L\, dt + \Delta I_L \cdot ESR$$

where ΔI_L is the ripple current in the output inductor and ESR is the equivalent series resistance of the output capacitors.

The first term is much smaller than the second due the high capacitance of the output capacitors so that the ripple voltage can be expressed as:

$$\Delta Vo = \Delta I_L \cdot ESR$$

The worst case will be at maximum input voltage.

Vsec = 2/9 • 72V = 16V

L = 10.8 μH

Maximum ripple current follows from:

$$\Delta I_{max} = \frac{V_{sec} \cdot t_{on}}{L} = \frac{16 \cdot 0.92\ \mu s}{10.8 \cdot 10^{-6}} = 1.35\ A$$

For a ripple voltage of less than 40 mV, the equivalent ESR should be less than 30mΩ. The capacitors chosen meet this requirement.

PCB layout

The multilayer FR4 PCB with 70 µm of copper comprises all windings of the transformer and output inductor. These windings are divided over the separate layers in the following way:

transformer	
primary (9turns):	-5 turns in layer 1
	-4 turns in layer 6
secondary (2 turns):	-1 turn in layer 2
	-1 turn in layer 5
sense (2 turns):	-1 turn in layer 3
	-1 turn in layer 4
output inductor	
	-1 turn in layer 1
	-1 turn in layer 2
	-1 turn in layer 3
	-1 turn in layer 4
	-1 turn in layer 5

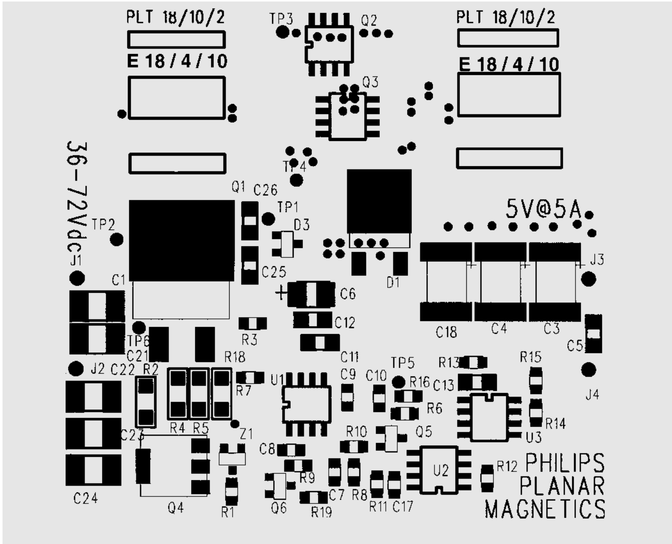


Fig.10 Component location

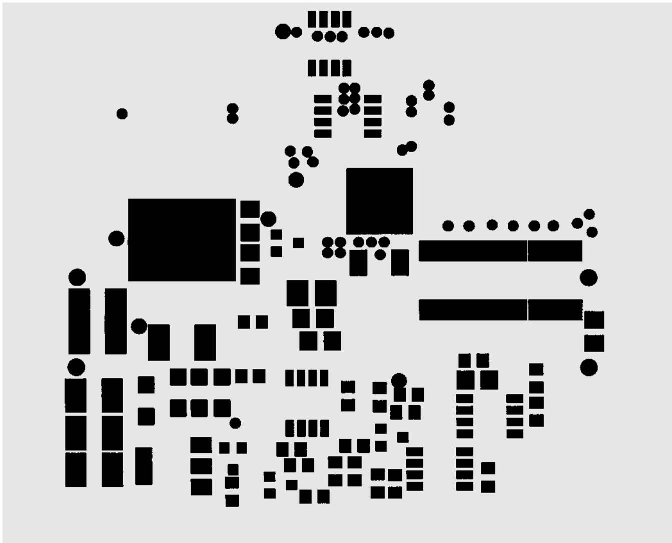


Fig.11 Solder mask layer 1

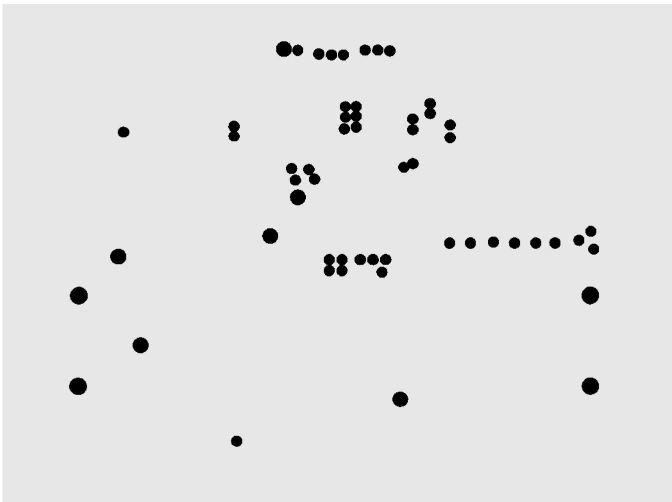


Fig.12 Solder mask layer 6

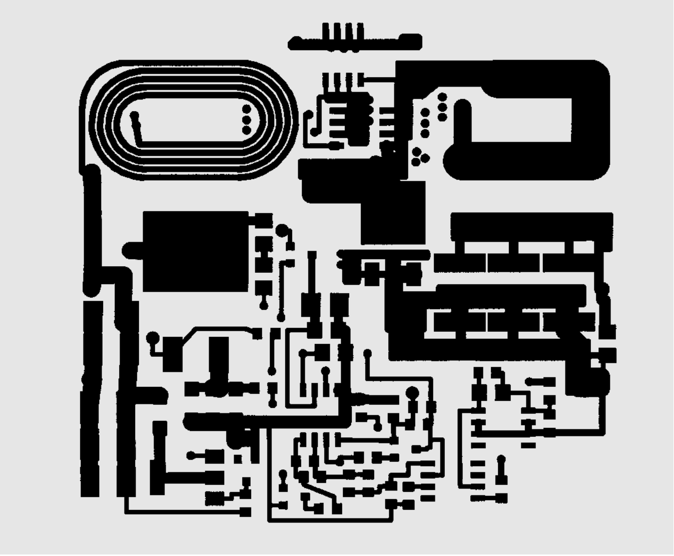


Fig.13 PCB layer 1

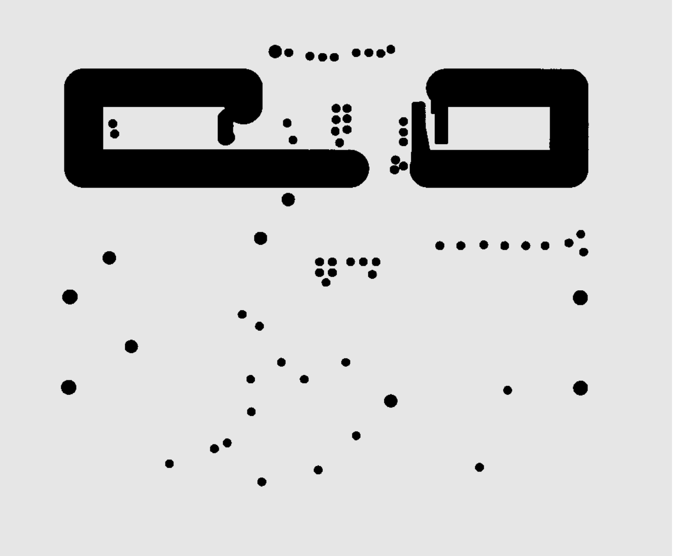


Fig.14 PCB layer 2

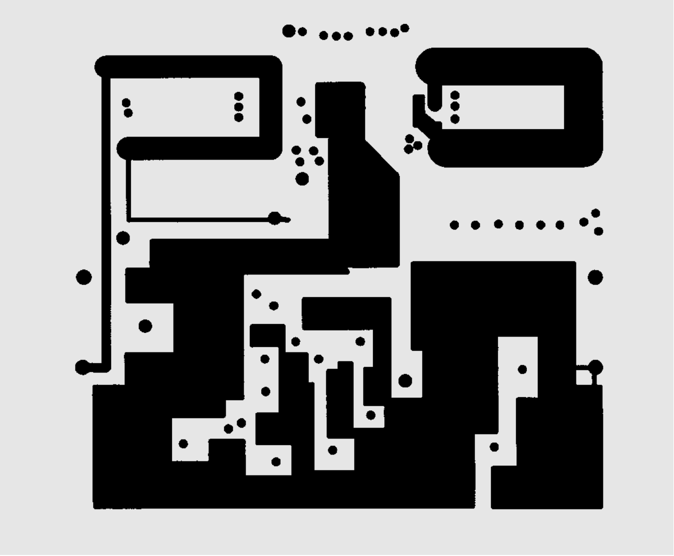


Fig.15 PCB layer 3

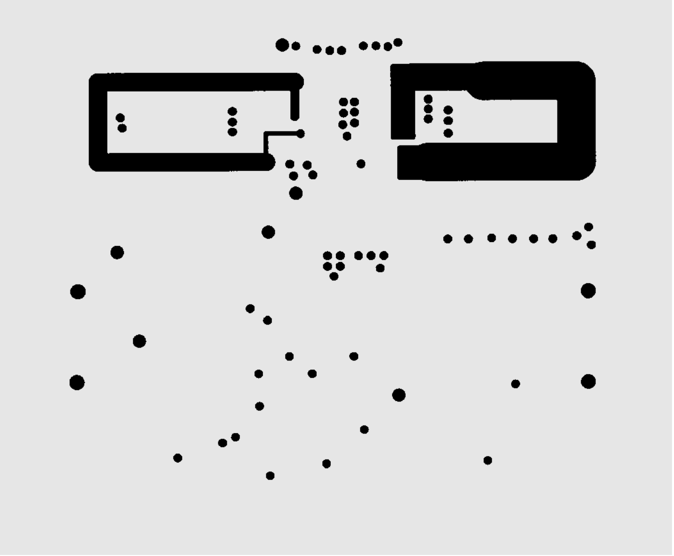


Fig.16 PCB layer 4

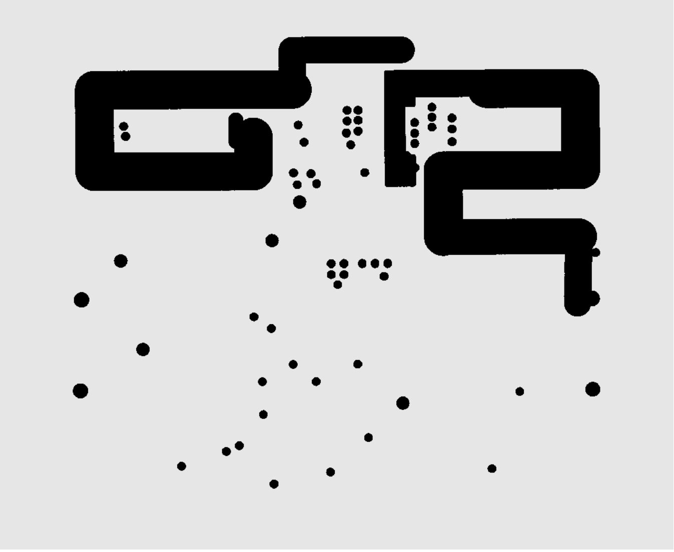


Fig.17 PCB layer 5

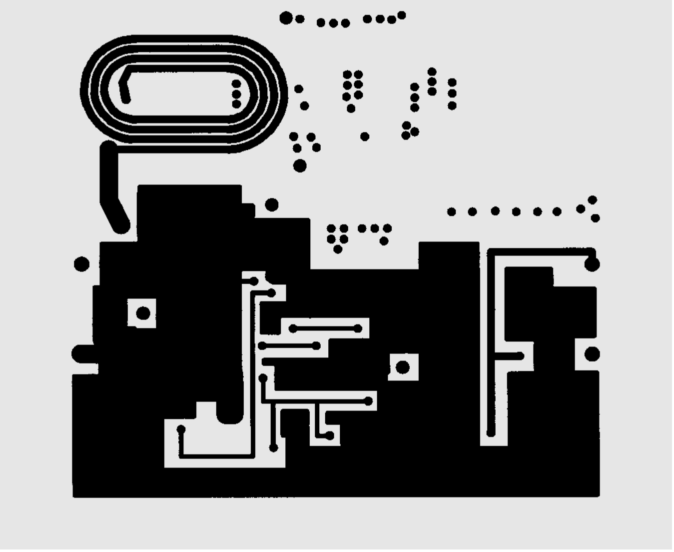
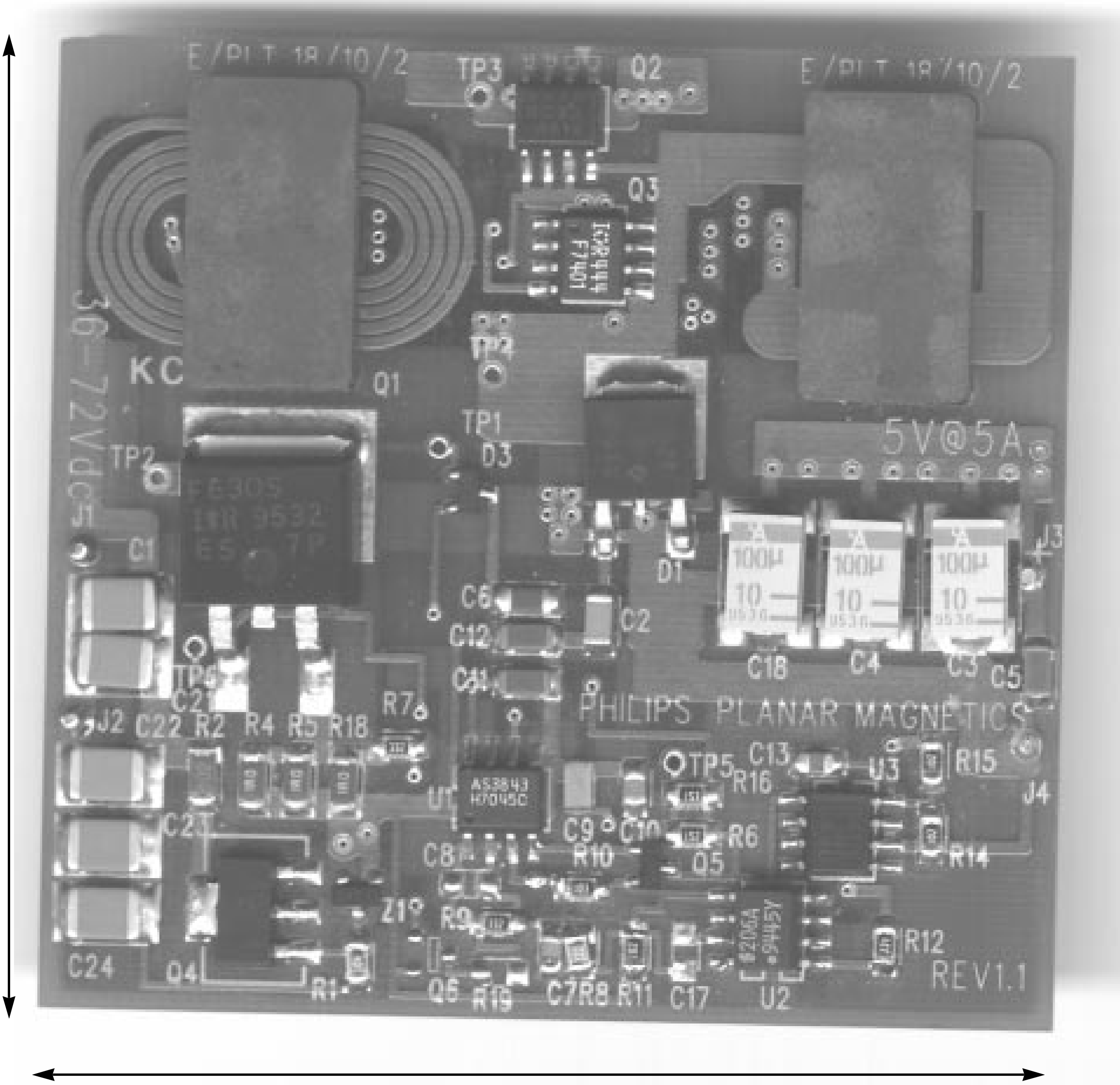


Fig.18 PCB layer 6



57 mm

60 mm

The complete converter

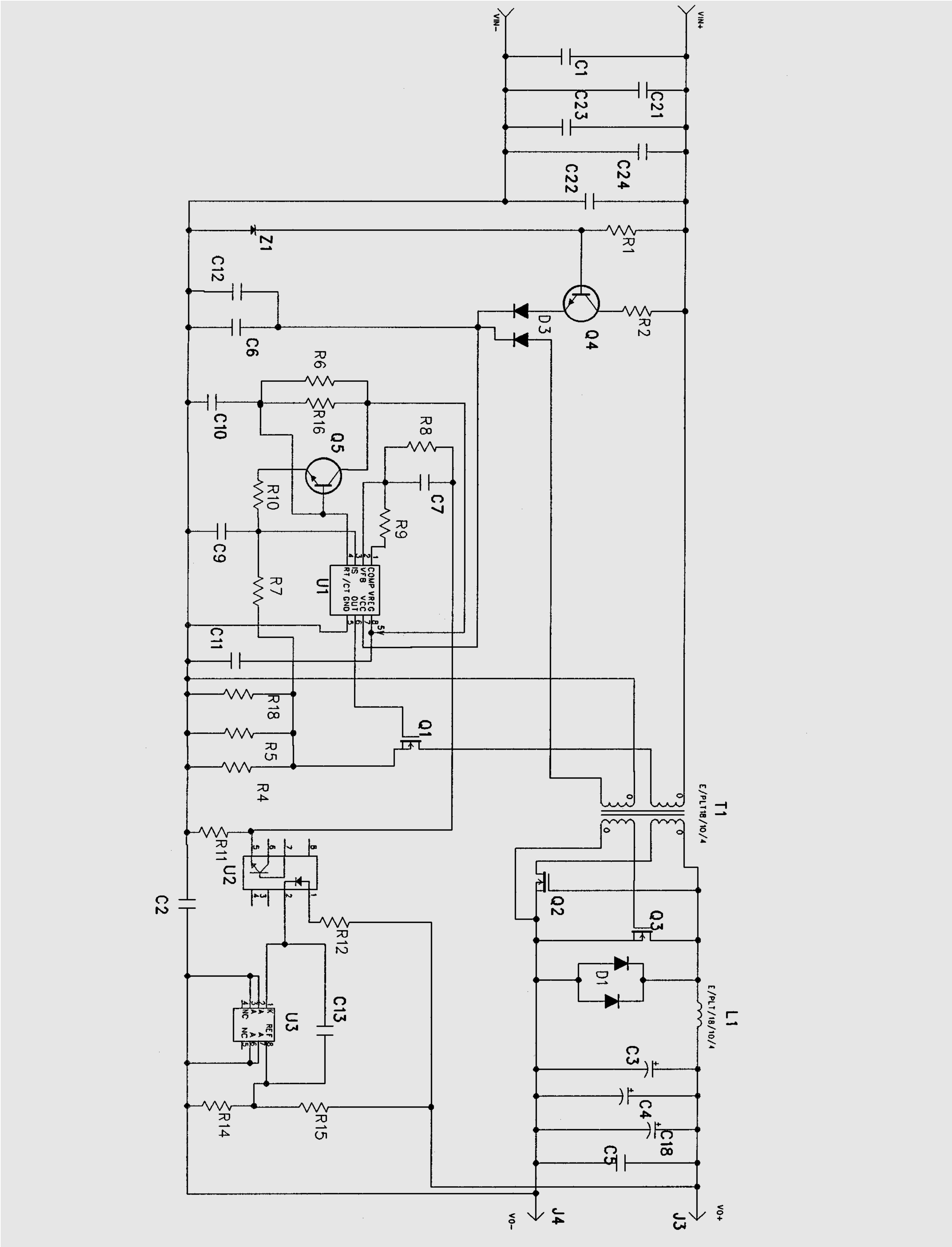


Fig.19 Circuit diagram

Components list

Reference	Part No. Series	Description	Package	Manufacturer
TR1	E18/4/10-3F3	Planar E Core		Philips
	PLT18/10/2-3F3	Plate		Philips
Ll	E18/4/10-3F3	Planar E Core		Philips
	PLT18/10/2-3F3	Plate		Philips
Ql	IRF630S	200V, 0.4Ω, MOSFET	SMD-220	I.R.
Q2	Si9410DY	30V, 30mΩ, MOSFET	SO-8	Siliconix
Q3	IRF7401	20V, 22mΩ, MOSFET	SO-8	I.R.
Q4	BCP56	80V, 1A, NPN Trans.	SOT223	-
Q5	BC848A	30V, 100mA,NPN Trans	SOT23	Philips
Dl	MBRD320	20V, 3A, Schottky Diode	D-Pak	Motorola
D3	BAV70	70V, 250mA Dual Diode	SOT-23	P.S.
Z1	BZX84C12	12V Zener Diode	SOT-23	P.S.
Ul	AS3843	PWM Controller	SO-8	Astec
U2	IL206A	opto-isolator	SO-8	Siemens
U3	T1431	Prog. Reference	SO-8	T.I.
R1	WCR	100K, 0.1W	0805	Welwyn
R2	RC-01	1K, 0.125W	1206	Philips
R4,R5,R18	RC-01	1R, 0.25W	1206	Philips
R6	WCR	1K5, 0.1W	0805	Welwyn
R8	WCR	2K2, 0.1W	0805	Welwyn
R7,R9	WCR	3K3, 0.1W	0805	Welwyn
R11,R14,R15	WCR	1K, 0.1W	0805	Welwyn
R10	WCR	10K, 0.1W	0805	Welwyn
R12	WCR	220R, 0.1W	0805	Welwyn
R16	WCR	15K, 0.1W	0805	Welwyn
C1,C21,C22, C23,C24		100nF,100V	1812	Syfer
C3,C4,C18	TAJ	100µF, 10V	D	AVX
C5,C11,C12	CG,2R	100nF, 63V	1206	Philips
C6		220nF	1206	AVX
C7,C10		22nF	0805	Philips
C9		22pF	0805	Philips
C13		15nF	0805	Kemet
C2		10nF 500V	1206	AVX

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