Analytical Loss Model of Power MOSFET

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***Abstract*—An accurate analytical model is proposed in this paper to calculate the power loss of a metal-oxide semiconductor field-effect transistor. The nonlinearity of the capacitors of the devices and the parasitic inductance in the circuit, such as the source inductor shared by the power stage and driver loop, the drain inductor, etc., are considered in the model. In addition, the ringing is always observed in the switching power supply, which is ignored in the traditional loss model. In this paper, the ringing loss is analyzed in a simple way with a clear physical meaning. Based on this model, the circuit power loss could be accurately predicted. Experimental results are provided to verify the model. The simulation results match the experimental results very well, even at 2-MHz switching frequency.**

***Index Terms*—Finite element analysis (FEA), metal-oxide semiconductor field-effect transistor (MOSFET).**

I. Introduction

IN ORDER to investigate the performance of a circuit, an accurate loss model is usually needed before the hardware is built. Based on the model, a lot of design cases are compared, which means the data could be huge. A lot of loss models have been previously proposed to achieve better accuracy and shorter simulation time. Basically, the loss model can be classified into three types. One is the physics-based model. The physical parameters of the device, such as geometry, doping density, etc., are input into the device simulation software, e.g., Medici and ISE [1], to do the finite element analysis (FEA). The simulation results match the experimental results very well. However, it is time-consuming. For instance, a simple open loop controlled Buck converter (shown in Fig. 1) at the test condition as follows: $V_{\rm in} = 12$ V, $V_{\rm o} = 1.2$ V, $I_{\rm o} = 12.5$ A, $f_{\rm s} = 1$ MHz. The high side switch is HAT2168. The low side switch is HAT2165. The driver is LM2726. It takes a workstation two days to calculate only two switching cycles. Obviously, this method is not suitable for massive data processing.

The second level is the behavior model. This method is widely used in the loss analysis because it has good trade-off between the accuracy and the simulation time. Almost every device vendor provides the device behavior model for Pspice and SABER on their websites. The device is usually described by some key parameters. However, it is still not suitable for massive data processing although its simulation speed is much faster than that of the physics-based model.

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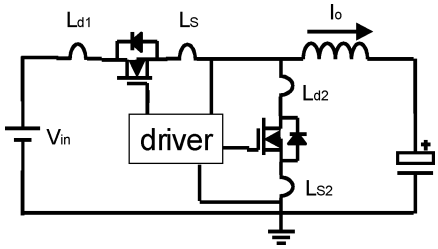


Fig. 1. Buck converter with parasitic inductors.

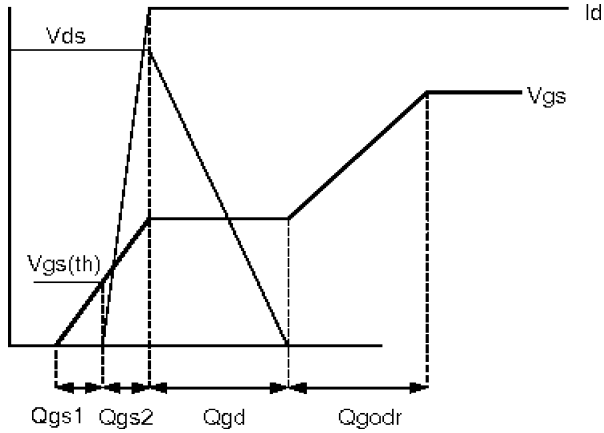


Fig. 2. Piecewise linear approximation of the conventional analytical loss model (turn-on period).

The last method is the analytical model (also called mathematical model). Based on some equivalent circuits, the loss expressions are derived. Compared to the aforementioned two methods, this method is fastest and suitable for data processing. The major challenge for this model is how to improve its accuracy.

The most simple analytical loss model [2] treats the switch turn-on and turn-off waveforms as piecewise linear (Fig. 2). It doesn't consider the source inductance and the nonlinear characteristics of the capacitors of the device. Therefore, the result normally doesn't match the experimental results very well, especially for high frequency application. Fig. 3 shows the comparison between the analytical model and the experiment. The test condition is the same as the previous case. The difference is significantly increasing as the switching frequency increases. The major reason is that the switching loss is not evaluated well.

In order to improve the accuracy of the analytical model, two important parameters should be taken into consideration: the parasitic inductors in the circuit and nonlinear capacitors of the device.

One important parameter is the common source inductor of the top switch, which is defined as the inductor shared by the power stage and driver loop and shown as $L_{\rm s}$ in Fig. 1. [3] partially addressed this issue. Based on this model, Fig. 4 illus-

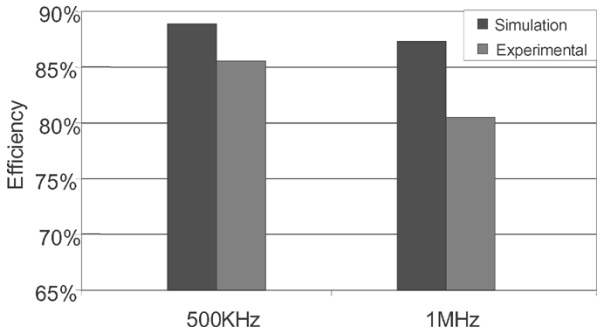


Fig. 3. Efficiency comparison between the analytical model [2] and the experimental results.

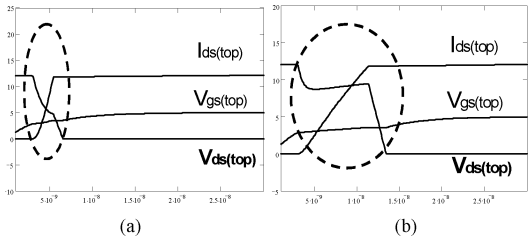


Fig. 4. Comparison between (a) without the source inductor $L_{\rm s} = 0$ and (b) with the source inductor $L_{\rm s} = 1$ nH.

trates that after $L_{\rm S}$ is considered; the commutation time dramatically increases, which significantly impacts on the switching loss. It must be considered in the analytical model. However, the model in [3] doesn't consider any ringing loss caused by the resonance between the parasitic inductors and capacitors (see Fig. 4), which is always observed in the pulse-width modulation (PWM) converters and could result in significant loss.

Another important parameter is the nonlinearity of the capacitors, which also dramatically impact the switching losses.

This paper addresses theses issues. The nonlinear capacitors and the parasitic components in the circuit are considered. In addition, the ringing loss is discussed and a simple method is proposed to calculate it. Experimental results are provided to verify the accuracy of the proposed analytical model.

II. Model of Nonlinear Capacitance of Devices

The method for modeling the nonlinear capacitors of a metal–oxide–semiconductor field-effect transistor (MOSFET) has been explained in some microelectronics textbooks. This method is also valid for low-voltage rating MOSFETs [4].

The input parameters of the model are the input capacitance $C_{\rm iss}$, the output capacitance $C_{\rm oss}$, and the reverse transfer capacitance C_{rss} at 16-V drain-source voltage and $C_{\rm oss}$, C_{rss} at 1-V drain-source voltage. All of them can be taken from the datasheet. Then, the gate-source capacitance at 16-V drain–source voltage is given by

$$C_{gs} = C_{\rm iss\_16\ V} - C_{rss\_16\ V}. \tag{1}$$

Normally, C_{gs} can be treated as a constant. The drain–source capacitances at 16-V and 1-V are

$$C_{ds\_16\ V} = C_{\rm oss\_16\ V} - C_{rss\_16\ V}, \text{ and} \tag{2}$$

$$C_{ds\_1\ V} = C_{\rm oss\_1\ V} - C_{rss\_1\ V}. \tag{3}$$

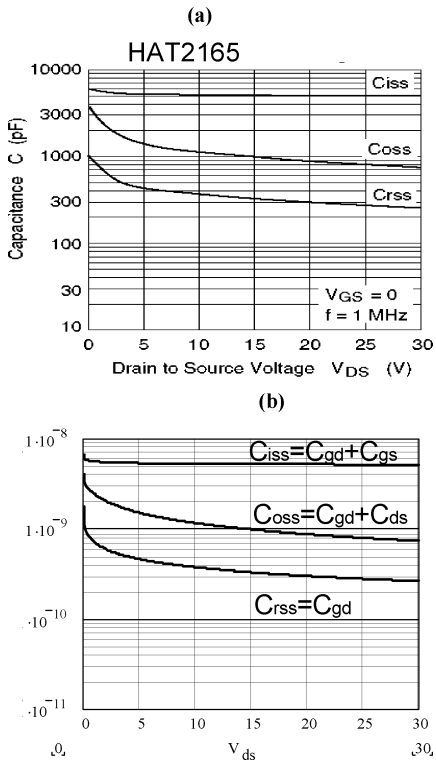


Fig. 5. Nonlinear capacitance comparison between (a) the data from datasheet and (b) data obtained from the proposed model.

The general drain–source capacitance can be expressed as

$$C_{ds} = \frac{C_{j1}}{\sqrt{1 + \frac{V_{ds}}{\Phi_1}}}. \tag{4}$$

Substituting (2) and (3) into (4), respectively, two equations are found. Based on these equations, the coefficients C_{j1} and Φ_1 can be solved.

The same method can be applied to the Miller capacitor, which is a gate–drain capacitor. The general gate–drain capacitance is expressed as

$$C_{gd} = \frac{1}{\frac{1}{C_{gd\_0\ V}} + \frac{V_{ds}^x}{C_{j2}}}$$

$$\text{where, } C_{gd\_0\ V} = \frac{Q_{gs(total)\text{-}5\ V}}{5} - C_{gs}. \tag{5}$$

And the coefficient x and C_{j2} can be calculated based on

$$C_{rss\_16\ V} = \frac{1}{\frac{1}{C_{gd\_0\ V}} + \frac{16^x}{C_{j2}}} \tag{6}$$

$$C_{rss\_1\ V} = \frac{1}{\frac{1}{C_{gd\_0\ V}} + \frac{1^x}{C_{j2}}}. \tag{7}$$

Fig. 5(a) is the nonlinear capacitors' curves captured from HAT2165 datasheet and Fig. 5(b) shows the curves got from the model. They match very well. After the relationship between the nonlinear capacitance and $\rm V_{ds}$ is established, more accurate losses model can be obtained.

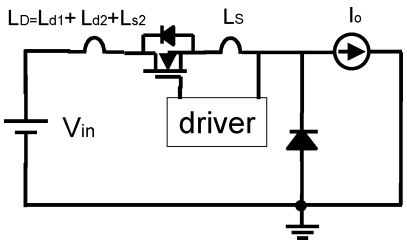


Fig. 6. Simplified equivalent circuit for buck converter during the commutation period.

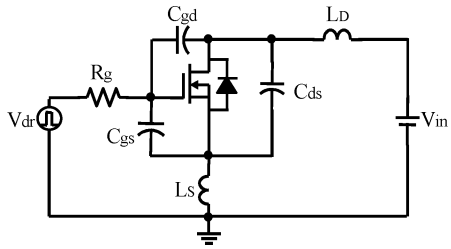


Fig. 7. Simplified equivalent circuit for the main transition period.

III. Model of Devices' Behaviors in Circuit

After the nonlinear capacitors of the devices are modeled, the next step is to analyze the impact of the parasitic inductance in the circuit, especially the common source inductance $L_{\rm s}$. The most difficult part of the device loss analysis is the switching loss and ringing loss compared to the conduction loss and gate drive loss. Therefore, the majority of the paper focuses on deriving the expressions for the switching loss and ringing loss.

A simple synchronous Buck converter is taken as an example. In order to avoid the shoot through problem, the gate signals between the top switch and bottom switch normally have a certain dead time, during which the body diode conducts current. It is reasonable to use a freewheeling diode instead of a MOSFET as the bottom switch for the switching loss analysis. The diode forward drop voltage is assumed to be 0 V for the convenience. And the inductor current is treated as a current source $I_{\rm o}$ without ripple because the commutation time is sufficiently small that the inductor current doesn't apparently change during this period.

Based on these assumptions, the buck converter in Fig. 1 is redrawn in Fig. 6. The parasitic inductors, L_{d1}, L_{d2}, and $L_{\rm s2}$, are combined as L_D. This equivalent circuit is valid as long as the freewheeling diode conducts current. Actually, the simplified circuit in Fig. 6 is also suitable for other topologies, such as boost, buck-boost etc., to analyze the device behaviors during the commutation period.

A. Turn-On Period

As discussed in [3], the MOSFET turn-on transition follows at least four distinct phases. In this paper, the analysis is also divided into four phases. However, the common source inductance $L_{\rm s}$ and the nonlinear capacitors are taken into consideration. Furthermore, the current ringing and diode reverse recovery phenomenon are analyzed.

1) Delay Period: When the gate voltage V_{dr} is added, the resultant gate current charges the input capacitor $C_{\rm iss}$, which is the combination of C_{gs} and C_{gd}. The gate voltage exponentially charges up toward drive voltage amplitude V_{dr} with a time constant τ_G

$$\tau_G = R_G\left(C_{gs}+C_{gd}\right) \tag{8}$$

$$v_{gs\_ondelay}(t) = V_{dr}\left(1-e^{-t/\tau_G}\right). \tag{9}$$

This period ends when the gate–source voltage reaches the threshold voltage. At this phase, the status of the power stage doesn't change at all because the gate voltage is below the threshold voltage.

2) Main Transition Period: During the main transition period, both the drain current and the drain–source voltage change. However, as mentioned in [3], the variation of one dominates that of the other in most circuits. For example, in a low-input voltage buck converter, the voltage normally collapses to zero before the current reaches the steady-state value. The simplified circuit in Fig. 6 is redrawn in Fig. 7 with the inherent components of the MOSFET and the parasitics.

Based on this equivalent circuit, the circuit equations are expressed by (10)–(13) using Laplace form

$$v_{gd}(s) = \frac{\frac{(V_{dr}-v_{gs}(s)-sL_{\rm s}(i_G(s)+i_D(s)))}{R_G} - sC_{gs}v_{gs}(s)}{sC_{gd}} \tag{10}$$

$$v_{ds}(s) = V_{\rm in} - sL_D i_D - sL_{\rm s}\left(i_D(s)+i_G(s)\right) \tag{11}$$

$$i_G(s) = sC_{gd}v_{gd}(s) + sC_{gs}v_{gs}(s) \tag{12}$$

$$v_{gs}(s) = v_{gd}(s) + v_{ds}(s). \tag{13}$$

Compared to the equations in [3], the common source inductor $L_{\rm s}$ is taken into consideration.

Based on (10)–(13), the gate–source voltage is derived as follows:

$$\begin{aligned} v_{gs}(s) &= \frac{V_{dr}}{s^2\tau_m\tau_{G'}+s\tau_{G''}+1}, \\ \text{where } \tau_m &= g_{fs}L_D,\ \tau_{G'} = C_{gd}R_G, \\ \tau_{G''} &= \left(C_{gd}+C_{gs}\right)R_G + g_{fs}L_S. \end{aligned} \tag{14}$$

g_{fs} is the forward transconductance of a MOSFET. It is usually nonlinear. In order to bring out a clear physical meaning, a simplifying assumption is made that the g_{fs} is a constant.

Transferring (14) back into time domain gives either sinusoidal or exponential solutions, depending on the relative magnitudes of $\tau_{G''}$ and $\tau_{G'}\tau_m$. The sinusoidal solutions occur when $\tau_{G''}^2 < 4\tau_{G'}\tau_m$

$$v_{gs}(t) = V_{dr} - \left(V_{dr}-V_{th}\right)e^{-t/\tau_a}\left(\cos\left(\omega_a t\right) + \frac{1}{\omega_a\tau_a}\sin\left(\omega_a t\right)\right)$$

where

$$\tau_m = \frac{2\tau_m\tau_{G'}}{\tau_{G''}},\ \omega_a = \sqrt{\frac{1}{\tau_m\tau_{G'}} - \left(\frac{\tau_{G''}}{2\tau_m\tau_{G'}}\right)^2}. \tag{15}$$

The drain current and drain-source voltage are

$$\begin{aligned} i_d(t) &= g_{fs}\left(v_{gs}(t)-V_{th}\right) \\ &= g_{fs}(V_{dr}-V_{th})\left(1-e^{-t/\tau_a}\left(\cos\left(\omega_a t\right)+\frac{1}{\omega_a\tau_a}\sin(\omega_a t)\right)\right) \end{aligned} \tag{16}$$

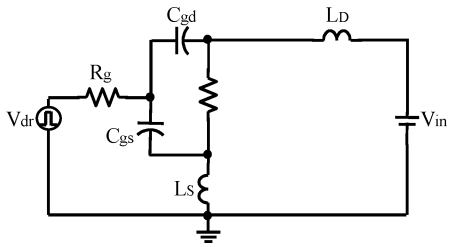


Fig. 8. Simplified equivalent circuit for the remaining transition period.

and

$$v_{ds}(t) = V_{\text{in}} - (L_S + L_D)\frac{di_d(t)}{dt} = V_{\text{in}} - g_{fs}(V_{dr} - V_{th})\omega_a (L_S + L_D) e^{-t/\tau_a} \times \left(1 + \left(\frac{1}{\omega_a \tau_a}\right)^2\right) \sin(\omega_a t). \quad (17)$$

The exponential solutions occur when $\tau_{G''}^2 > 4\tau_{G'}\tau_m$

$$v_{gs}(t) = V_{dr} - (V_{dr} - V_{th})\frac{e^{-t/\tau_b}\tau_b - e^{-t/\tau_c}\tau_c}{\tau_b - \tau_c}$$
$$\text{where } \tau_b = \frac{2\tau_m\tau_{G'}}{\tau_G - (\tau_{G''}^2 - 4\tau_m\tau_{G'})^2}, \tau_c = \frac{2\tau_m\tau_{G'}}{\tau_G - (\tau_{G''}^2 - 4\tau_m\tau_{G'})^2}. \quad (18)$$

The drain current and drain–source voltage are

$$i_d(t) = g_{fs}(V_{dr} - V_{th})\left(1 - \frac{e^{-t/\tau_b}\tau_b - e^{-t/\tau_c}\tau_c}{\tau_b - \tau_c}\right) \quad \text{and} \quad (19)$$

$$v_{ds}(t) = V_{\text{in}} - g_{fs}(V_{dr} - V_{th})(L_S + L_D)\frac{e^{-t/\tau_b}\tau_b - e^{-t/\tau_c}\tau_c}{\tau_b - \tau_c}. \quad (20)$$

This period ends when either the drain–source voltage drops to zero or the drain current reaches the load current I_{o}.

Please note that the nonlinearity of the device capacitances become more and more significant as the drain–source voltage falls below the gate voltage. Therefore taking the model of Section II into account is necessary. After solving V_{ds} and i_d, the capacitance, as a function of V_{ds}, is used in the expressions.

3) Remaining Transition Period: At the end of the main transition period, one of two situations obtains. Either the drain–source voltage reaches zero or the drain current reaches the load current. If the current reaches the load current I_{o} before the drain–source voltage goes to zero, the analysis directly jumps into the next phase: the current ringing period. It will be discovered in the next section that it is more meaningful to treat this loss as a part of ringing loss.

In case of the current slower than the voltage, the equivalent circuit is shown in Fig. 8. Assuming the $R_{ds(\text{on})}$ is small enough and therefore it is not considered. Because the drain-source voltage has reaches zero, the Miller effect no longer operates. The gate current charges C_{gs} and C_{gd} in parallel. And the gate–source voltage resumes its exponential approach toward V_{dr}. The drain current rising time is determined by the loop inductance L_D and L_S. And the equations are listed as

$$v_{gs}(t) = \left(V_{dr} - V_{\text{gs\_main}} - \frac{L_S}{L_D + L_S}V_{\text{in}}\right)\left(1 - e^{-t/\tau_{G'''}}\right) + V_{\text{gs\_main}} \quad (21)$$

where $\tau_{G'''} = R_G(C_{gs} + C_{gd})$, and $V_{\text{gs\_main}}$ is the gate-source voltage at the end of the main transition period. Please note that at this stage, the gate-drain capacitance is much larger than that in the delay period.

The drain current is

$$i_d(t) = I_{\text{d\_main}} + \frac{V_{\text{in}}}{L_D + L_S}t \quad \text{where } I_{\text{d\_main}} \text{ is the drain current at the end of main transition period.} \quad (22)$$

The period ends when the drain current reaches the load current I_{o}.

4) Current Ringing Period: After the drain current reaches the load current I_{o}, the current ringing begins. A typical top switch current and voltage waveforms are shown in Fig. 9, which could be divided into three time frames. The first time frame $[t_0, t_1]$ has been analyzed in 1-1, 1-2, and 1-3. The unified equivalent circuit is shown in Fig. 6. Beyond t_1, the diode begins to recover but still cannot block voltage. At t_2, the drain current reaches its peak value and the diode begins to block voltage. The ringing isn't completely damped until t_3. The power loss derivation based on the equivalent circuits during $[t_1, t_2]$ and $[t_2, t_3]$ could be very complicated. In this paper, a simple method is introduced with very clear physical meaning.

To analyze the ringing loss, we assume the ringing can be completely damped during the top switch turn-on period, which is normally true for a converter with well-designed layout and switching frequency less than 3 MHz. With the development of the device integration, the parasitics are further reduced and the ringing could be completely damped in one switching cycle with even higher switching frequency.

The equivalent circuits for $[t_1, t_2]$ and $[t_2, t_3]$ can be unified as Fig. 10. It is pointed out that the current contributing the ringing is only the difference between drain current of the top switch i_{top} and the load current I_L. The current source I_{o} doesn't influence the oscillation at all. As long as the drain current reaches I_{o}, the branch of the current source can be taken out of consideration. Therefore, the output inductor branch is not drawn in Fig. 10.

The L_{loop} is the sum of the parasitic inductance of loop. The R_{loop} represents the ac and dc resistance. The ac resistance increases as the oscillation frequency increases. Usually, the oscillation has very high frequency, e.g., 20 $\sim$ 40- MHz. Hence, the ac resistance plays a more important role than does the DCR [5] and therefore cannot be ignored in the ringing analysis. The analysis and measurement of ac resistance is beyond this discussion, which deserves more fundamental research. $C_{\text{oss\_bot}}$

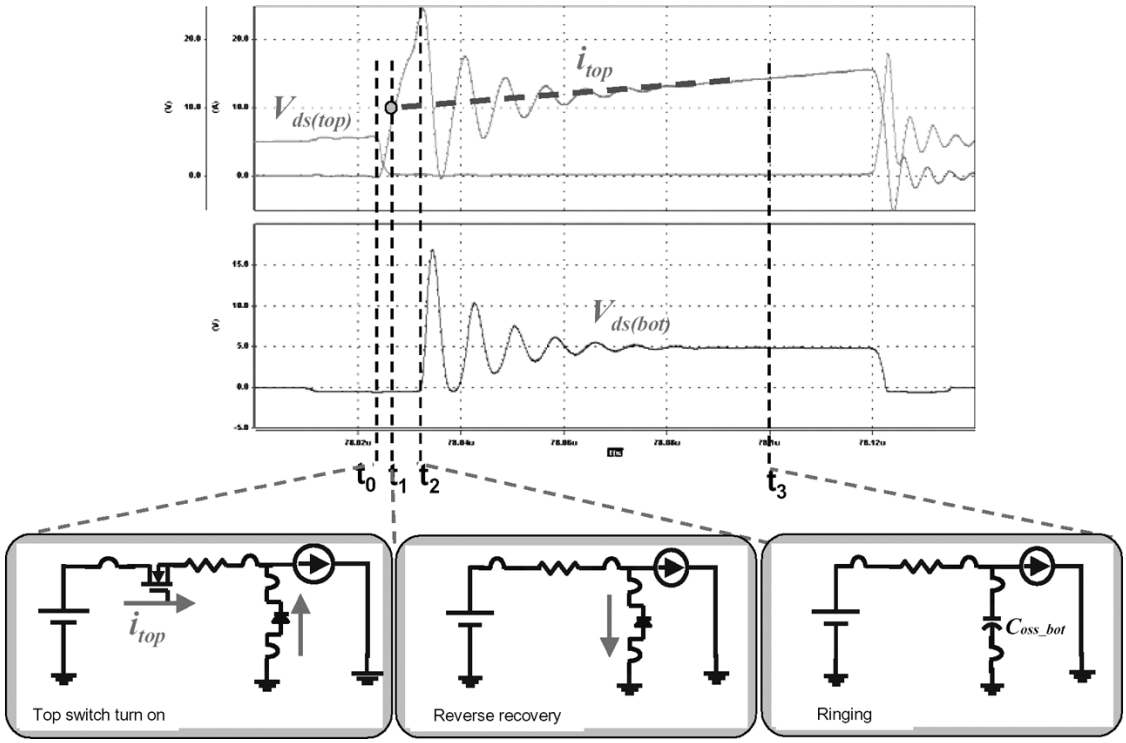


Fig. 9. Typical waveforms of a buck converter and its simplified equivalent circuits for the different periods during turn-on.

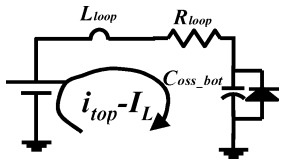


Fig. 10. Unified equivalent circuit during $[t_1, t_2]$ and $[t_2, t_3]$ shown in Fig. 9.

represents the output capacitance of the bottom switch if the synchronous rectifier is used.

During this period, the ringing energy pumped by the input source is simply expressed as

$$\begin{aligned} E_{\text{source}} &= \int_{t_1}^{t_2} V_{\text{in}} i_{\text{top}}(t)dt - \int_{t_1}^{t_2} V_{\text{in}} I_L dt \\ &= V_{\text{in}} \cdot \int_{t_1}^{t_2} \left(i_{\text{top}}(t) - I_L\right) dt \\ &= V_{\text{in}} \cdot (Q_{\text{rr}} + Q_{\text{oss\_bot}}) \end{aligned} \tag{23}$$

where Q_{rr} is the reverse recovery charge of the diode. The derivation of (23) is similar to the analysis of a gate drive circuit during the charging period. The first term is the total energy provided by the input source. The second term is the energy to the load side, which is not dissipated and therefore deducted. The difference of these two terms is the energy for reverse recovery and stored in the output capacitor of the bottom switch $C_{\text{oss\_bot}}$.

At t_3, when the ringing is fully damped, the whole circuit reaches another steady state. The only energy saved is that stored in $C_{\text{oss\_bot}}$. Therefore, the dissipated energy during the ringing period is

$$\begin{aligned} E_{\text{ring\_turnon}} &= E_{\text{source}} - \frac{1}{2} Q_{\text{oss\_bot}} V_{\text{in}} \\ &= V_{\text{in}} Q_{\text{rr}} \cdot + \frac{1}{2} Q_{\text{oss\_bot}} V_{\text{in}}. \end{aligned} \tag{24}$$

It is very interesting to find that the total ringing loss is not dependent on the loop resistance, but only V_{in}, Q_{rr}, and $Q_{\text{oss\_bot}}$. Therefore; the ringing loss can be easily derived without knowing the detailed waveforms of the voltage and current.

Another important thing that should be pointed out is that the reverse recovery loss of the diode has been treated as a part of the ringing loss. Simply multiplying the voltage and current of the diode cannot obtain the reverse recovery loss. The majority of the reverse recovery loss is not dissipated in the diode, but in the whole loop. A part of it causes additional turn-on loss of the top switch if the voltage doesn't drop to zero before the current reaches I_{o}. Another part dissipates by the loop resistance.

In order to get the ringing loss, $Q_{\text{oss\_bot}}$ and Q_{rr} should be known. Based on the nonlinear capacitor model in Section II, the $Q_{\text{oss\_bot}}$ can be easily achieved.

For Q_{rr}, it is relatively difficult because it is related to the load current I_{o} and the loop inductance L_{loop}, which determines the current slew rate during the diode's reverse recovery period. The data provided by the device vendor is normally acquired at a specific test condition. In order to achieve relatively accurate loss estimation, it is better to use a physics-based device model to simulate Q_{rr} under different conditions. For example, Fig. 11 shows the relationship between Q_{rr} and L_{loop} of HAT2165 at $I_{\text{o}} = 12.5$- A based on the ISE simulation tool. As L_{loop} is less than 2 nH, Q_{rr} is very sensitive to di/dt. As L_{loop} is greater than 3 nH, Q_{rr} is pretty much constant. This is a unique characteristic of the body diode of the low-voltage-rating ($<$ 30- V) MOSFET [6]. For today's practical layout, the loop inductance is usually larger than 3 nH.

Based on the ringing loss expression (24) and the equations in the previous three periods of turn-on, it is possible to achieve the turn-on loss and ringing loss. Please keep in mind that the re-

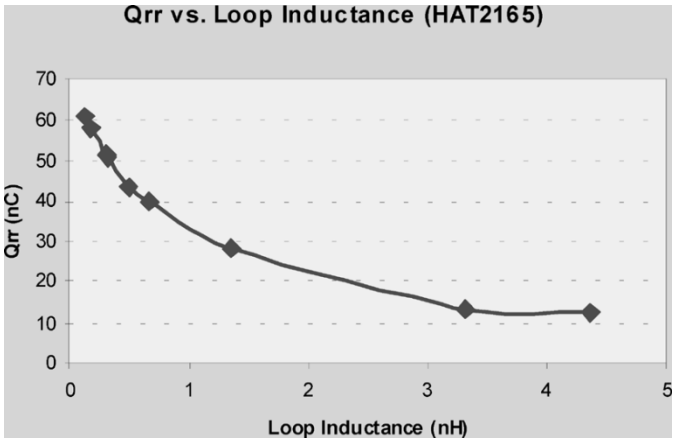


Fig. 11. Relationship between the reverse recovery charge of the diode and the loop inductance.

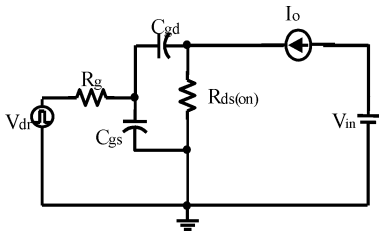


Fig. 12. Simplified equivalent circuit for the delay period of turn-off.

verse recovery loss of the diode has been included in the ringing loss.

In this final phase, the gate–source voltage exponentially increases while the drain current is oscillating and the MOSFET is operating in the ohmic region. At this stage, the $R_{ds(\mathrm{on})}$ is influenced by the gate–source voltage

$$v_{gs}(t) = (V_{dr} - V_{\mathrm{gs\_remain}})\left(1 - e^{-t/\tau_{G''''}}\right) + V_{gs\_remain} \tag{25}$$

where $\tau_{G''''}$ has the same expression as $\tau_{G'''}$, but the value changes a lot due to the nonlinear capacitance.

After the switch fully turns on, the calculation of the conduction loss is relatively simple. The expression is shown as

$$P_{\mathrm{cond\_top}} = \left(I_{\mathrm{o}}^2 + \frac{\Delta I_{\mathrm{o}}^2}{12}\right) \cdot D\, R_{ds(\mathrm{on})\_top} \tag{26}$$

where ΔI_{o} is the ripple of the load current I_{o}, D is the duty cycle and $R_{ds(\mathrm{on})\_\mathrm{top}}$ is the on resistance of the top switch. Because the $R_{ds(\mathrm{on})}$ is dependent on the temperature, it is better to consider the temperature effect in the loss calculation, which expressed in

$$R_{ds(\mathrm{on})} = R_{ds(\mathrm{on})\_25} + k\,(T_j - 25) \tag{27}$$

where $R_{ds(\mathrm{on})\_25}$ is the on resistance at 25 °C; k is the temperature coefficient, which can be obtained from the datasheet; and T_j is the junction temperature.

B. Turn-Off Period

Similar to the turn-on period, the MOSFET turn-off transition can also be divided into four distinct phases.

1) Delay Period: During the first phase of turn-off, the equivalent circuit is shown in Fig. 12. The gate–source voltage

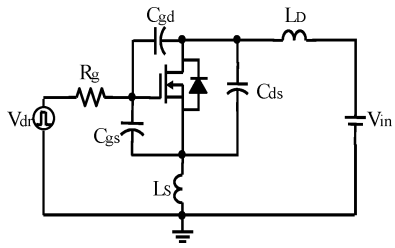


Fig. 13. Simplified equivalent circuit for the drain-source voltage rising period.

starts to fall, and discharge the device capacitances C_{gs} and C_{gd}. The drain current and drain-source voltage don't change at this stage. The gate-source voltage is expressed as

$$v_{gs}(t) = V_{dr} e^{-t/\tau_{G''''}}. \tag{28}$$

This stage ends when the gate source voltage satisfies the following relationship:

$$v_{gs}(t) = V_{th} + \frac{I_{\mathrm{o}}}{g_{fs}}. \tag{29}$$

2) Drain–Source Voltage Rising Period: During this stage, the equivalent circuit is shown in Fig. 13. The gate voltage is held and a plateau is normally observed. The analysis in [3] indicates that the drain–source voltage linearly rises

$$v_{ds}(t) = \frac{g_{fs}V_{th} + I_{\mathrm{o}}}{(1 + g_{fs}R_G)\,C_{gd} + C_{ds}}t. \tag{30}$$

When the drain-source voltage is equal to the input voltage V_{in}, this stage ends.

3) Drain Current Falling Period: After the drain-source voltage reaches input voltage, the drain current begins to fall. Assume the drain–source voltage is not clamped, which is a reasonable assumption because in a buck converter the voltage usually cannot be clamped due to the existence of parasitic components in the loop. The clamped-voltage case is not discussed in this paper. The equivalent circuit is the same as Fig. 13. The analysis is similar to that in Section III-A2. The time constants are also defined as before.

The sinusoidal solutions occur when $\tau_{G''}^2 < 4\tau_{G'}\tau_m$

$$v_{gs}(t) = \left(\frac{I_{\mathrm{o}}}{g_{fs}} + V_{th}\right)e^{-t/\tau_a}\left(\cos(\omega_a t) + \frac{1}{\omega_a \tau_a}\sin(\omega_a t)\right). \tag{31}$$

The drain current and the drain–source voltage are

$$i_d(t) = (g_{fs}V_{th} + I_{\mathrm{o}})\,e^{-t/\tau_a}\left(\cos(\omega_a t) + \frac{1}{\omega_a \tau_a}\sin(\omega_a t)\right) - g_{fs}V_{th}. \tag{32}$$

$$v_{ds}(t) = V_{\mathrm{in}} + (g_{fs}V_{th} + I_{\mathrm{o}})\,\omega_a\,(L_S + L_D)\,e^{-t/\tau_a} \times \left(1 + \left(\frac{1}{\omega_a \tau_a}\right)^2\right)\sin(\omega_a t). \tag{33}$$

The exponential solutions occur when $\tau_{G''}^2 > 4\tau_{G'}\tau_m$

$$v_{gs}(t) = \left(\frac{I_{\mathrm{o}}}{g_{fs}} + V_{th}\right)\frac{e^{-t/\tau_b}\tau_b - e^{-t/\tau_c}\tau_c}{\tau_b - \tau_c}. \tag{34}$$

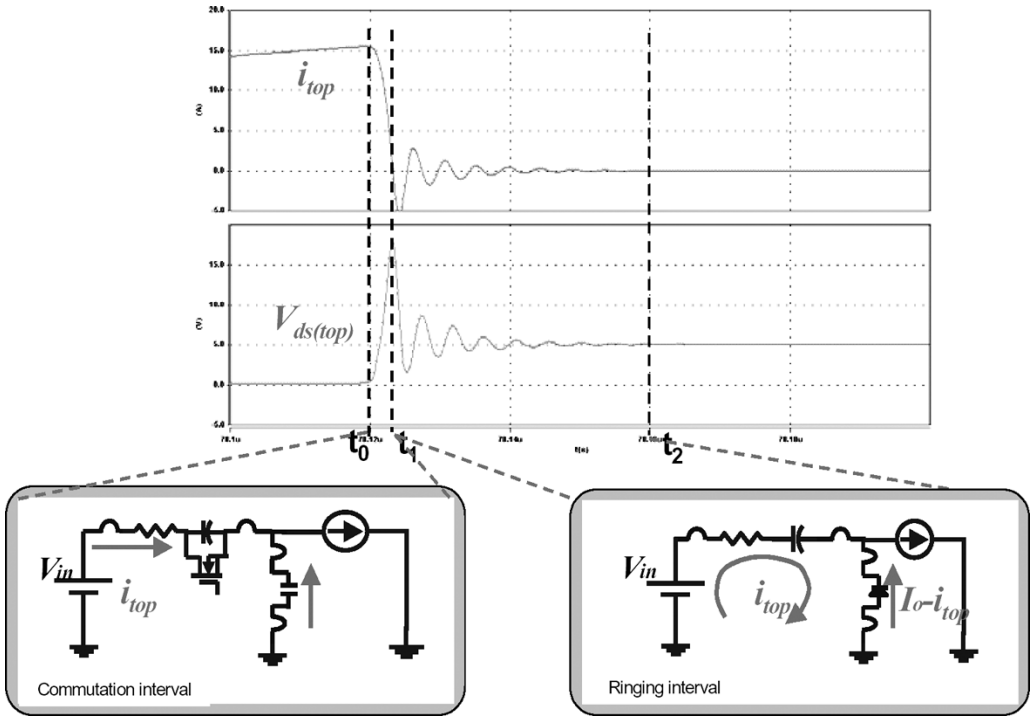


Fig. 14. Typical waveforms of a buck converter and its simplified equivalent circuits for the different periods during turn-off period.

The drain current and the drain–source voltage are

$$i_d(t) = (g_{fs}V_{th} + I_{\rm o})\left(1 - \frac{e^{-t/\tau_b}\tau_b - e^{-t/\tau_c}\tau_c}{\tau_b - \tau_c}\right) - g_{fs}V_{th}. \quad (35)$$

$$v_{ds}(t) = V_{\rm in} + (g_{fs}V_{th} + I_{\rm o})(L_S + L_D)\frac{e^{-t/\tau_b}\tau_b - e^{-t/\tau_c}\tau_c}{\tau_b - \tau_c}. \quad (36)$$

This stage ends when the drain current reaches zero.

4) Ringing Period: A typical turn-off waveform is shown in Fig. 14. A severe voltage ringing is observed after the current reaches zero. We assume the oscillation can be damped before the top switch turns on in the next cycle.

The $[t_0, t_1]$ period has been analyzed in 2-1, 2-2, and 2-3. At t_1, the drain–source voltage reaches its peak while drain current reaches zero. After t_1, the defined ringing period begins until it is well damped.

As usual, the loss can be calculated based on the current and voltage expressions. Based on the equivalent circuit in Fig. 15, the ringing voltage is derived as

$$v_{ds}(t) = V_{\rm in} + (V_{ds\_ifall} - V_{\rm in})\, e^{-t/\tau_d}\cos(\omega_d t) \quad (37)$$

where $\tau_d = 2L_{\rm loop}/R_{\rm loop}$, $\omega_d = \left[1/L_{\rm loop}C_{D\_top} - (R_{\rm loop}/2L_{\rm loop})^2\right]^{1/2}$, $L_{\rm loop}$ is the sum of $L_{\rm loop\_top}$ and $L_{\rm loop\_bot}$, V_{ds_ifall} is the drain–source voltage at the end of the drain–current falling period, and $C_{D\_top} = C_{ds} + C_{gd}$. It is pointed out again that the resistance $R_{\rm loop}$ is not only the dc value any more. Due to the high frequency ringing, the ac resistance should be considered.

Obviously, it is complicated. Following the same method used in the ringing loss calculation of the turn-on period, the ringing loss during the turn-off period can be derived as follows.

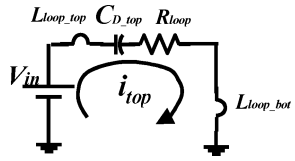


Fig. 15. Simplified equivalent circuit for the ringing period during the turn-off period.

First, the equivalent circuit is shown in Fig. 15. Again, the load current doesn't contribute to the oscillation and therefore is not considered.

The energy stored in the loop at t_1 is

$$E_{t1} = \frac{1}{2}Q_{\rm Vpeak}V_{\rm peak} + \frac{1}{2}L_{\rm loop\_bot}I_{\rm o}^2 \quad (38)$$

where $Q_{\rm Vpeak}$ is the charge stored in the output capacitor C_{D_top} of the top switch when the voltage reaches its peak value $V_{\rm peak}$, $L_{\rm loop\_bot}$ is the parasitic inductance in series with the bottom switch.

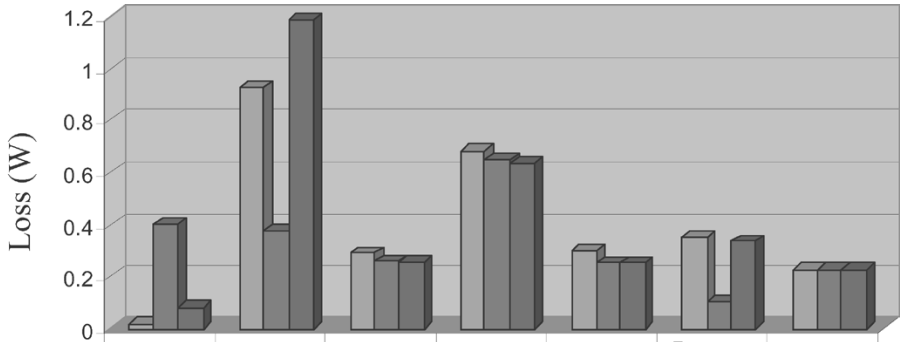
At t_2, the oscillation is damped. The circuit reaches another steady state. And the energy stored in the output capacitor is

$$E_{t2} = \frac{1}{2}Q_{Vin}V_{\rm in} + \frac{1}{2}L_{\rm loop\_bot}I_{\rm o}^2 \quad (39)$$

where Q_{Vin} is the charge stored in C_{D_top} when the voltage reaches its steady state $V_{\rm in}$.

The energy recovered by the input source $V_{\rm in}$ during $[t_1, t_2]$ is

$$E_{\rm source} = \int_{t1}^{t2} V_{\rm in}i_{\rm top}(t)dt = V_{\rm in}\int_{t1}^{t2} i_{\rm top}(t)dt = V_{\rm in}\left(Q_{\rm Vpeak} - Q_{Vin}\right). \quad (40)$$



	HS turn-on	HS turn-off	HS Cond.	LS Cond.	BD Cond.	Reverse recovery & ringing	Drive loss
physical model	0.014	0.926	0.288	0.682	0.3	0.35	0.225
conventional analytical Model	0.401	0.374	0.256	0.648	0.25	0.1	0.225
proposed analytical model	0.081	1.19	0.255	0.6345	0.25	0.334	0.225

Fig. 16. Comparison of loss breakdown based on different models.

Therefore, the energy dissipated in the loop is

$$E_{\text{ring\_turnoff}} = E_{t1} - E_{t2} - E_{\text{source}} = \frac{1}{2} Q_{\text{Vpeak}} (V_{\text{peak}} - 2V_{\text{in}}) + \frac{1}{2} Q_{Vin} V_{\text{in}}. \quad (41)$$

It is found that the ringing loss is relevant to the peak voltage value and independent on the loop resistance. In order to get the ringing loss, the peak voltage value should be derived first, which can be solved based on (32) and (33), or (35) and (36). The peak voltage is achieved at the moment when the drain current falls to zero at the first time.

After the top switch turns off, the current fully shifts to the bottom switch branch. Due to the dead time of the gate signals, the body diode conducts current prior to the bottom MOSFET turn-on and causes body diode conduction loss. It is expressed as

$$P_{cond\_\text{bot}} = V_{DF} \Delta I_{\text{o\_V}} T_{d1} f_{\text{s}} + V_{DF} \Delta I_{\text{o\_p}} T_{d2} f_{\text{s}} \quad (42)$$

where V_{DF} is the forward voltage drop, $\Delta I_{\text{o\_V}}$ is the valley value of the load current I_{o}, $\Delta I_{\text{o\_p}}$ is the peak value of the load current I_{o}, T_{d1}, and T_{d2} are the dead time and f_{s} is the switching frequency.

Because the bottom MOSFET operates at zero-voltage-switching (ZVS) condition, the turn-on loss is neglected. And, because the current shifts from MOSFET to its body diode when it turns off, the turn-off loss is also negligible. Therefore, the major loss of the bottom MOSFET is the conduction loss given by

$$P_{cond\_\text{bot}} = \left(I_{\text{o}}^2 + \frac{\Delta I_{\text{o}}^2}{12} \right) \cdot (1 - D) \, R_{ds(\text{on})\_\text{bot}} \quad (43)$$

where ΔI_{o} is the ripple of the load current I_{o}, D is the duty cycle, and $R_{ds(\text{on})\_\text{bot}}$ is the on resistance of the bottom switch. Following (27), more accurate $R_{ds(\text{on})}$ can be achieved.

IV. Model Comparison and Discussion

In order to verify this analytical model, a lot of comparisons have been carried out. One example is provided in this section. The circuit setup is as follows. The device combination is HAT2168 (for top switch) and HAT2165 (for bottom switch). The input voltage is 12 V. The output voltage is 1.3-V. The output inductance is 200-nH. The output current is 12.5 A. The switching frequency is 1 MHz. The parasitic inductance are $L_{d1} = 3$- nH, $L_{\text{s}} = 1$- nH, $L_{d2} = 3$- nH and $L_{\text{s2}} = 1$- nH. The ac resistance is 150 mΩ at 40 MHz. The dead time for body diode conduction is 40 ns. The junction temperature is 100 °C.

The loss breakdown is shown in Fig. 16. The left-hand-side bars are the simulation results based on device physical model and the simulation tool is Medici. The middle bars are the simulation results based on the conventional analytical model [3]. And the right-hand-side bars are the simulation results based on the proposed analytical model.

The device physical model is used as a benchmark for this comparison because it is the most accurate model we have so far. The time frame of the turn-on loss is defined as $[t_0, t_1]$ in Fig. 9. The ringing loss during the top switch turn-on is calculated in the following way: when the drain current reaches I_{o}, start to integral the energy pumped from the input source until the oscillation is completely damped. Then, the energy sent to the output and the conduction loss of the top switch is deducted. The ringing loss during the top switch turn-off is calculated from the moment when the drain current falls back to zero until the oscillation is damped.

Compared to the benchmark, the conventional analytical model has a huge error for the switching loss of the top switch. And the ringing loss is much smaller. The reason is that the nonlinear capacitor and parasitic inductance dramatically impact the switching loss. The proposed analytical model shows better accuracy. The switching loss and ringing loss are close to the results of the benchmark. The error is mainly caused by the nonlinear g_{fs}.

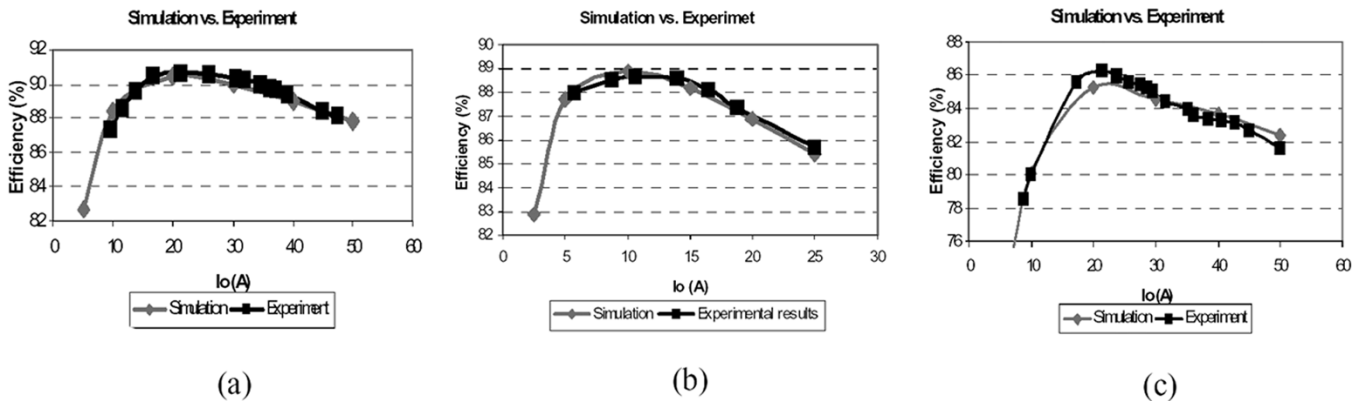


Fig. 17. Loss model verification with experimental results: (a) top switch HAT2168, bottom switch Si4864, $L = 200$ nH, driver LM2726, $f_s = 1$ MHz, $V_{in} = 5$ V, $V_o = 1.2$ V; (b) top switch HAT2168, bottom switch HAT2165, $L = 100$ nH, driver LM2726, $f_s = 1$ MHz, $V_{in} = 12$ V, $V_o = 1.5$ V and (c) top switch HAT2168, bottom switch Si4864, $L = 100$ nH, driver LM2726, $f_s = 2$ MHz, $V_{in} = 5$ V, $V_o = 1.2$ V.

TABLE I
EXPERIMENT CIRCUIT SETUP

	Top switch	Bottom switch	Output inductance (nH)	Driver	f_s (MHz)	V_{in} (V)	V_o (V)
Case (a)	HAT2168	Si4864	200	LM2726	1	5	1.2
Case (b)	HAY2168	HAT2165	100	LM2726	1	12	1.5
Case (c)	HAT2168	Si4864	100	LM2726	2	5	1.2

V. EXPERIMENT VERIFICATION

Because it is very difficult to break down the loss in the measurement, the efficiency curves are compared between the experimental results and the simulation results based on the proposed model.

The synchronous Buck converter shown in Fig. 1 is used as an example. Fig. 17 shows three-case comparison between experiment and simulation results. The setup is listed in Table I.

The parasitic inductances and ac resistances are simulated through the Maxwell Q3D. The parasitic inductance are $L_{d1} =$ 2- nH, $L_s =$ 1- nH, $L_{d2} =$ 2- nH and $L_{s2} =$ 1- nH. The ac resistance is 150-mΩ at 40-MHz oscillation frequency.

The simulation results match the experimental results very well. It works well even at 2-MHz switching frequency. It shows good accuracy. Compared to the physics-based model, the simulation time is much less. To simulate the same amount of data (18 points in Fig. 17), the physics-based model normally takes more than one month (two days for each point) while the proposed model needs only around 1 min.

This analytical model has been successfully used in the optimal bus voltage study for two-stage approach [7]. And it could also be used in other fields needing massive data process to shorten the simulation time.

VI. CONCLUSION

An accurate analytical model is proposed in this paper and demonstrates good trade-off between the accuracy and simulation time. The nonlinearity of the capacitors of the devices and the parasitic inductance in the circuit are considered in the model. In addition, the ringing loss is considered and the physical meaning could be easily understood. Therefore, the accuracy is significantly improved. Based on this model, the circuit loss could be accurately predicted. The simulation results match the experimental results very well even at 2-MHz switching frequency.

As a conclusion, the proposed analytical model is suitable for massive data processing of some applications that need good accuracy and short simulation time, such as topology comparison and investigation.

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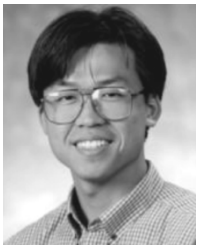

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