Synchronous and Rectified Buck PWM Controller

FEATURES:

- Input Voltage Range from 4.5 V to 13.2 V
- 320 kHz Internal Oscillator
- Boost Pin Operates to 26.5 V
- Voltage Mode PWM Control
- 0.8 V ~1.5% Internal Reference Voltage
- Adjustable Output Voltage
- Internal Soft-Start
- Internal 1.5 A Gate Drivers
- Adaptive Non-Overlap Circuit
- 90% Max Duty Cycle
- Input UVLO
- Over-Temperature Protection
- Fully Specified over -40C to 85C
- SOP8 Package
- RoHS Compliant (100% Pb-free available)

GENERAL DESCRIPTION:

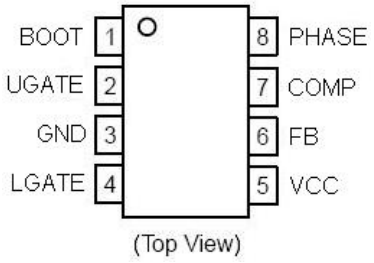
The CAT7580 is a voltage mode PWM controller designed to operate from a 5.0 V to 12.0 V supply and produce an output voltage as low as 0.8 V. This 8-pin device provides an optimal level of integration to reduce size and cost of the power supply. The CAT7580 has a fixed 320 kHz oscillator and soft-start function. The CAT7580 provides a 1.5 A floating gate driver design to drive N-Channel MOSFETs in a synchronous configuration. Adaptive non-overlap circuitry reduces switching losses by preventing simultaneous conduction of both outputs. Protection features include thermal shutdown and undervoltage lockout (UVLO).

The CAT7580 is available in an 8-pin SOIC package.

APPLICATION:

- Graphics Cards
- Desktop Computers
- Servers/Networking
- DSP and FPGA Power Supply
- DC-DC Regulator Modules
- LCD Monitor and LCD TV

PIN CONFIGURATION:

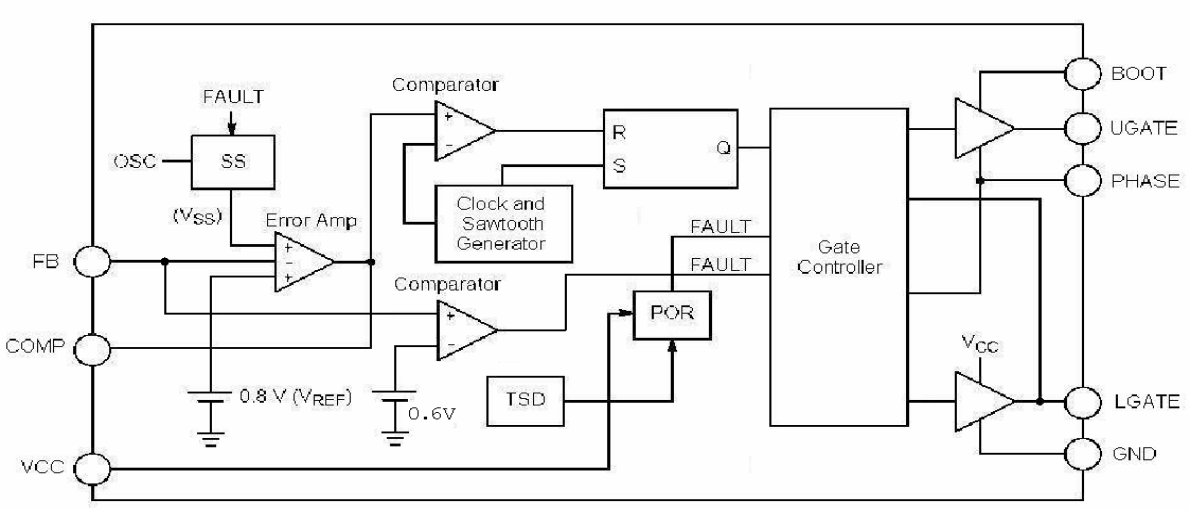


(Top View)

ORDERING INFORMATION:

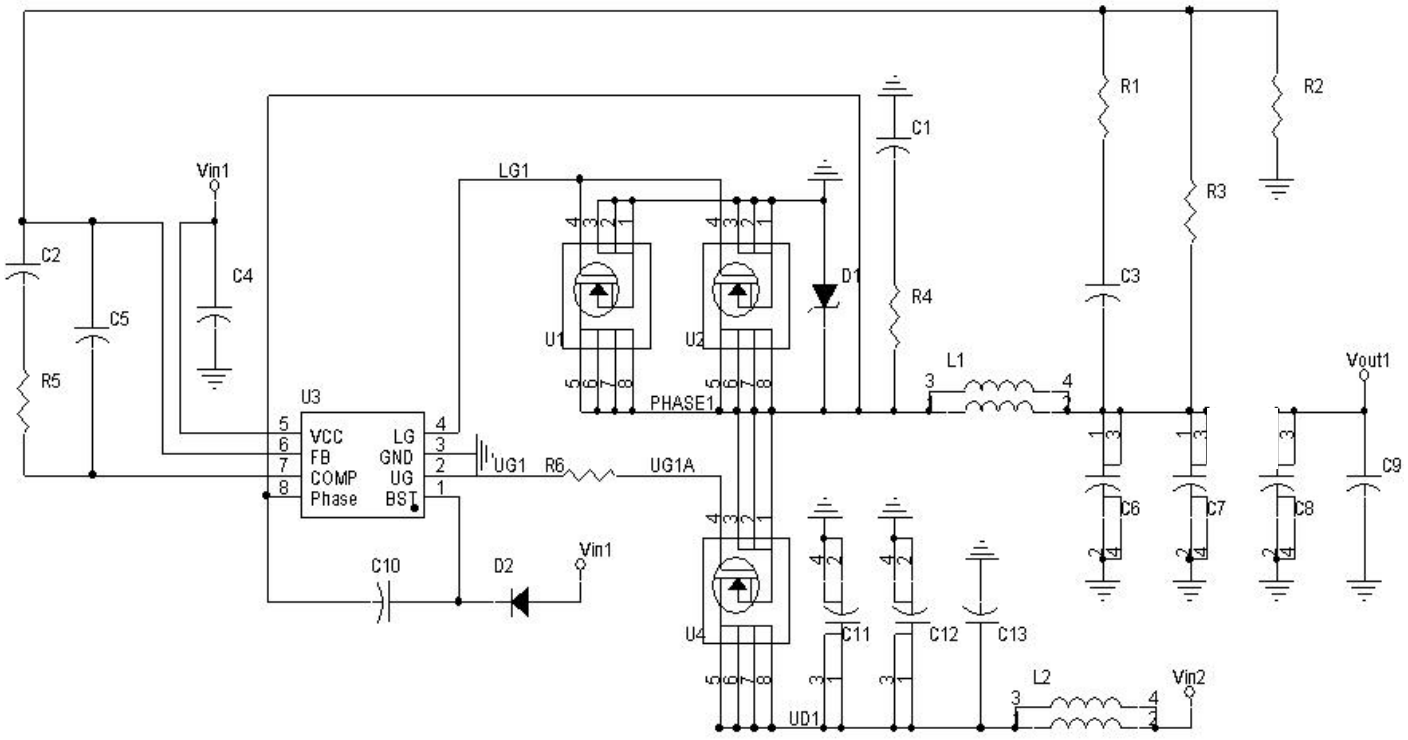
Part Number	Package	Shipping
CAT7580CA	8L SOP(Green)	2500/Tape & Reel
CAT7580CH	8L SOP(Pb-free)	

FUNCTION BLCOK DIAGRAM:



TYPICAL APPLICATION:

All signals of CAT7580 should be routed at least 30mil trace width.



Vout=0.8x(1+R3/R2)

*note: The recommended applications shall be customer design-in orientation to fit each customers demand. Based on the nature of customers demand-oriented, please contact CAT or agent for design support service.

ABSOLUTE RATING

Parameter	Symbol	Max. Rating
Vcc, Supply Voltage	VCC	15V
Bootstrap Supply Voltage Input	BOOT	30V wrt/GND 15V wrt/PHASE
Swtiching Node (Bootstrap Supply Return)	PHASE	30V
High-Side Driver Output (Upper Gate)	UGATE	30V wrt/GND 15V wrt/PHASE
Low-Side Driver Output (Lower Gate)	LGATE	15V
Feedback	FB	5.5V
COMP	COMP	5.5V
Operating Temperature		0℃ to 70℃
Storage Temperature		-55℃ to 150℃
Max. Junction Temperature		150℃
ESD Classification		Class 2

*note: The IC has a protection circuit against static electricity. Do not apply high static electricity or high voltage that exceeds the performance of the protection circuit to the IC.

ELECTRICAL CHARACTRISTIC:

(Recommended Operating Conditions, Unless Otherwise Noted; VCC = 12V; Temperature = 0 - 70 °C (typical = 25 °C))

Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage					
Input Voltage Range		4.5		13.2	V
Boost Voltage Range		4.5		26.5	V
Supply Current					
Quiescent Supply	VFB=1.0V, No Switching, VCC=13.2V		1.0	1.75	mA
Boost Quiescent	EN=0 V		140		μA
VCC Undervoltage Lockout					
UVLO Threshold	VCC rising Edge	3.85	4.2		V
UVLO Hysteresis			0.5		V
VOUT Undervoltage Lockout					
Under-Voltage Level	Percent of Nominal		75		%
Switching Regulator					
VFB Feedback Voltage Control Loop in Regulation (Note 1)	TA = 0℃ to 70℃ TA = -40℃ to 85℃	0.788 0.784	0.800	0.812 0.816	V
Oscillator Frequency		240	320	400	KHz
Ramp-Amplitude Voltage			1.1		V
Minimum Duty Cycle			0		%
Maximum Duty Cycle		85	90	95	%
ERROR Amplifier					
DC Gain			96		dB
Gain-Bandwidth Product			20.0		MHz
Slew Rate	COMP_GND=10pF		8.0		V/μs
FB Bias Current	VFB=1V		0.1		μA
Gate Driver					
UGATE Rise Time (Note 2)			6.0	15	ns
UGATE Fall Time (Note 2)	Load=1.0nF		15	30	ns
LGATE Rise Time (Note 2)	VCC=8.0V		6.0	15	ns
LGATE Fall Time (Note 2)			6.0	15	ns
UGATE Sink Current (Note 2)			1.0		A
UGATE Source Current (Note 2)	VCC=12V VUGATE=VLGATE=2.0V		1.5		A
LGATE Sink Current (Note 2)			1.5		A
LGATE Source Current (Note 2)			1.5		A

Internal Soft-Start					
Time			1.2	0	ms
Thermal Shutdown					
Over-Temperature Trip Point			160		℃

Note:
1. Specifications to -40℃ are guaranteed via correlation using standard statistical quality control, not tested in production
2. Guaranteed by design; not production tested.

PIN DESCRIPTION

BOOT
This pin provides bias voltage to the upper MOSFET driver. A bootstrap circuit may used to generate BOOT voltage suitable to drive a standard N-channel MOSFET.

UGATE
Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for upper MOSFET. It is also monitored by the adaptive shoot through protection function to determine when upper MOSFET has turned off.

GND
IC ground reference. All control circuits are referenced to this pin.

LGATE
Connect UGATE to the lower MOSFET gate. This pin provides the gate drive for lower MOSFET. It is also monitored by the adaptive shoot through protection function to determine when lower MOSFET has turned off.

VCC
Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 μF capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.

FB
This pin is the inverting input to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage-control feedback loop. Connect this pin to the output resistor divider (if used) or directly to Vout.

COMP
Compensation Pin. This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage-control feedback loop. This pin should not be shorted to ground to disable switching.

PHASE
Switch node pin. Connect this pin to the source of the top MOSFET. A Schottky diode between this pin and ground is recommended to reduce negative transient voltages which are common in a power supply system.

FUNCTION DESCRIPTION

Duty Cycle and Maximum Pulse Width Limits

In steady state DC operation, the duty cycle will stabilize at an operating point defined by the ratio of the input to the output voltage. The CAT7580 can achieve a 90% duty cycle. There is a built in off−time which ensures that the bootstrap supply is charged every cycle.

INPUT VOLTAGE RANGE (VCC AND BOOT)

The input voltage range for both VCC and BOOT is 4.5 V to 13.2 V with respect to GND and PHASE, respectively. Although BOOT is rated at 13.2 V with respect to PHASE, it can also tolerate 26.5 V with respect to GND.

NORMAL SHUTDOWN BEHAVIOR

Normal shutdown occurs when the IC stops witching because the input supply reaches UVLO threshold. In this case, switching stops, the internal SS is discharged, and all GATE pins go low. The switch node enters a high impedance state and the output capacitors discharge through the load with no ringing on the output voltage.

INTERNAL SOFT−START

The CAT7580 features an internal soft−start function, which reduces inrush current and overshoot of the output voltage. Soft−start is achieved by ramping up the internal soft−start voltage (VSS) which is applied to the input of the error amplifier. This sequence begins once VCC surpasses its UVLO threshold. The typical soft−start time is 1.2 msec. The internal soft−start voltage is held low when the part is in UVLO.

VCC UVLO

Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when VCC is too low to support the internal rails and power the converter. For the CAT7580, the UVLO is set to ensure that the IC will start up when VCC reaches 4.2 V and shutdown when VCC drops below 3.7 V. This permits operation when converting from a 5.0 V input voltage.

VOUT UVLO

The FB pin is monitored during converter operation by an Under-Voltage (UV) comparator. If the FB voltage drops below 75% of the reference voltage (0.8V), a fault signal is internally generated, and the fault logic shuts down the regulator.

THERMAL SHUTDOWN

The CAT7580 also provides Thermal Shutdown (TSD) for added protection. The TSD circuit monitors the die temperature and turns off the top and bottom gate drivers if an over temperature condition is detected. The internal soft−start state is reset. This is a latched state and requires a power cycle to reset.

DRIVERS

The CAT7580 includes 1.5 A gate drivers to switch external N−Channel MOSFETs. This allows the CAT7580 to address high−power as well as low−power conversion requirements. The gate drivers also include adaptive non−overlap circuitry. The non−overlap circuitry increases efficiency, which minimizes power dissipation, by minimizing the body diode conduction time.

Careful selection and layout of external components is required, to realize the full benefit of the onboard drivers. The capacitors between VCC and GND and between BOOT and PHASE must be placed as close as possible to the IC. The current paths for the UGATE and LGATE connections must be optimized. A ground plane should be placed on the closest layer for return currents to GND in order to reduce loop area and inductance in the gate drive circuit.

INPUT CAPACITOR SELECTION

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$I_{inRMS} = I_{OUT}\sqrt{D \times (1 - D)}$$

where D is the duty cycle, I_{inRMS} is the input RMS current, and I_{OUT} is the load current. The equation reaches its maximum value with D = 0.5. Losses in the input capacitors can be

calculated with the following equation:

$$P_{CIN} = ESR_{CIN} \times Iin_{RMS}^2$$

where P_{CIN} is the power loss in the input capacitors and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur.

CALCULATING INPUT STARTUP CURRENT

To calculate the input startup current, the following equation can be used.

$$I_{inrush} = \frac{C_{OUT} \times V_{OUT}}{t_{SS}}$$

where I_{inrush} is the input current during startup, C_{OUT} is the total output capacitance, V_{OUT} is the desired output voltage, and t_{SS} is the internal soft−start interval. If the inrush current is higher than the steady state input current during max load, then the input fuse should be rated accordingly, if one is used.

OUTPUT INDUCTOR SELECTION

The output inductor is selected to meet the output voltage ripple requirements and affects the load transient response. Higher inductance reduces the inductor's ripple current and induces lower output ripple voltage. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Although increase the inductance reduce the ripple current and voltage, but the large inductance reduces the regulator's response time to load transient. Increasing the switching frequency (Fs) for a given inductor also reduces the ripple current and voltage but it will increase the switching loss of the power MOS.

To select the inductor value, a guideline is to choose the ripple current ($\triangle$I) to be approximately 10%~50% of the maximum output current. Once the inductor value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. It is also important to have the inductance tolerance specified to keep the accuracy of the system controlled. Using 20% for the inductance (at room temperature) are reasonable tolerances that most manufacturers can meet. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

OUTPUT CAPACITORS SELECTION

An output capacitor is required to filter the output and supply the load transient current. Higher Capacitor value and lower ESR reduce the output ripple and the load transient drop. These requirements are met with a mix of capacitors and careful layout.

In typical switching regulator design, the ESR of the output capacitor bank dominates the transient response. The number of output capacitors can be determined by using the following equations:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

$\triangle V_{ESR}$ = change in output voltage due to ESR (assigned by the designer).

$\triangle I_{OUT}$ = load transient.

ESR_{CAP} = maximum ESR per capacitor

(specified in manufacturer's data sheet).

ESR_{MAX} = maximum allowable ESR.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Consult the capacitors manufacturer to make sure the decoupling requirements.

FEEDBACK COMPENSATION

The compensation required for VOUT1 and VOUT2 is similar to many other switching regulators.

The figure 2 shows type-3 compensation, but the simpler type 2 is also possible, under the right conditions. A simple rule of thumb of type-3 compensation is that when buck capacitors are used on the outputs, the effective ESR is about smaller than 3 mohm. Notes that the component labels match the equations given in this section, but may not match other diagrams in this datasheet.

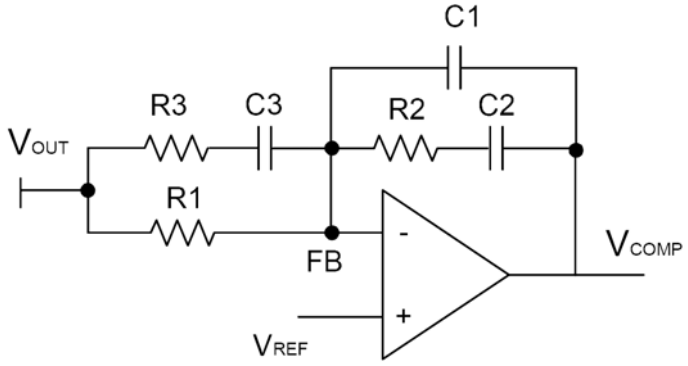


Figure 1

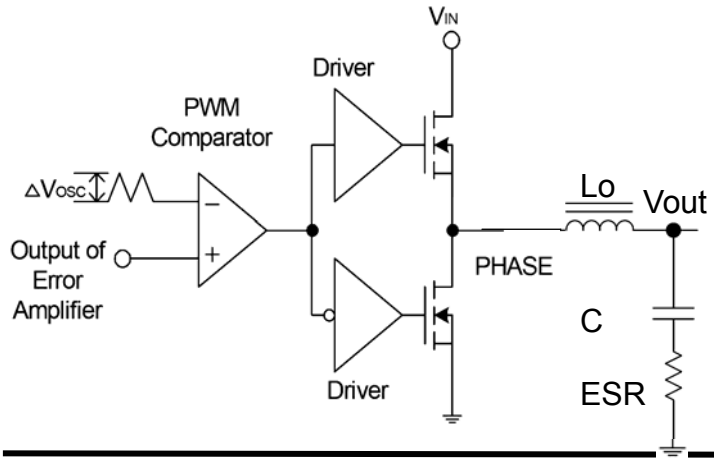


Figure 2

In Figure 1 and 2, the output voltage (Vout) is regulated to the Reference voltage level. The error amplifier output (V_{COMP}) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of VIN at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The closed loop transfer function of the converter includes two part, the error amplifier compensation and the modulator transfer functions. The modulator transfer function is dominated by a DC gain and the output filter, with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (VIN) divided by the peak-to-peak oscillator voltage $\triangle V_{OSC}$.

$$F_{LC} = \frac{1}{2\pi \bullet \sqrt{L_O \bullet C_O}} \qquad F_{ESR} = \frac{1}{2\pi \bullet (ESR \bullet C_O)}$$

The poles and zeros location of the type-3 compensation of error amplifier list below.

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C2} \qquad F_{P1} = \frac{1}{2\pi \bullet R2 \bullet \left(\frac{C1 \bullet C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \bullet (R1 + R3) \bullet C3} \qquad F_{P2} = \frac{1}{2\pi \bullet R3 \bullet C3}$$

The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (fco) and adequate phase margin.

The following guidelines will help users to design the compensation network.

(1). Select the desired zero crossover frequency

F_{CO}.

F_{CO} is usually 1/4 ~ 1/10 switch frequency (F_S).

(2). Choose a value for R1.

(3). Pick gain R2/R1 for desired F_{CO}. To simplify, the

R2 can be calculated by

$$V_{in} / \triangle V_{osc} * F_{LC}/F_{CO} * R2/R1 = 1$$

(4). Place F_{Z1} about 0.75 * F_{LC} to calculate the C2.

(5). Place F_{P1} at F_{ESR} to calculate the C1.

(6). Place F_{Z2} about F_{LC}.

(7). Place F_{P2} about 0.5 * F_s.

Combined (6), (7) the R3 and C3 will be calculated.

(8). Estimate the stability, Modify F_{CO} and R2/R1 gain then repeat if necessary.

The Figure 3 shows an asymptotic plot of the converter's gain vs. frequency.

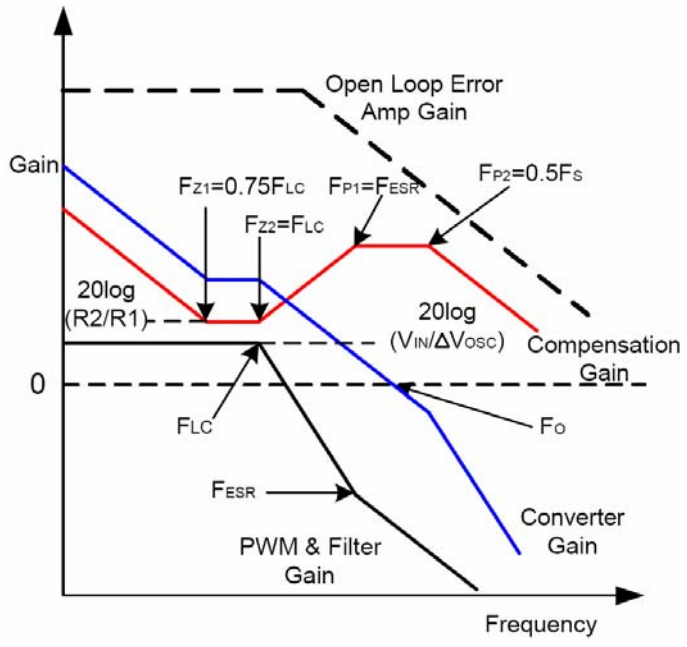


Figure 3

Thermal Considerations

The power dissipation of the CAT7580 varies with the MOSFETs used, VCC, and the boost voltage (V_{BOOT}). The average MOSFET gate current typically dominates the control IC power dissipation. The IC power dissipation is determined by the formula:

$$P_{IC} = (I_{CC} \times VCC) + P_{UGATE} + P_{LGATE}.$$

Where:

P_{IC} = Control IC power dissipation,
I_{CC} = IC measured supply current,
V_{CC} = IC supply voltage,
P_{UGATE} = Top gate driver losses,
P_{LGATE} = Bottom gate driver losses.

The upper (switching) MOSFET gate driver losses are:

$$P_{UGATE} = Q_{UGATE} \times f_{SW} \times V_{BOOT}.$$

Where:

Q_{UGATE} = Total upper MOSFET gate charge at V_{BOOT},
f_{SW} = The switching frequency,
V_{BOOT} = The BOOT pin voltage.

The lower (synchronous) MOSFET gate driver losses are:

$$P_{LGATE} = Q_{LGATE} \times f_{SW} \times V_{CC}.$$

Where:

Q_{LGATE} = total lower MOSFET gate charge at VCC.

The junction temperature of the control IC can then be calculated as:

$$T_J = T_A + P_{IC} + \theta_{JA}.$$

Where:

T_J = The junction temperature of the IC,
T_A = The ambient temperature,
θ_{JA} = The junction−to−ambient thermal resistance of the IC package.

The package thermal resistance ($R_{\theta JA}$) can be obtained from the specifications section of this data sheet and a calculation can be made to determine the IC junction temperature. In addition, a thermal resistance (Junction−to−Ambient/Safe Operating Area) curve has been included below to further aid design. However, it should be noted that the

physical layout of the board, the proximity of other heat sources such as MOSFETs and inductors, and the amount of metal connected to the IC, impact the temperature of the device. Use these calculations as a guide, but measurements should be taken in the actual application.

POWER MOS SELECTION

CAT7580 requires 2 N-channel power MOSs for each PWM output. These should be selected base on $R_{ds(on)}$, gate supply voltage, gate charge (capacitance) and thermal management requirements. In general, the upper power MOS should be chosen to minimize the gate charge, since switching loses dominate. Since the lower power MOS is on most of the time, low $R_{ds(on)}$ should be the main consideration.

It can be advantageous to use multiple power MOSs to reduce power consumption. By placing a number of MOSs in parallel, the effective $R_{ds(on)}$ is reduced, thus reducing the ohmic power loss. However, placing MOSs in parallel increases the gate capacitance so that switching losses increase. As long as adding another parallel MOS reduces the ohmic power loss more than the switching losses increase, there is some advantage to doing so.

The following equations can be used to calculate power dissipation in the power MOSs.

$$P_{UPPER} = I_O^2 \times r_{DS(ON)} \times D + \frac{1}{2} Io \times V_{IN} \times t_{SW} \times Fs$$

$$P_{LOWER} = I_O^2 \times r_{DS(ON)} \times (1 - D)$$

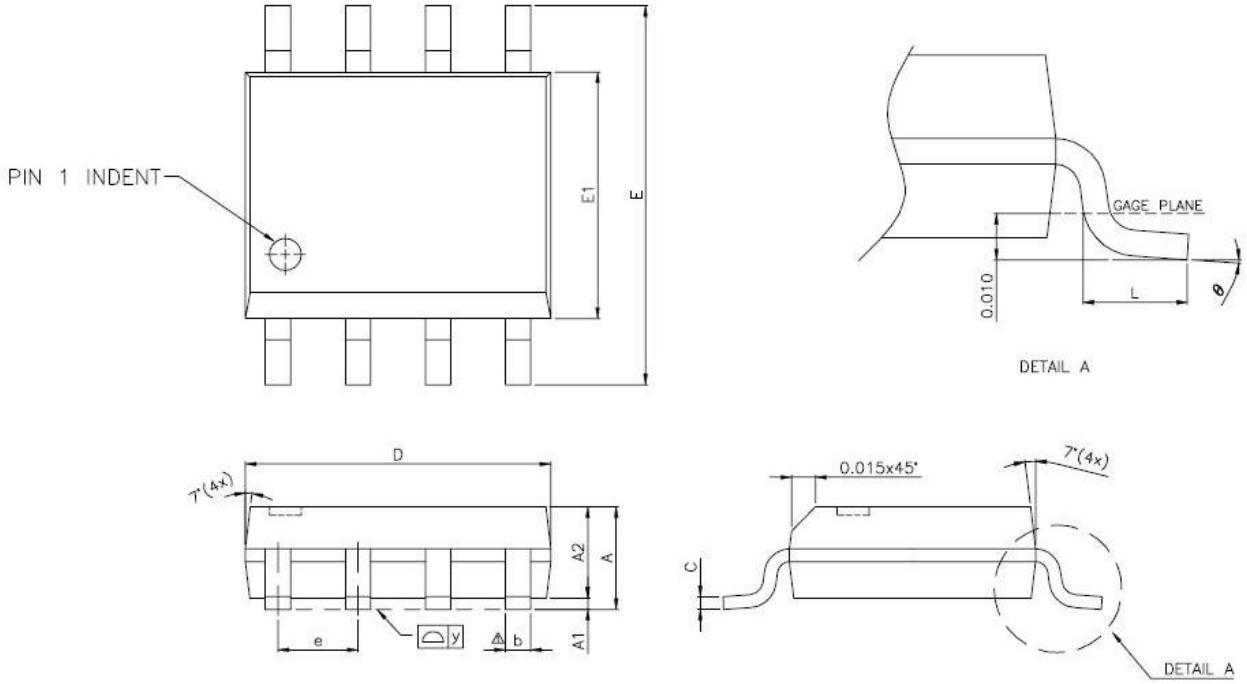
Where,

D is the duty cycle = Vout / Vin.

t_{SW} is the switching interval.

Fs is the switching frequency.

MECHINICAL DIMENSION



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.47	1.60	1.73
A1	0.10	——	0.25
A2	——	1.45	——
b	0.33	0.41	0.51
C	0.19	0.20	0.25
D	4.80	4.85	4.95
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	——	1.27	——
L	0.38	0.71	1.27
⚠3 y	——	——	0.076
θ	0°	——	8°

⚠3
NOTE :

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-012

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