HIGH FIDELITY CLASS D AUDIO AMPLIFIER SOLUTION

DESCRIPTION

The ZXCD1000 provides complete control and modulation functions at the heart of a high efficiency high performance Class D switching audio amplifier solution. In combination with custom output magnetics (ZXFN1000) and Zetex HDMOS MOSFET devices, the ZXCD1000 provides a high performance Class D audio amplifier with all the inherent benefits of Class D.

The ZXCD1000 solution uses proprietary circuitry and magnetic technology to realise the true benefits of Class D without the traditional drawback of poor distortion performance. The combination of circuit design, magnetic component choice and layout are essential to realising these benefits.

The ZXCD1000 reference designs give output powers up to 50W rms with typical open loop (no feedback) distortions of less than 0.2% THD + N over the entire audio frequency range at 90% full output power. This gives an extremely linear system. The addition of a minimum amount of feedback (10dB) further reduces distortion figures to give < 0.1 % THD + N typical at 1kHz.

From an acoustic point of view, even more important than the figures above, is that the residual distortion is almost totally free of any crossover artifacts. This allows the ZXCD1000 to be used in true hi-fi

applications. This lack of crossover distortion, sets the ZXCD1000 solutions quite apart from most other presently available low cost solutions, which in general suffer from severe crossover distortion problems.

FEATURES

- 90% efficiency
- 4 / 8 Ω drive capability
- Noise Floor -115dB for solution
- Flat response 20Hz - 20kHz
- High gate drive capability (2200pF)
- Very low THD + N 0.1% typical full power full band (for the solution)
- Complete absence of crossover artifacts
- OSC output available for sync in multi-channel applications
- Available in a 16 pin eQSOP package

APPLICATIONS

- Automotive audio systems
- Home Theatre
- Multimedia
- Wireless speakers
- Portable audio
- Sub woofer systems
- Public Address system
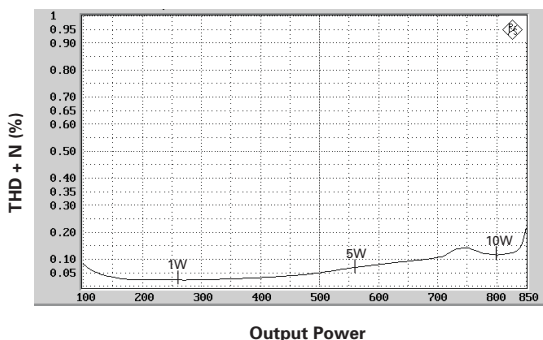
Distortion v Power
8Ω open loop at 1kHz.

The plot shows Distortion v Power into an 8Ω load at 1kHz. This plot clearly demonstrates the unequalled performance of the Zetex solution. Typical distortion of 0.05% at 1W can be seen with better than 0.15% at 10W. Truly world class performance.

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ABSOLUTE MAXIMUM RATINGS

Terminal Voltage with respect to G_{ND}

V_{CC}	20V
Power Dissipation	1W
Operating Temperature Range	-40°C to 70°C
Storage Temperature Range	-50°C to 85°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS
TEST CONDITIONS (unless otherwise stated) V_{cc} = 16V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Operating Voltage Range		12	16	18	V
I_{ss}	Operating Quiescent Current	V_{CC} = 12V V_{CC} = 18V V_{CC} = 16V		40 40 40		mA mA mA
F_{osc}	Switching Frequency	C_{osc} = 330pF	150	200	250	kHz
$F_{osc(tol)}$	Frequency Tolerance	C_{osc} = 330pF			+/-25	%
Vol OutA/B	Low level output voltage	No load			100	mV
Voh OutA/B	High level output voltage	No load	7.5			V
T_{Drive}	Output Drive Capability (OUT A / B Rise/Fall)	Load Capacitance = 2200pF		50		ns
5V5tol	Internal Rail Tolerance	1µF Decoupling	5.23	5.5	5.77	V
9VA/Btol	Internal Rail Tolerance	1µF Decoupling	8.32	8.75	9.18	V
Audio A / B	Input Impedence		1.35k	1.8k	2.3k	Ohms
Triangle A / B	Input Impedence		1.35k	1.8k	2.3k	Ohms
Audio A / B	Bias Level		2.95	3.1	3.25	V
Triangle A / B	Bias Level		2.95	3.1	3.25	V
Osc A / B	Amplitude		0.89	1.05	1.2	V

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Pin number	Pin Name	Pin Description
1	Audio A	Audio Input for Channel A
2	Triangle A	Triangle Input for Channel A
3	Osc A	Triangle Output
4	Dist	No connection
5	C_{osc}	External timing capacitor node (to set the switching frequency)
6	Osc B	Triangle Output (for slave ZXCD1000 in stereo application)
7	Triangle B	Triangle Input for Channel B
8	Audio B	Audio Input for Channel B
9	Gnd	Small Signal GND
10	OUT B	Channel B PWM Output to drive external Bridge MOSFETs
11	Gnd2	Power GND (for Output Drivers)
12	9VB	Internal Supply Rail (Decouple with 1μF Cap)
13	VCC	Input Supply Pin (Max = 18V)
14	9VA	Internal Supply Rail (Decouple with 1μF Cap).
15	OUT A	Channel A PWM Output to drive external Bridge MOSFETs
16	5V5	Internal Supply Rail (Decouple with 1μF Cap)
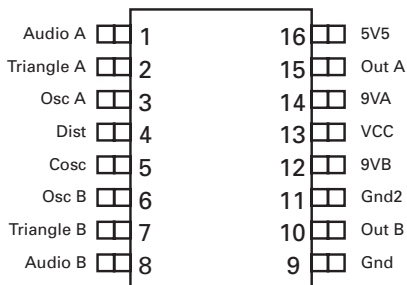
Figure 1
Pin Connection Diagram

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ZXCD1000 Class D controller IC

A functional block diagram of the ZXCD1000 is shown in Figure 2. The on chip series regulators drop the external V_{CC} supply (12V-18V) to the approximate 9V (9VA/9VB) and 5.5V (5V5) supplies required by the internal circuitry.

A triangular waveform is generated on chip and is brought out at the OscA and OscB outputs. The frequency of this is set (to ~200kHz) by an external capacitor (C_{osc}) and on chip resistor. The triangular waveform must be externally AC coupled back into the ZXCD1000 at the TriangleA and TriangleB inputs. AC coupling ensures symmetrical operation resulting in minimal system DC offsets. TriangleA is connected to one of the inputs of a comparator and TriangleB is connected to one of the inputs of a second comparator. The other inputs of these two comparators are connected to the AudioA and AudioB inputs, which are anti-phase signals externally derived from the audio input. The triangular wave is an order higher in frequency than the audio input (max 20kHz). The outputs of the comparators toggle every time the TriangleA/B and the (relatively slow) AudioA/B signals cross.
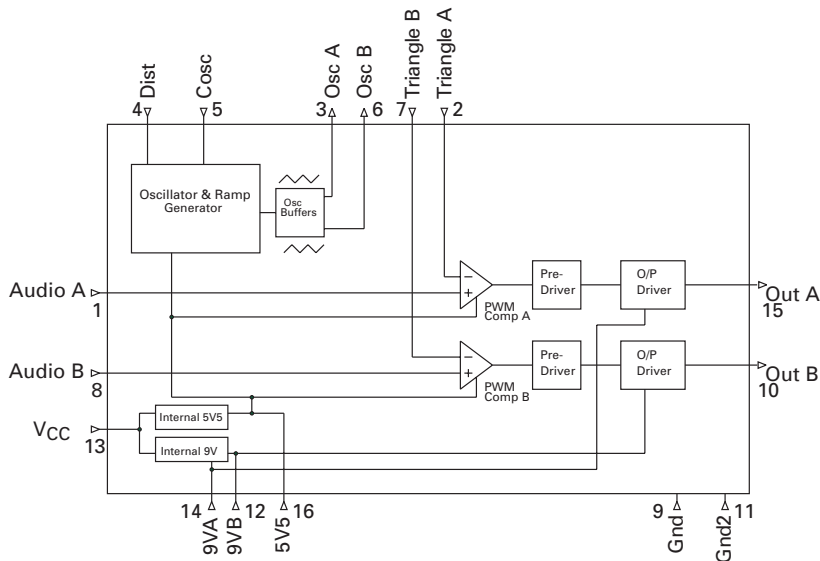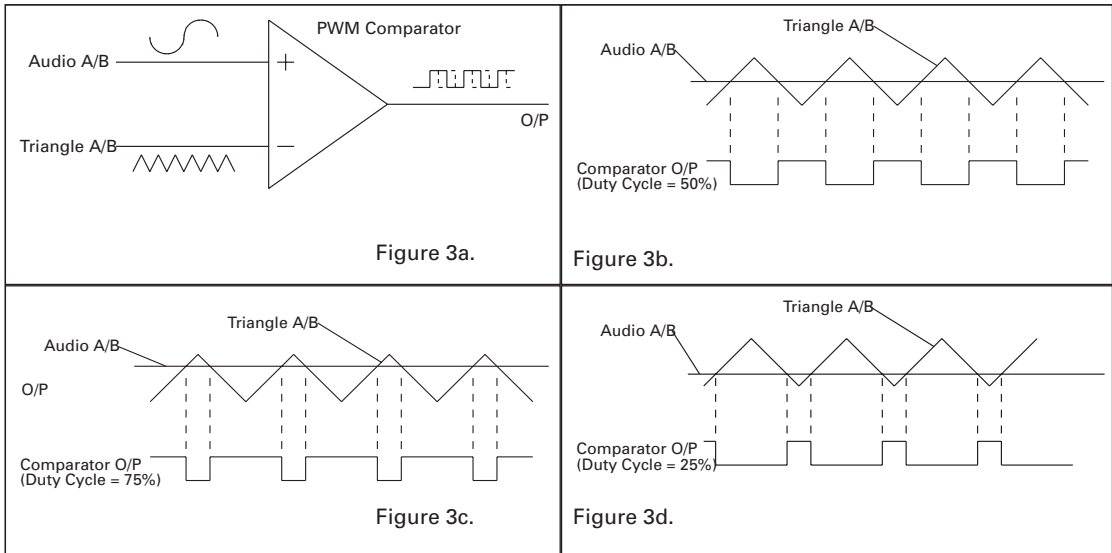

Figure 2.
Functional Block Diagram

Figure 3a.

Figure 3b.
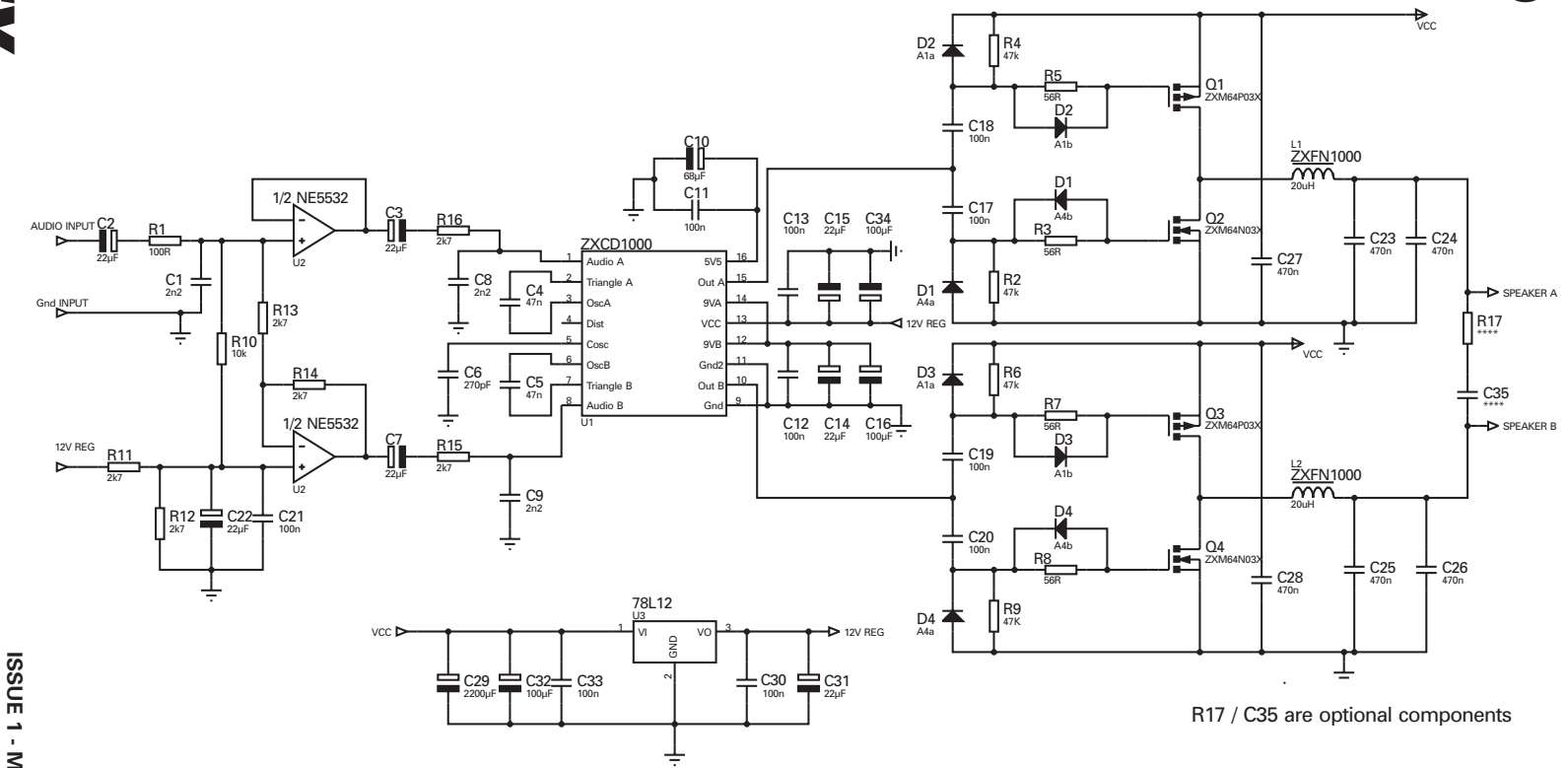

Figure 3c.

Figure 3d.

Figures 3a,3b,3c and 3d
The audio input Pulse Width Modulates the comparator output.

With no audio input signal applied, the AudioA/B inputs are biased at the mid-point of the triangular wave, and the duty cycle at the output of the comparators is nominally 50%. As the AudioA/B signal ascends towards the peak level, the crossing points with the (higher frequency) triangular wave also ascend. The comparator monitoring these signals exhibits a corresponding increase in output duty cycle. Similarly, as the AudioA/B signal descends, the duty cycle is correspondingly reduced. Thus the audio input Pulse Width Modulates the comparator outputs. This principle is illustrated in Figures 3a, b, c and d. The comparator outputs are buffered and used to drive the OutA and OutB outputs. These in turn drive the speaker load (with the audio information contained in the PWM signal) via the off chip output bridge and single stage L-C filter network.

The ramp amplitude is approximately 1V. The AudioA, AudioB, TriangleA and TriangleB inputs are internally biased to a DC voltage of approximately VCC/5. The mid - point DC level of the OscA and OscB triangular outputs is around 2V. The triangular wave at the Cosc pin traverses between about 2.7Vand 3.8V and the dist pin exhibits a roughly square wave from about 1.4V to 2V. (The above voltages may vary in practice and are included for guidance only).

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Figure 4
Zetex Class D 25W Mono Open Loop Solution

R17 / C35 are optional components

Class D 25W Mono Open Loop (Bridge Tied Load - BTL) Solution – Circuit Description

Proprietary circuit design and high quality magnetics are necessary to yield the high THD performance specified. Deviation from the Zetex recommended solution could significantly degrade performance.

The speaker is connected as a Bridge Tied Load (BTL). This means that both sides of the speaker are driven from the output bridge and therefore neither side of the speaker connects to ground. This allows maximum power to be delivered to the load, from a given supply voltage. The supply voltage for this solution is nominally 16V.

A schematic diagram for the solution is shown in Figure 4. The audio input is AC coupled and applied to a simple R-C (R1 and C1) low pass filter and a phase splitter built around the NE5532 dual op-amp. One of these op-amps is configured as a voltage follower and the other as a X1 inverting amplifier. This produces in phase and inverted signals for application to the ZXCD1000. The op-amp outputs are AC coupled into the ZXCD1000 Audio A and Audio B inputs via simple R-C low pass filters (R16/C8 and R15/C9). The op-amps are biased to a DC level of approximately 6V by R11 and R12.

The Pulse Width Modulated (PWM) outputs, OutA and OutB, which contain the audio information, are AC coupled and DC restored before driving the Zetex ZXM64P03X and ZXM64N03X PMOS and NMOS output bridge FET's. AC coupling is via C17, C18, C19 and C20. DC restoration is provided by the D2(A1a)/R4, D1(A4a)/R2 and D3(A1a)/R6, D4(A4a)/R9 components. This technique allows the output stage supply voltage to be higher than the high level of the OutA and OutB outputs (approximately 8.5V), whilst still supplying almost the full output voltage swing to the gates of the bridge FET's (thereby ensuring good turn on). This can be exploited to yield higher power solutions with higher supply voltages – this is discussed later.

The resistor/diode combinations (R5/D2(A16), R3/D1(A46), R7/D3(A16) and R8/D4(A46)) in series with the bridge FET gates, assist in controlling the switching of the bridge FET's. This design minimises shoot through currents whilst still achieving the low distortion characteristics of the system.

The purpose of the (ZXFN1000) inductors in conjunction with the output capacitors C23, C24, C25 and C26 is to low pass filter the high frequency switching PWM signal that comes from the bridge. Thus the lower frequency audio signal is recovered and is available at the speakerA and speakerB outputs across which the speaker should be connected. The ZXFN1000 magnetics form an integral part of, and are specially designed for, the Zetex solution.

The optional components R17 and C3 form a Zobel network. The applicability of these depends upon the application and speaker characteristics. Suggested values are 47nF and 10 ohms

Efficiency

The following plots show the measured efficiency of the Zetex solution at various power levels into both 4Ω and 8Ω loads. As a comparison, typical efficiency is plotted for a class A-B amplifier. They clearly demonstrate the major efficiency benefits available from the Zetex class D solution.
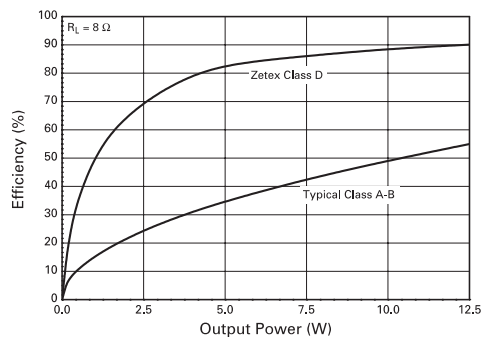
Output Stage Efficiency v Power

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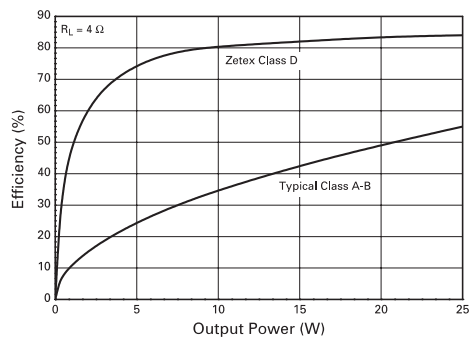
ZXCD1000

Class D 25W Mono Open Loop (Bridge Tied Load - BTL) Solution
– PCB description and Operation.

The top copper, the bottom copper and the silk screen (top) are shown in Figures 5, 6 & 7 respectively, for the double sided PCB implementation of the applications circuit of Figure 4. A component listing is given in the BOM (Bill of Materials) table. Gerber files for this solution are available from Zetex Plc.

The board operates from a 16V (nom.) supply which should be applied to the underside of the supply decoupling capacitor C29. The audio input and speaker connections should be made to the solder pads indicated on Figure 7. The audio input should have a maximum amplitude of approximately 1V pk-pk. For diagnostic purposes, the speaker outputs can be monitored single-endedly with respect to ground with an oscilloscope (or other instrument) if desired. However remember that the speaker is connected as a Bridge Tied Load, therefore any results obtained in this manner, are not valid for assessing performance. The true performance depends upon some differential cancellation across the speaker load. To view the differential output across speakerA and speakerB, a floating monitor must be used i.e. neither side of the speaker should be grounded! For example, this can be achieved with a two channel oscilloscope by monitoring the speakerA and speakerB outputs, and using the invert and add functions.
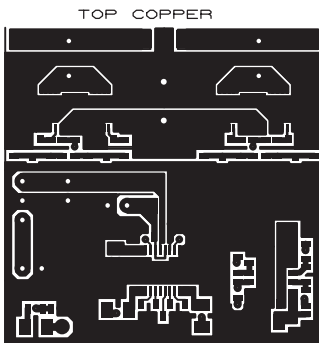

Figure 5.
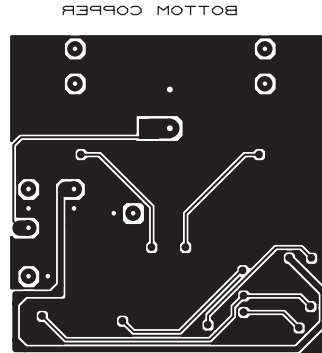Class D 25W Mono O.L. PCB Top Copper (Actual Size)

Figure 6.
Class D 25W Mono O.L. PCB Bottom Copper (Actual Size)

The exposed pad on the underside of the ZXCD1000 eQSOP package should be soldered down to the PCB. This in conjunction with vias and top and bottom copper areas, functions as a heat sink.
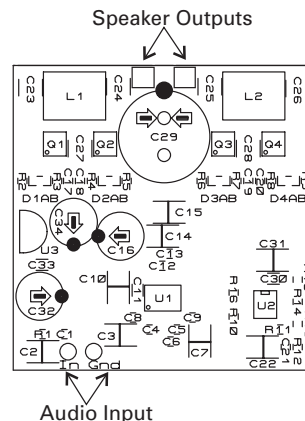

Figure 7.
Class D 25W Mono O.L. PCB
Silk Screen (Actual Size)

Plots of typical performance for the solution are shown in the included graphs. As previously stated, a very important feature of the Zetex solution is that the residual distortion is almost totally free of any crossover artifacts. This lack of crossover distortion sets the ZXCD1000 solutions quite apart from most other presently available low cost solutions, which in general suffer from severe crossover distortion problems.

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It is well known that this kind of distortion is particularly unpleasant to the listener. The two scope traces clearly show the lack of such artifacts with the Zetex solution
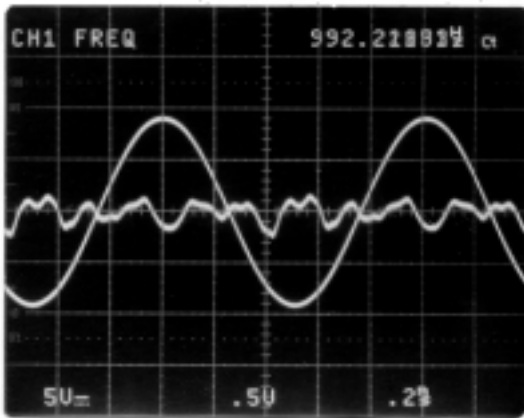
ZETEX Class D Solution. (10W into 4Ω)
Note lack of Crossover Artifacts
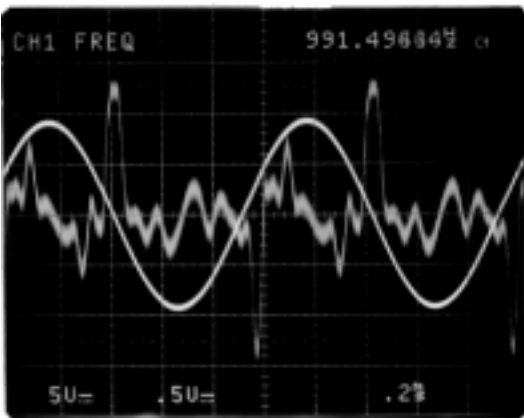
Typical Class D Solution.
Note Large Crossover Artifacts

Other Solutions - Stereo, Closed Loop and Higher Powers.

STEREO

It is possible to duplicate the above solution to give a 2 channel stereo solution. However if the oscillator frequencies are not locked together, a beat can occur which is acoustically audible. This is undesirable. A stereo solution which avoids this problem can be achieved by synchronising the operating frequencies of both ZXCD1000's class D controller IC's, by slaving one device from the other. This is illustrated in Figure 8.
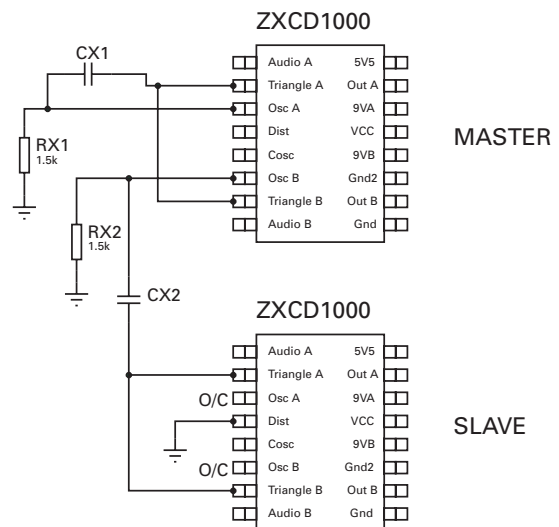
Figure 8.
Frequency sync for Stereo Apps.

Here OscA on the master is used to drive both TriangleA and TriangleB inputs on the master. OscB on the master is used to drive both TriangleA and TriangleB inputs on the slave. In order to achieve the increased drive capabilty required by the OscA/B outputs on the master, 1.5kΩ pull down resistors are added from these pins to ground. The slave oscillator is disabled by connecting pin 4 (dist) to ground. Great care must be taken when linking the triangle from the master to the slave. Any pickup can cause slicing errors and result in increased distortion. The best connection method is to run two tracks, side by side, from the master to the slave. One of these tracks would be the triangle itself, and the other would be the direct local ground linking the master pin9 ground to the slave pin 9 ground.
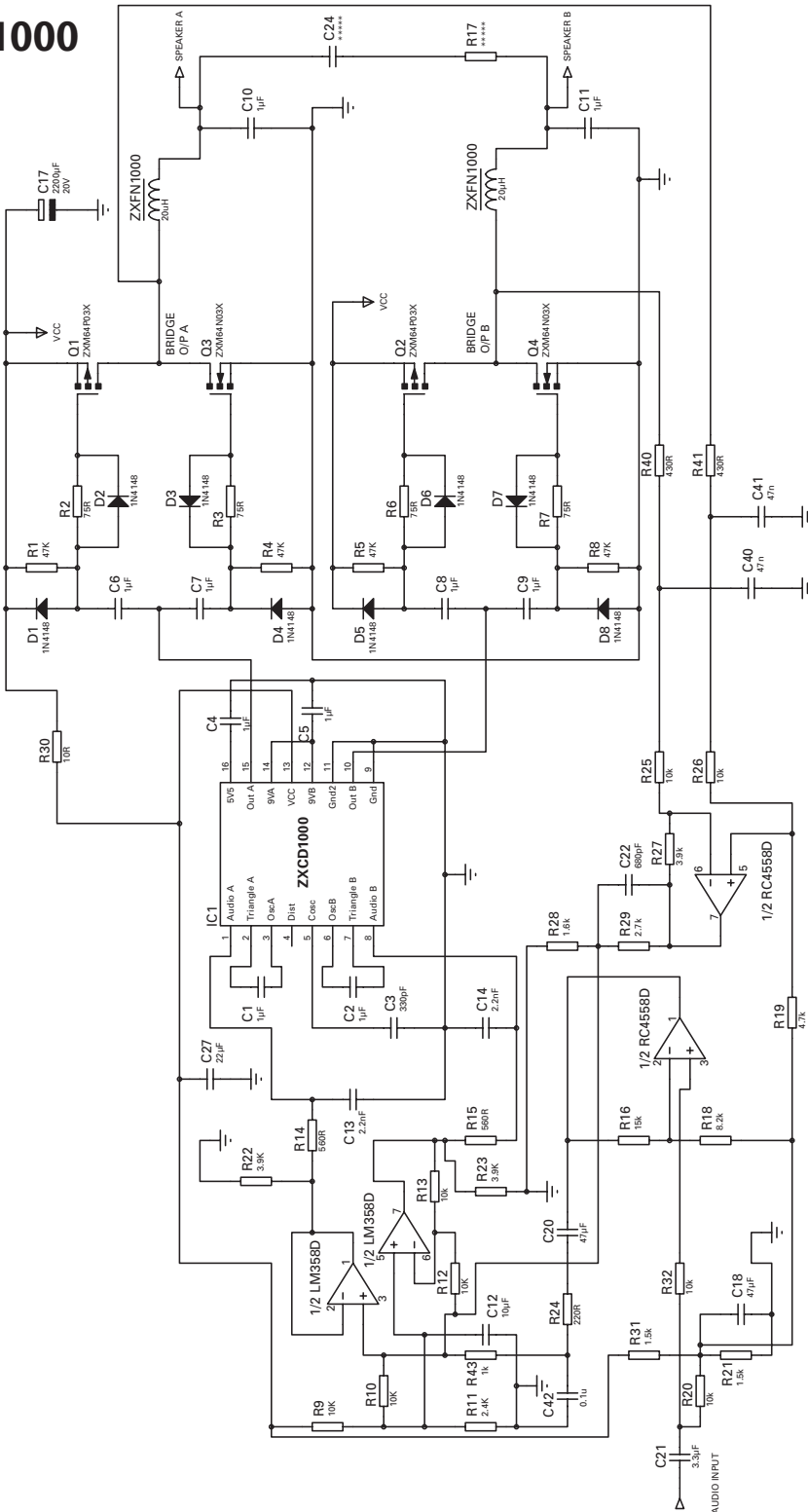
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ZXCD1000

Figure 9.
25W Mono with Feedback

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Class D 25W Mono Bridge Tied Load (BTL) Solution with Feedback – Circuit Description

With the addition of feedback (hence closed loop solution) it is possible to obtain even better THD performance. A schematic diagram for this is shown in Figure 9. Again proprietary circuit and special magnetic design is necessary to yield the high THD performance and deviation from this could significantly reduce performance.

Much of the circuitry is the same as described for the open loop solution. The main differences being a consequence of using the feedback circuitry. The input and feedback circuitry is shown separately in Figure 10 and is now described. The audio input is ac coupled and applied to an op-amp (1/2 of RC4558D) configured as a non–inverting amplifier with a gain of approximately 2.8. The op-amp input is tied to a DC level of approximately VCC/2. Feedback is applied differentially from the bridge outputs via the other half of the RC4558D op-amp. A portion of the single ended output from this op-amp is subtracted from the output of the non-inverting op-amp output above. Overall negative feedback is applied due to the polarity and connection of the signals involved.

The audio signal from the above circuitry is applied to a phase splitter (see Figure 11) as was done for the open loop solution. This is built around the other LM3580 dual op-amp. One of these op-amps is configured as a voltage follower and the other as a X1 inverting amplifier. This produces in phase and inverted signals for application to the ZXCD1000 Audio A and Audio B inputs respectively.

The output circuitry downstream of the ZXCD1000 is as described for the open loop solution, but the components may be slightly different (and have different numbering).

Higher Power Solutions

With some modifications the applications solutions can be extended to give 50W or even higher output powers. A 50W solution can be implemented with a circuit very similar to the 25W solution. The main differences being the supply voltage and the output magnetics. The magnetics for 50W are necessarily larger than required for 25W in order to handle the higher load currents. For 50W operation the supply voltage to the circuit is nominally 25V. However the maximum supply voltage to the ZXCD1000 class D controller IC is 20V, hence a voltage dropper is required. This could be done, for example, as in the open loop solution described previously. In addition, for the closed loop solution, slightly modified feedback resistor ratios are required.

The ZXCD1000 class D controller IC is inherently capable of driving even higher power solutions, with the appropriate external circuitry. However as stated above the maximum supply voltage to the ZXCD1000 class D controller IC is 20V and the higher supply voltages must therefore be dropped. Also due consideration must be given to the ZXCD1000 output drive levels and the characteristics of the bridge MOSFET's. The latter must be sufficiently enhanced by the OutA and OutB outputs to ensure the filter and load network is driven properly. If the gate drive of the ZXCD1000 is too low for the chosen MOSFET then the OUTA and OUTB signal must be buffered using an appropriate MOSFET driver circuit. Additionally, suitable magnetics are essential to achieve good THD performance.

Package details

The ZXCD1000 is available in a 16 pin eQSOP package. The exposed pad on the underside of the package should be soldered down to an area of copper on the PCB, to function as a heatsink. The PCB should have plated through vias to the underside of the board, again connecting to an area of copper.
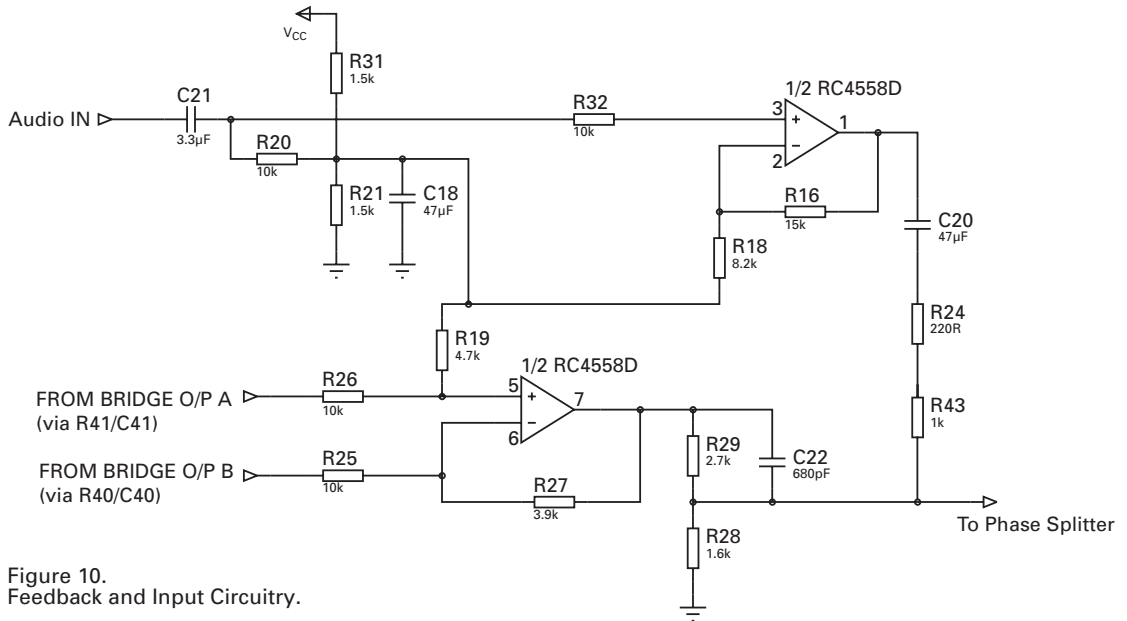
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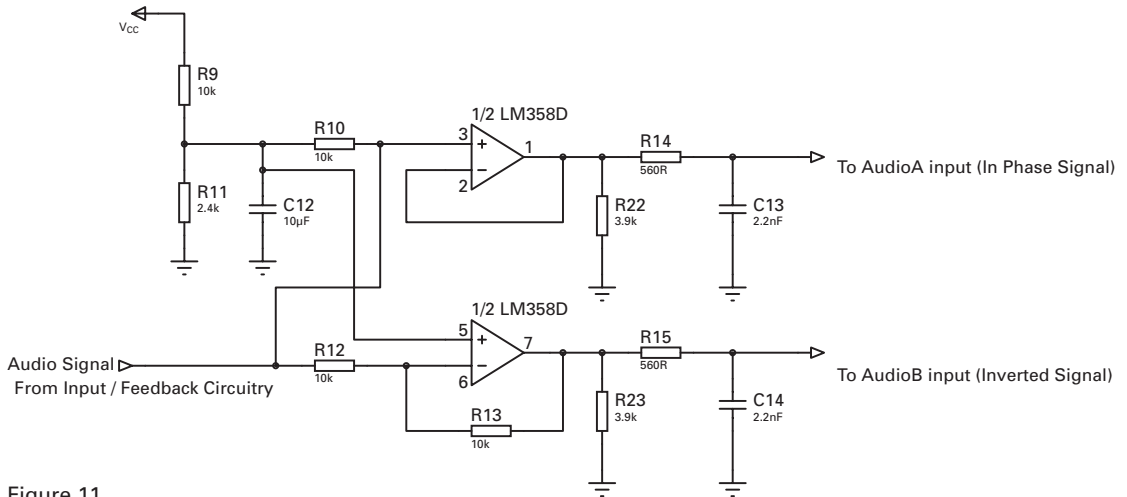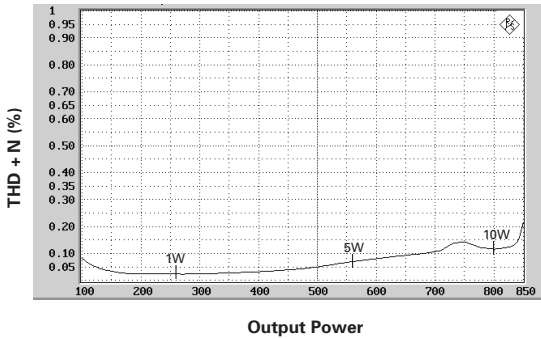

Figure 10.
Feedback and Input Circuitry.

Figure 11.
Phase Splitter

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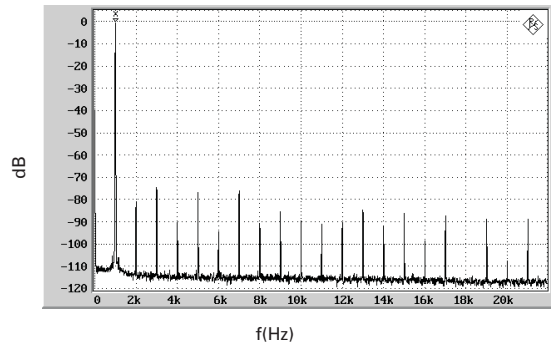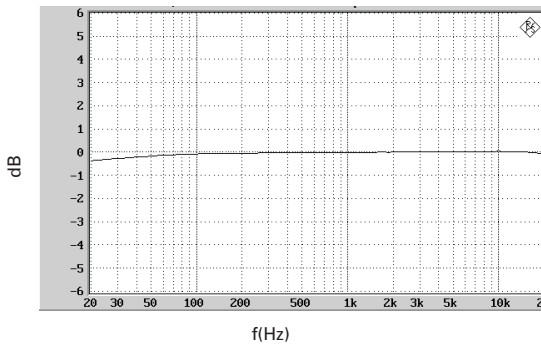
Typical performance graphs for the Zetex 25W open loop solution are shown here for both 4 and 8Ω loads. These graphs further demonstrate the true high fidelity performance achieved by the Zetex solutions.
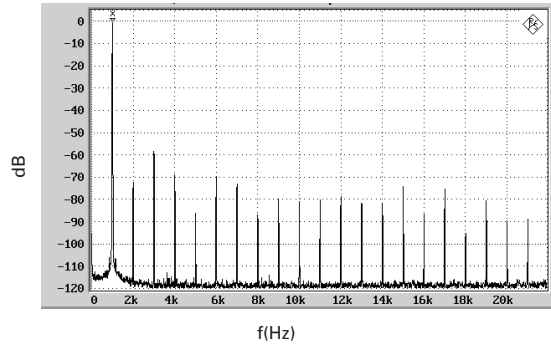

THD v Power into 8Ω at 1kHz
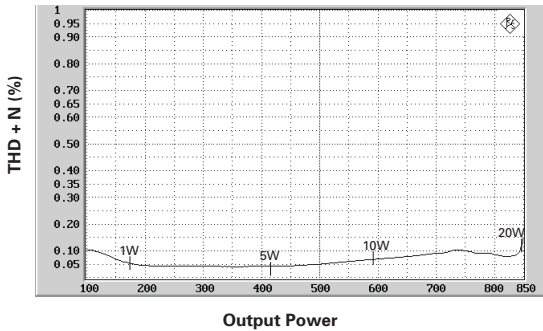

FFT of distortion and noise floor at 1W (8Ω load)
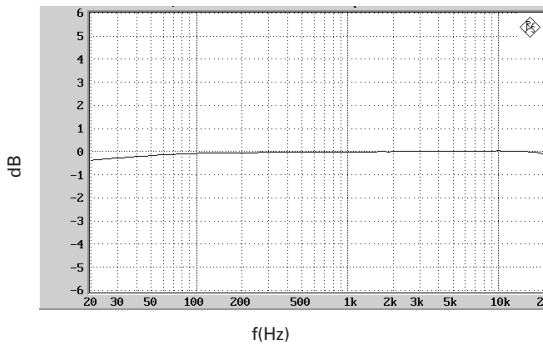

Frequency response (8Ω load)

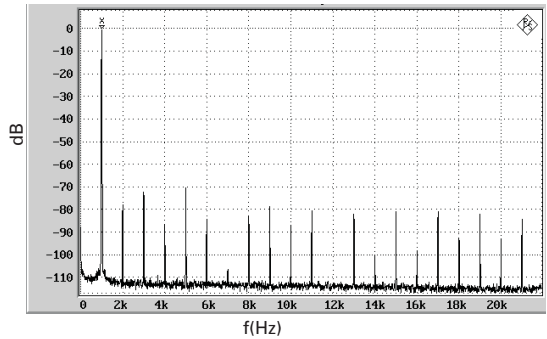**FFT of distortion and noise floor at 10W (8Ω load)**

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THD v Power into 4Ω at 1kHz

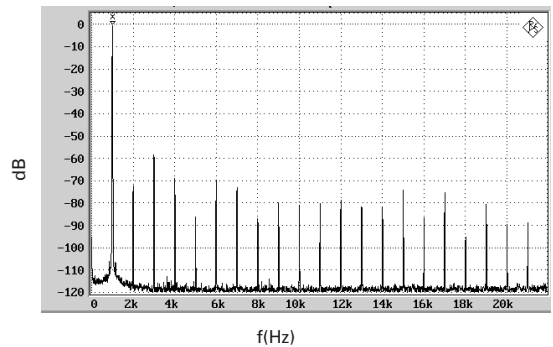**FFT of distortion and noise floor at 1W (4Ω load)**

Frequency response (4Ω load)

Note roll off.
This can be corrected by using an alternative values for output filter components.

FFT of distortion and noise floor at 20W (4Ω load)

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B.O.M. Table for 25W Mono Open Loop Solution

PCB ID	Value	Case	Notes
R1	100R	SMD 0805	
R2	47K	SMD 0805	
R3	56R	SMD 0805	
R4	47K	SMD 0805	
R5	56R	SMD 0805	
R6	47K	SMD 0805	
R7	56R	SMD 0805	
R8	56R	SMD 0805	
R9	47K	SMD 0805	
R10	10K	SMD 0805	
R11	2K7	SMD 0805	
R12	2K7	SMD 0805	
R13	2K7	SMD 0805	
R14	2K7	SMD 0805	
R15	2K7	SMD 0805	
R16	2K7	SMD 0805	
C1	2n2 COG	SMD 0805	
C2	22µF 10V	SMD Tant B	
C3	22µF 6V3	SMD Tant B	
C4	47n X7R	SMD 0805	
C5	47n X7R	SMD 0805	
C6	270pF COG	SMD 0805	
C7	22µF 6V3	SMD Tant B	
C8	2n2 COG	SMD 0805	
C9	2n2 COG	SMD 0805	
C10	68µF 6V3	SMD Tant B	
C11	100n X7R	SMD 1206	
C12	100n X7R	SMD 0805	
C13	100n X7R	SMD 0805	
C14	22µF 10V	SMD Tant B	
C15	22µF 16V	SMD Tant B	
C16	100µF 10V	std. Dia 6.3mm	
C17	100n X7R	SMD 0805	
C18	100n X7R	SMD 0805	
C19	100n X7R	SMD 0805	
C20	100n X7R	SMD 0805	
C21	100n X7R	SMD 0805	

PCB ID	Value	Case	Notes
C22	22µF 6V3	SMD Tant B	
C23	470n	SMD 1812	
C24	470n	SMD 1812	
C25	470n	SMD 1812	
C26	470n	SMD 1812	
C27	470n	SMD 1812	
C28	470n	SMD 1812	
C29	2200µF 16V	std. Dia 12.5mm	
C30	100n X7R	SMD 1206	
C31	22µF 16V	SMD Tant B	
C32	100µF 16V	std. Dia 6.3mm	
C33	100n X7R	SMD 1206	
C34	100µF 16V	std. Dia 6.3mm	
U1	ZXCD1000		
U2	NE5532	SMD SO 8	
U3	78L12	TO92	
Q1	ZXM64P03X	SMD MSOP 8	
Q2	ZXM64N03X	SMD MSOP 8	
Q3	ZXM64P03X	SMD MSOP 8	
Q4	ZXM64N03X	SMD MSOP 8	
D1	BAV70	SMD SOT23	A4-Common Cathode
D2	BAW56	SMD SOT23	A1-Common Anode
D3	BAW56	SMD SOT23	A1-Common Anode
D4	BAV70	SMD SOT23	A4-Common Cathode
L1	20µH (ZXFN1000)	std.	Custom core
L2	20µH (ZXFN1000)	std.	Custom core

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PACKAGE DIMENSIONS

TOP VIEW

END VIEW

BOTTOM VIEW

EXPOSED PAD

SEE DETAIL "A"

SIDE VIEW

SEATING PLANE

DETAIL "A"

SEATING PLANE
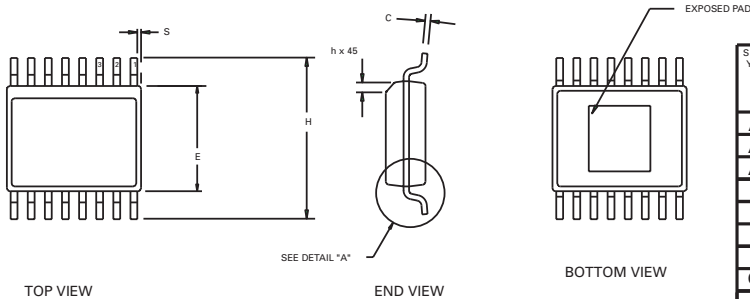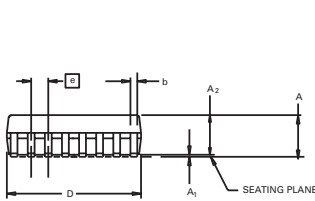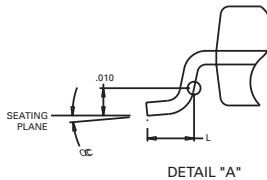
SYMBOL	DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.
A	.058	.061	.066
A$_1$	.001	.003	.005
A$_2$	.055	.058	.061
b	.008		.012
c	.007		.010
D	.189	.194	.196
E	.150	.154	.157
e	.025 BSC		
H	.228	.236	.244
h	.010	.013	.016
L	.016	.025	.035
S	.002	.005	.007
$\propto$	0	5	8

Zetex part ordering information (per channel)				
Qty per channel	Device	Description	Package	T&R Suffix
1	ZXCD1000EQ16	Class D modulator	eQSOP16	TA, TC
2	ZXFN1000	Custom magnetics		TA, TC
2	ZXM63N03X	N Channel MOSFET	MSOP8	TA, TC
2	ZXM63P03X	P Channel MOSFET	MSOP8	TA, TC

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