

FEATURES

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 μ A (Max.) @ $V_{DS} = 60V$
- Lower $R_{DS(ON)}$: 0.122 Ω (Typ.)

$$BV_{DSS} = 60 V$$

$$R_{DS(on)} = 0.155\Omega$$

$$I_D = 8.2 A$$

D-PAK I-PAK



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	60	V
I_D	Continuous Drain Current ($T_C=25^\circ C$)	8.2	A
	Continuous Drain Current ($T_C=100^\circ C$)	5.2	
I_{DM}	Drain Current-Pulsed ①	30	A
V_{GS}	Gate-to-Source Voltage	± 0	V
E_{AS}	Single Pulsed Avalanche Energy ②	58	mJ
I_{AR}	Avalanche Current ①	8.2	A
E_{AR}	Repetitive Avalanche Energy ①	1.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
P_D	Total Power Dissipation ($T_A=25^\circ C$) *	2.5	W
	Total Power Dissipation ($T_C=25^\circ C$)	18	W
	Linear Derating Factor	0.14	W/°C
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	°C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	6.81	°C/W
$R_{\theta JA}$	Junction-to-Ambient *	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

* When mounted on the minimum pad size recommended (PCB Mount).



Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	60	–	–	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	–	0.045	–	V/°C	$I_D=250\mu A$ See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	1.0	–	2.0	V	$V_{DS}=5V, I_D=250\mu A$
I_{GSS}	Gate-Source Leakage, Forward	–	–	100	nA	$V_{GS}=20V$
	Gate-Source Leakage, Reverse	–	–	-100		$V_{GS}=-20V$
I_{DSS}	Drain-to-Source Leakage Current	–	–	10	μA	$V_{DS}=60V$
		–	–	100		$V_{DS}=48V, T_C=125^\circ C$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	–	–	0.155	Ω	$V_{GS}=5V, I_D=4.1A$ ④
g_{fs}	Forward Transconductance	–	4.9	–	S	$V_{DS}=30V, I_D=4.1A$ ④
C_{iss}	Input Capacitance	–	265	345	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	–	100	115		
C_{rss}	Reverse Transfer Capacitance	–	37	45		
$t_{d(on)}$	Turn-On Delay Time	–	10	30	ns	$V_{DD}=30V, I_D=10A,$ $R_G=12\Omega$ See Fig 13 ④ ⑤
t_r	Rise Time	–	16	45		
$t_{d(off)}$	Turn-Off Delay Time	–	21	55		
t_f	Fall Time	–	15	40		
Q_g	Total Gate Charge	–	7.2	10	nC	$V_{DS}=48V, V_{GS}=5V,$ $I_D=10A$ See Fig 6 & Fig 12 ④ ⑤
Q_{gs}	Gate-Source Charge	–	2.6	–		
Q_{gd}	Gate-Drain("Miller") Charge	–	3.2	–		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	–	–	8.2	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	–	–	30		
V_{SD}	Diode Forward Voltage ④	–	–	1.5	V	$T_J=25^\circ C, I_S=8.2A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	–	50	–	ns	$T_J=25^\circ C, I_F=10A$
Q_{rr}	Reverse Recovery Charge	–	0.075	–	μC	$di_F/dt=100A/\mu s$ ④

Notes :

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
 ② $L=1\text{mH}, I_{AS}=8.2A, V_{DD}=25V, R_G=27\Omega$, Starting $T_J=25^\circ C$
 ③ $I_{SD} \leq 10A, di/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ C$
 ④ Pulse Test : Pulse Width = 250 μs , Duty Cycle $\leq 2\%$
 ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

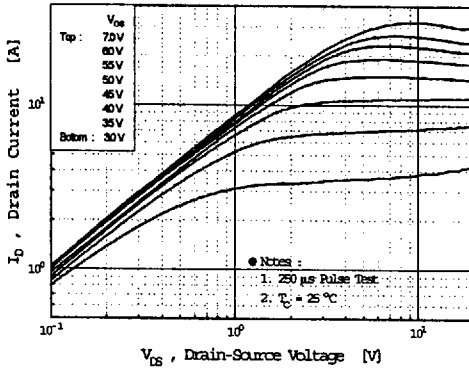


Fig 2. Transfer Characteristics

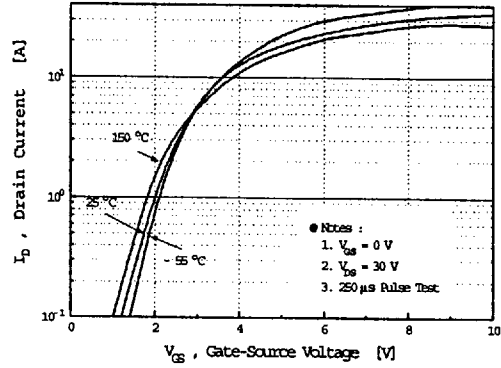


Fig 3. On-Resistance vs. Drain Current

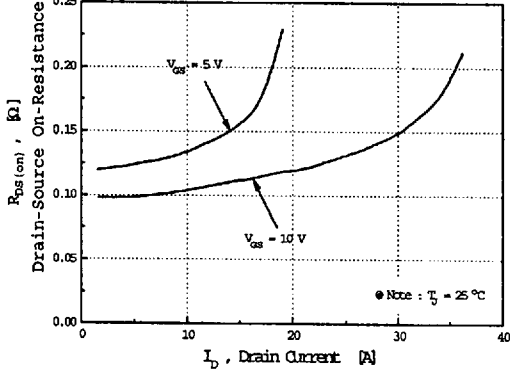


Fig 4. Source-Drain Diode Forward Voltage

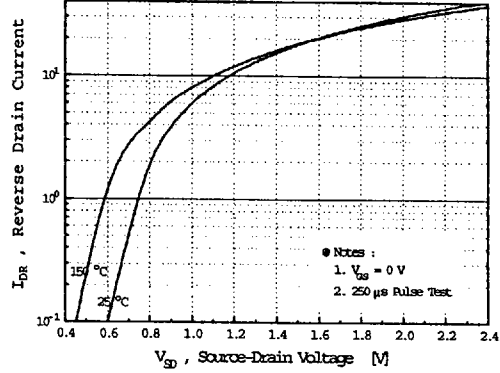


Fig 5. Capacitance vs. Drain-Source Voltage

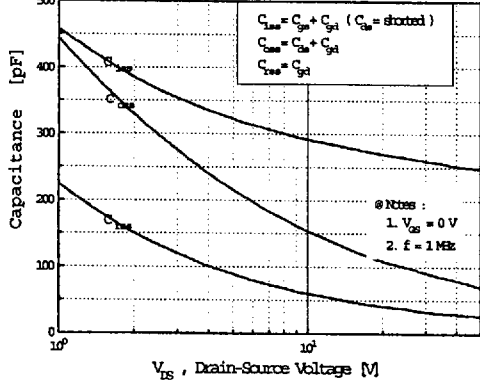


Fig 6. Gate Charge vs. Gate-Source Voltage

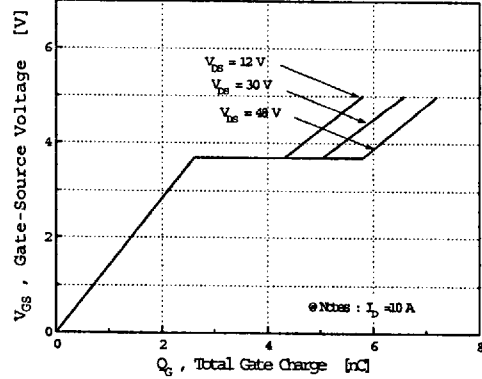


Fig 7. Breakdown Voltage vs. Temperature

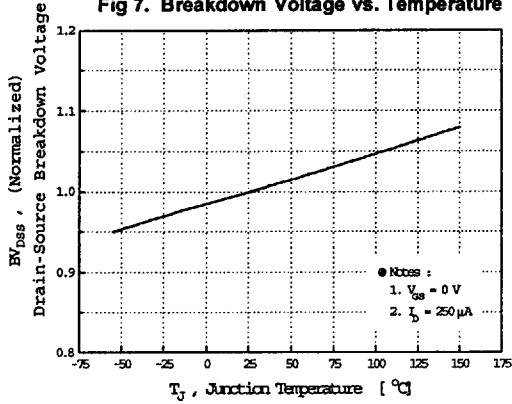


Fig 8. On-Resistance vs. Temperature

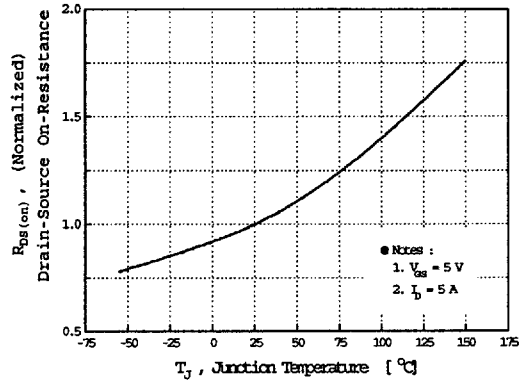


Fig 9. Max. Safe Operating Area

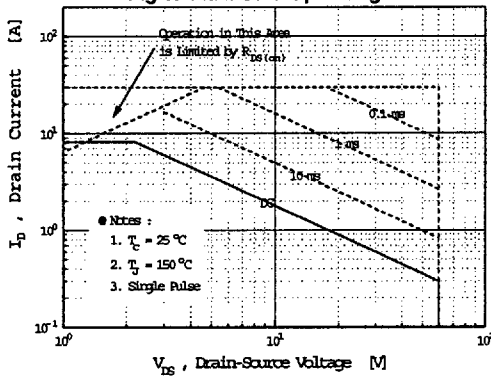


Fig 10. Max. Drain Current vs. Case Temperature

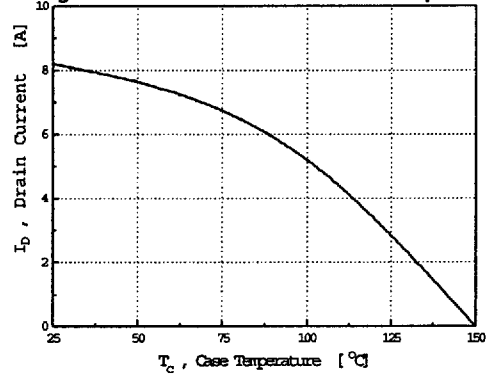


Fig 11. Thermal Response

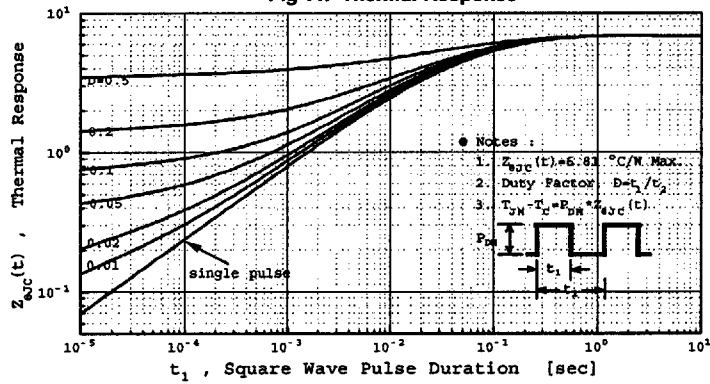


Fig 12. Gate Charge Test Circuit & Waveform

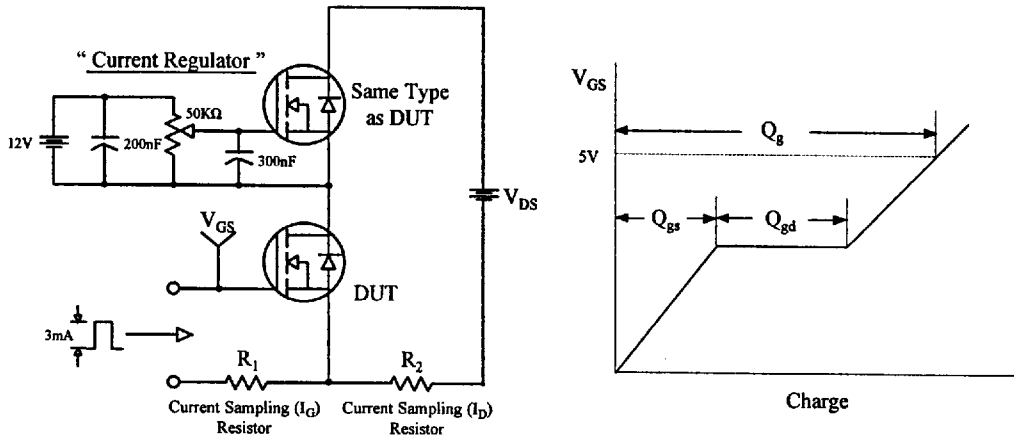


Fig 13. Resistive Switching Test Circuit & Waveforms

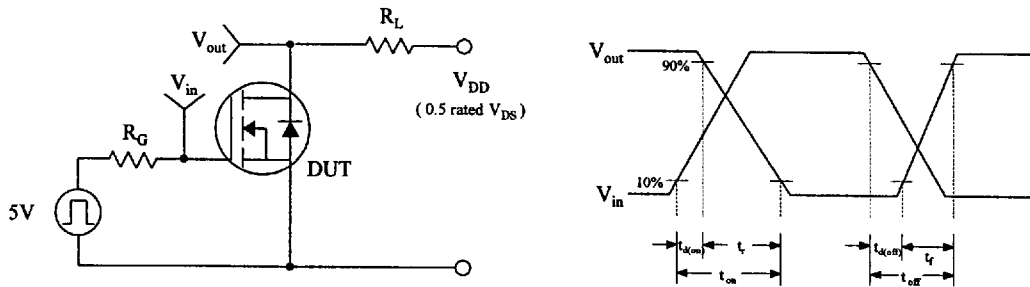


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

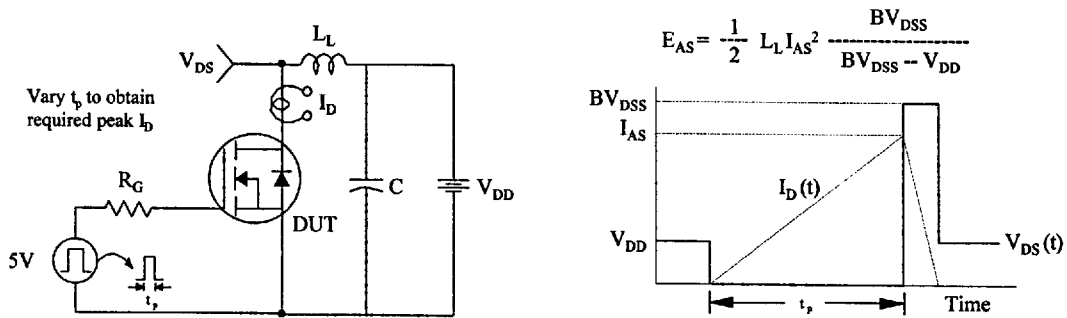


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

