METHOD AND APPARATUS FOR IMPROVED MOS GATING TO REDUCE MILLER CAPACITANCE AND SWITCHING LOSSES

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Patent Application No. 60/405,369 filed Aug. 23, 2002.

FIELD OF THE INVENTION

The present invention relates to semiconductors, and more particularly to metal-oxide semiconductor field effect transistors (MOSFETs).

DESCRIPTION OF THE RELATED ART

MOSFETs are used extensively in switching applications, such as, for example, switching power supplies, practically to the exclusion of other types of transistors. MOSFETs are suited to such switching applications due to their relatively high switching speed and low power requirements. However, the dynamic losses in MOSFETs represent a large percentage of the total losses in DC-to-DC converters. The dynamic losses are directly proportional to the device rise and fall times which are, in turn, proportional to the gate-to-drain capacitance, i.e., the Miller capacitance, of the device (C_{GD} or Q_{GD}).

The Miller capacitance, as shown in FIG. **3**, also results in a "flat" region in the gate curve of conventional MOSFETs. This flat region, referred to as the Miller region, is representative of the device transitioning from a blocking state to a conducting state or from a conducting state to a blocking state. It is in the Miller region that most of the switching losses occur since the device current and voltage are high. Reducing the Miller capacitance will reduce the time the device requires to undergo the transition from conduction to blocking or vice versa, and thereby reduce switching losses.

The Miller capacitance is reduced by reducing the area over which the gate and drain regions overlap. In prior art devices, this overlap area includes the bottom of the gate trench. Thus, many prior art attempts to reduce the Miller capacitance have focused on narrowing the trench width to thereby reduce the width of the trench bottom and thus the overlap area. However, the ability to further reduce trench width is limited by the ability to etch narrow trenches, and the corresponding need to be able to fill the narrow trenches with gate electrode material.

Therefore, what is needed in the art is a MOSFET having a reduced miller capacitance, and therefore reduced switching losses.

Moreover, what is needed in the art is a MOSFET having a reduced Miller capacitance for a given trench width.

SUMMARY OF THE INVENTION

The present invention provides a gate structure for a semiconductor device.

The invention comprises, in one form thereof, a switching electrode and a shielding electrode. Respective portions of the shielding electrode are disposed above said drain region and said well region. A first dielectric layer is disposed between the shielding electrode and the drain and well regions. The switching electrode includes respective portions that are disposed above said well region and said source region. A second dielectric layer is disposed between the switching electrode and the well and source regions. A third dielectric layer is disposed between the shielding electrode and the switching electrode.

An advantage of the present invention is that for a given trench width, Miller capacitance of the semiconductor device is reduced relative to a prior art device.

A further advantage of the present invention is that the device switching times and switching losses are reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned and other features and advantages of this invention, and the manner of attaining them, will become apparent and be better understood by reference to the following description of one embodiment of the invention in conjunction with the accompanying drawings, wherein:

FIG. **1** is a cross-sectional schematic view of a prior art trench metal-oxide-semiconductor-gated (MOS-gated) structure;

FIG. **2** is a cross-sectional schematic view of one embodiment of a MOS-gated structure of the present invention;

FIG. **3** is a plot of the gate switching waveforms for a conventional MOS-gated structure and the MOS-gated structure of FIG. **2**;

FIG. **4** is a plot of the typical net doping profile of the well of the MOS-gated structure of FIG. **2**;

FIG. **5** is a cross-sectional schematic view of one embodiment of a planar MOSFET of the present invention;

FIG. **6** is a cross-sectional schematic view of a second embodiment of a planar MOSFET of the present invention;

FIG. **7** is a cross-sectional schematic view of one embodiment of a lateral MOSFET of the present invention;

FIG. **8** is a cross-sectional schematic view of a second embodiment of a lateral MOSFET of the present invention;

FIG. **9** is a cross-sectional schematic view of one embodiment of a trench MOS-gated structure of the present invention; and

FIG. **10** is a process diagram illustrating one embodiment of a process by which the device of FIG. **2** is fabricated.

Corresponding reference characters indicate corresponding parts throughout the several views. The exemplifications set out herein illustrate one preferred embodiment of the invention, in one form, and such exemplifications are not to be construed as limiting the scope of the invention in any manner.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring now to the drawings and particularly to FIG. **1**, there is shown in cross-section a schematic view of a prior art trench-gated MOSFET device. MOSFET device **10** includes drain region **12**, well region **14**, body region **16**, source region **18**, gate region **20** and trench **24**, all of which are formed on substrate **26**.

More particularly, N+ type substrate **26** includes upper layer **26*a*** within which is formed N− drain region **12**. P-type well region **14** overlies drain region **12**. At an upper surface (not referenced) of upper layer **26*a*** and within a portion of well region **14** is defined a heavily doped P+ body region **16**. Also formed at the upper surface of upper layer **26*a*** and within a portion of well region **14**, and proximate trench **24**, is formed heavily doped N+ source region **18**. The sidewalls and bottom (not referenced) of trench **24** are lined with dielectric material **28**, such as, for example, oxide. Gate