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Examination of reverse recovery losses in a synchronous buck converter circuit

Introduction

A synchronous buck converter is a commonly used topology for step down DC to DC conversion applications. A schematic of this topology is shown in Fig. 1. The step down ratio V_{out}/V_{in} is controlled by changing the duty cycle of the control FET (Q1). To improve efficiency it is desirable to have the sync FET (Q2) turned on when Q1 is turned off. However, due to finite FET turn-on and turn-off time the state of two FETs cannot be switched instantaneously.

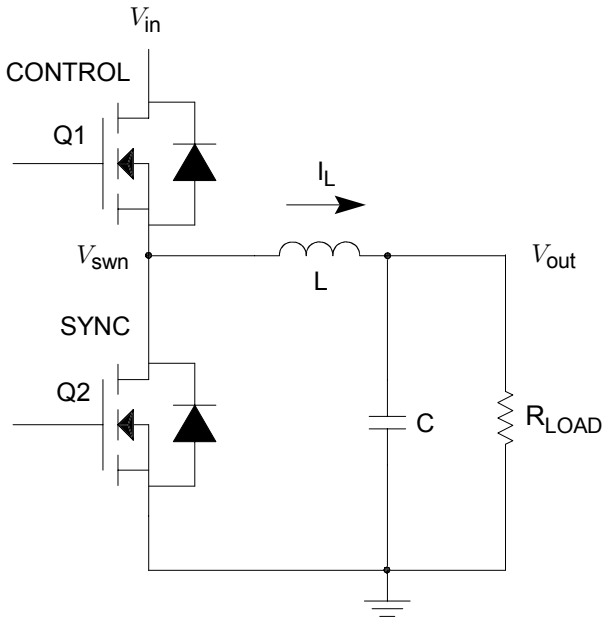

Figure 1. PN body diode in parallel with the FETs. To maintain current flow through inductor L after the control FET switches off, the bottom diode will conduct until the sync FET turns on.

A state diagram depicting the possible switching modes of a sync buck converter is shown in Fig. 2. Under normal operation of the sync buck circuit, the switching sequence is B-A-C-A-B. The dwell time in state A is commonly referred to as dead time. To improve efficiency the designers would like to reduce the dead time to a minimal duration. However, if the dead time is reduced below the turn-on or turn-off time of the FETs, the switches may go to state D, instead of state A. State D is often referred to as shoot-through when both transistors are on at the same time shorting the input supply. This state should be avoided as it can result in significant loss of efficiency and could damage the FETs.

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The switches drive an inductive load as shown in Fig. 1. When the circuit transitions from state B to A, the current through the inductor cannot instantly drop to zero and will continue to flow through the PN body diode of sync FET Q2. The diode will conduct the current through the inductor until the bottom FET can be turned on in state C. Generally, during state A, current flows through the diode. In this paper, we would like to discuss the impact of conduction through the diode on the efficiency of the sync buck converter.

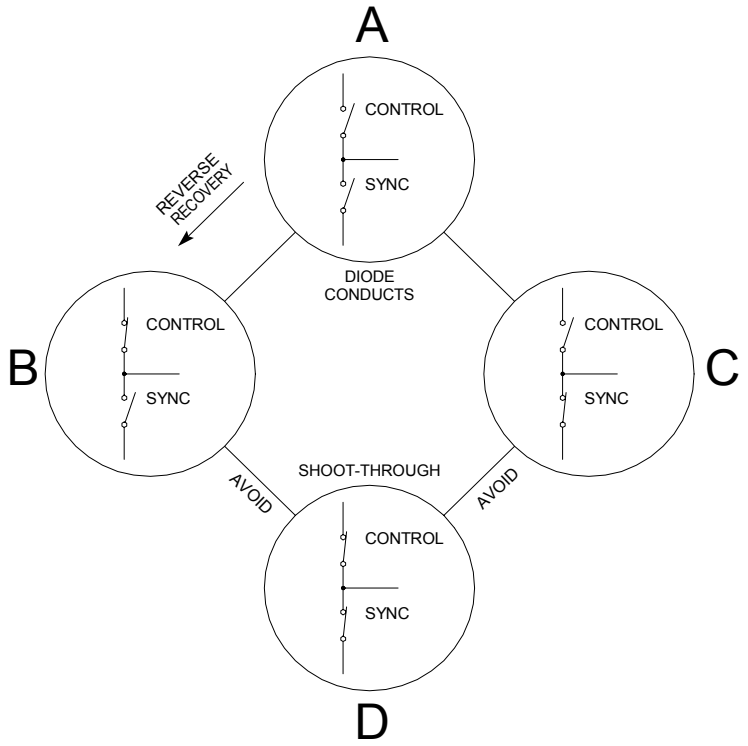

Figure 2. State diagram showing possible switching states in a sync buck circuit. The preferred sequence is B-A-C-A-B. If timing is skewed, state D may be entered causing a shoot-through condition which lowers efficiency and may damage the switching transistors.

Conduction Loss

The presence of the diode results in diode conduction losses which are proportional to the forward voltage V_F multiplied by the current through the diode. A diode with a smaller V_F would have a proportionally smaller conduction loss.

Reverse Recovery Loss

Another source of power loss due to the presence of the diode in the circuit is a direct result of the diode reverse recovery. Reverse recovery results when the forward conducting diode is taken from forward to reverse bias [1]. Fig. 3a shows typical reverse recovery waveforms for an inductively loaded diode [2]. Period I of the diode conduction characteristics of Fig. 3a shows a diode conducting a current I_F in the forward direction with a forward voltage drop of V_F. When the diode is reverse biased in period II the

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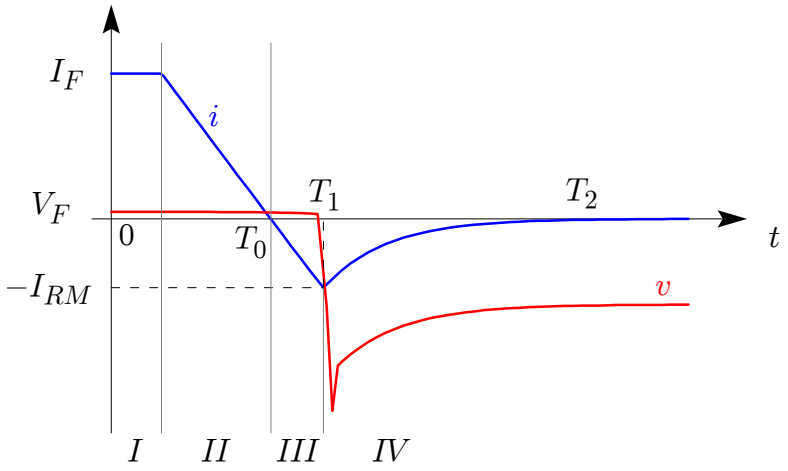
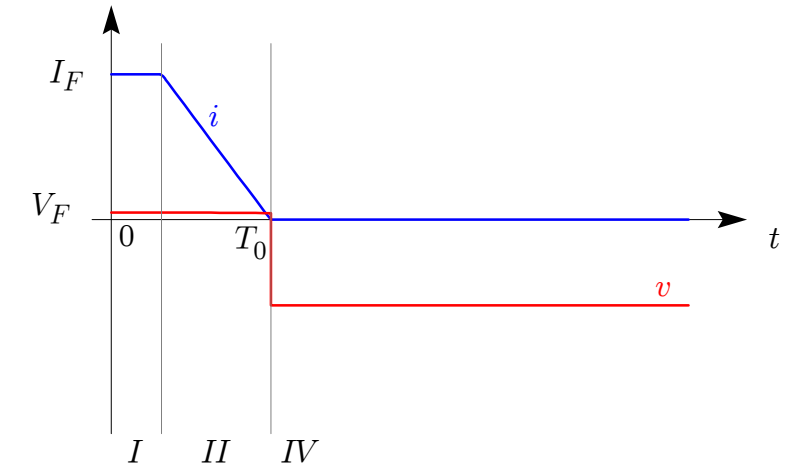
series inductance within the circuit continues to force current through the diode. The voltage V_F will remain approximately constant as the current reaches zero at time T_0. In period III the stored charges within the diode PN junction are depleted, resulting in a



(a) PN diode turn-off results in reverse recovery waveforms



(b) ideal diode turn-off does not exhibit reverse recovery effects

Figure 3. Diode reverse recovery waveforms showing current and voltage as a function of time. The reverse recovery waveforms are strikingly different from the ideal diode turn-off characteristics. Reverse recovery decreases the circuit efficiency.

large negative current which peaks at a value of I_{RM} at time T_1. The diode acts as an energy source during period III, delivering energy to the circuit. When the stored charge is depleted across the junction, the voltage drop across the diode snaps in the direction of the reverse bias and after a brief overshoot will settle at the steady-state reverse biased value in period IV. In the reverse recovery case, power is dissipated during period IV until equilibrium is restored within the PN junction and the diode current drops to zero.

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To illustrate the consequences of reverse recovery, examine the turn-off characteristics of an ideal diode as shown in Fig. 3b. For an inductive load, the current slope di/dt will be finite, but at T_0 the current will stay at zero and the voltage will jump to the reverse bias voltage. Power is not dissipated in the ideal diode during period IV because the current is zero.

From the state diagram of Fig. 2 it was shown that the transition to and from state A results in current flow through the diode. Transition from state A to B results in the diode switching off and the diode experiences reverse recovery. The transition from state A to C switches the diode off, but the sync switch in parallel with the diode clamps the reverse recovery behavior.

Reverse recovery effects on control FET

During the transition from state A to B, diode reverse recovery extends the time it takes for the switch node voltage to transition from $-V_F$ to V_{in} as the voltage across the diode is effectively held constant until reverse recovery current peaks in period III. In period IV the control FET is forced to supply not only the load current, but also the diode reverse recovery current. During period IV, switch node voltage rises reaching the steady state value of V_{in} after reverse recovery. The combination of delayed voltage drop across the control FET and increased current results in higher power dissipation. The control FET must be derated to handle the extra current during reverse recovery. Transition losses of the control FET are computed by integrating current through and voltage drop across the FET

$$P_{trans} = f_{sw} \int_0^{T_{trans}} (V_{\text{in}} - V_{\text{swn}})\, I_{\text{in}}\, dt \tag{1}$$

where the period of integration is the transition time T_{trans} and f_{sw} is the sync buck switching frequency. Reverse recovery increases the current I_{in} as well as the transition time T_{trans} which in turn may increase the transition losses in the control FET by as much as 50%.

Reverse recovery effects on sync FET

During the transition from state A to B, diode reverse recovery results in undesired current flowing in the diode during periods III and IV. During period IV, large voltages and currents are present across the diode. One method of estimating the losses in the diode due to this reverse recovery current is

$$P_{rr} = Q_{rr} V_{\text{in}} f_{sw} \tag{2}$$

where Q_{rr} is the reverse recovery charge as given in the manufacturer's data sheet, and f_{sw} is the switching frequency [3].

Several techniques have been developed by circuit designers to mitigate the effects of reverse recovery and improve efficiency. The magnitude of the reverse recovery current

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can be reduced by decreasing the slope di/dt by slowing down the turn-on time of the control FET. While reverse recovery losses may be reduced using this method, the transition losses will increase due to the slower turn-on of the control FET. Another method is to minimize the dead time in state A. Truncating the dead time will further reduce reverse recovery effects by limiting the energy storage in the body diode and associated parasitics. Some manufacturers have begun producing switching controllers that minimize the dead time to increase the overall efficiency. Limiting reverse recovery by controlling critical timing of switching events is problematic in that a great deal of effort is needed to maintain optimal timing across load and temperature variations.

A straightforward method of limiting the effects of reverse recovery is to place a Schottky diode in parallel with the body diode as shown in Fig. 4. The Schottky diode has a very low reverse recovery charge Q_{rr} which practically eliminates the reverse recovery effects. For best results the Schottky diode should be rated to handle the full current load with the Schottky diode I-V characteristics chosen such that less than $1/100$ of the current flows through the body diode. Circuit efficiency improves, especially at lower frequencies, if care is taken to minimize the parasitic inductances L_{p1} and L_{p2} between the Schottky and body diode by optimizing the packaging and placement of the Schottky diode. If either of the parasitic inductances L_{p1} and L_{p2} between the body diode and the Schottky diode is not negligible, the efficacy of the Schottky will be reduced—if not negated.

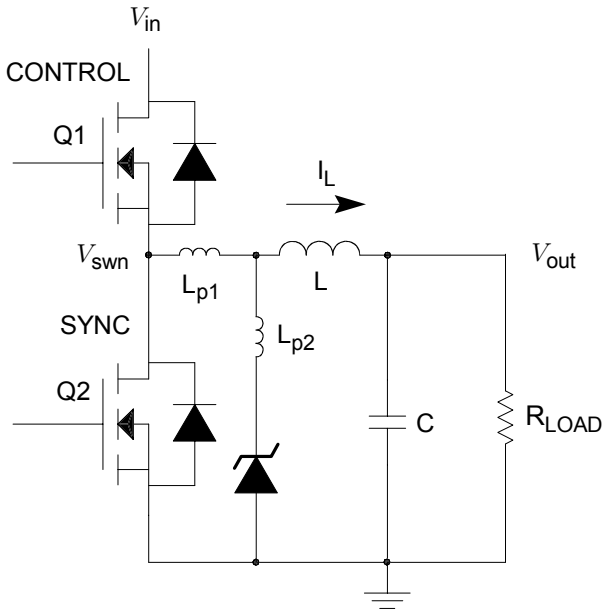

Figure 4. Mitigating effects of body diode reverse recovery by placing a Schottky diode in parallel with the PN body diode. Parasitic inductances L_{p1} and L_{p2} limit the effectiveness of the Schottky diode.

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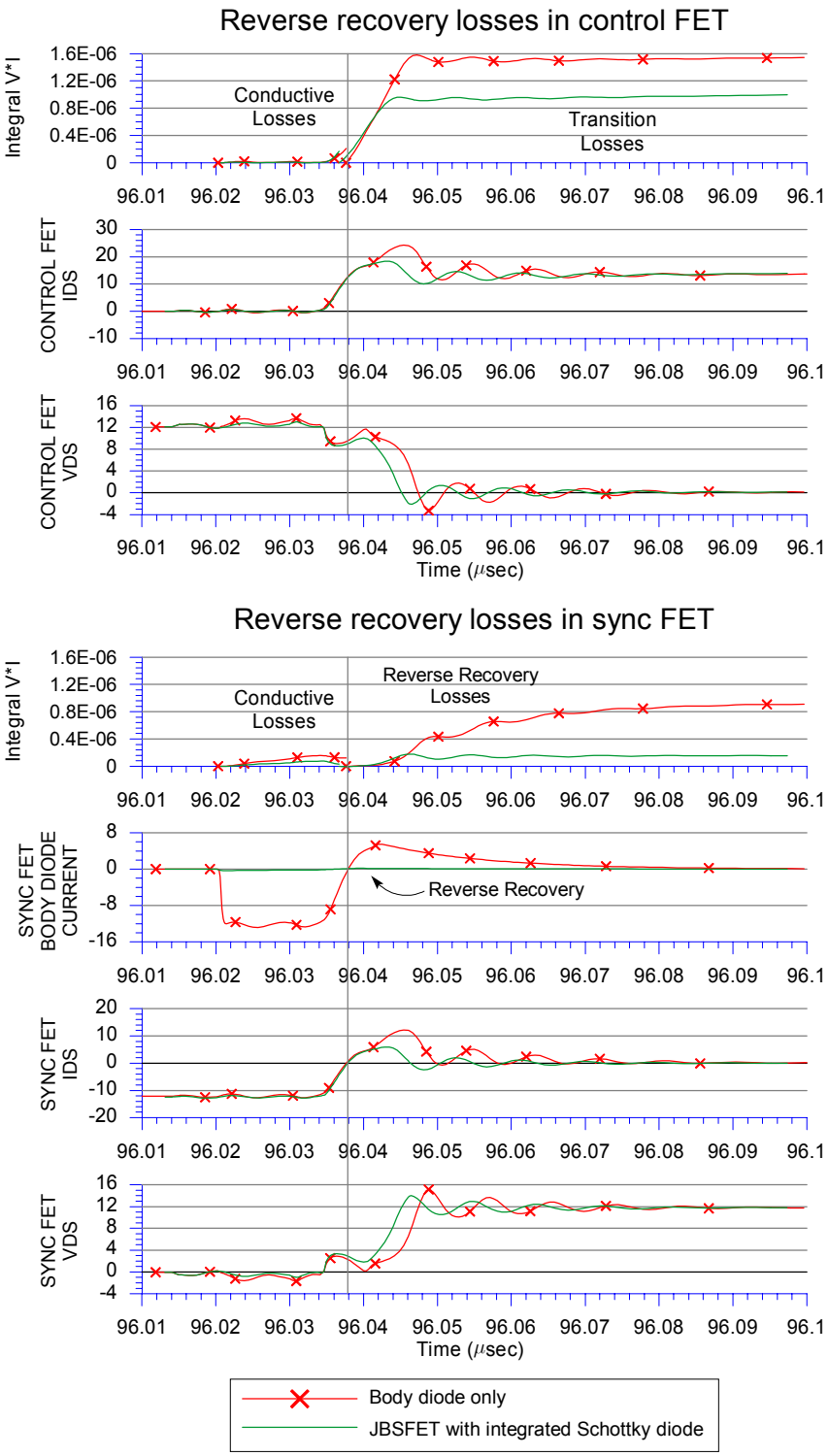

Figure 5. Timing diagram showing voltages, currents, and dissipated energy in the control and sync FETs for two cases: 1) body diode and 2) JBSFET with integrated Schottky diode.

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An ideal solution for the reverse recovery problem is to use a junction barrier Schottky FET (JBSFET) for the sync switch. The JBSFET has an integrated Schottky diode that clamps the body diode reverse recovery using a low leakage, low forward voltage Schottky structure interdigitated between the internal FET cell structure. A JBSFET is more than just a MOSFET plus Schottky diode. The structure of the JBSFET allows the Schottky to have the same current handling area of the switch FET without compromising the size of the FET or its RDSON value.

Simulation results showing the improvement in performance between a sync FET with body diode and a JBSFET with integrated Schottky diode is shown in Fig. 5. The reverse recovery of the body diode is clearly seen, as well as the dissipated energy in both the control and sync FET. The simulation results show a reduction in reverse recovery losses in the sync FET and a reduction in transition losses when using the JBSFET. Conduction losses, while lower with the JBSFET than the body diode case, are negligible compared with the significant reverse recovery losses. The JBSFET improves overall circuit efficiency by eliminating the effects of reverse recovery.

Measurements on a circuit with a JBSFET with integrated Schottky diode and a comparable trench FET device without a Schottky diode confirm that the elimination of

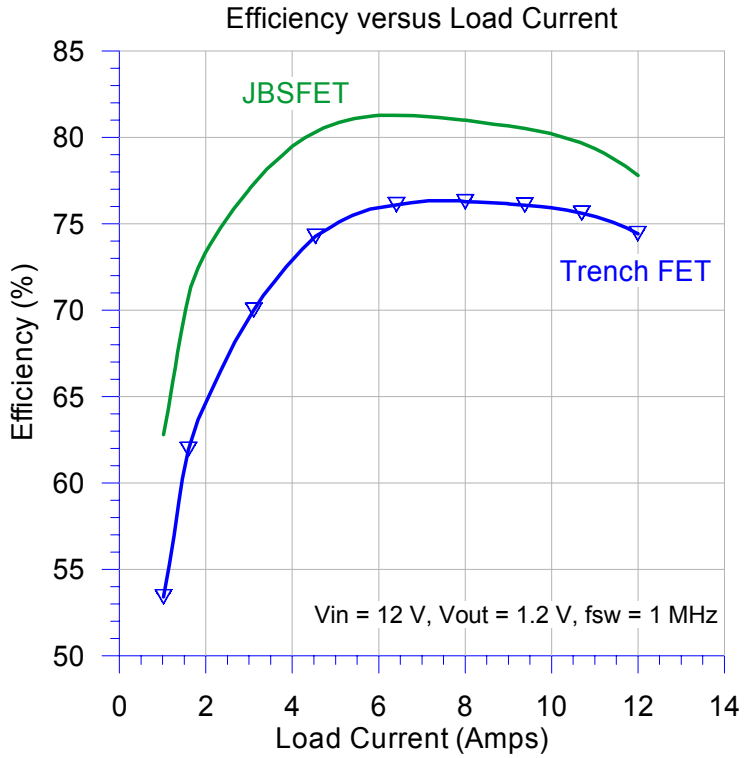

Figure 6. By eliminating reverse recovery the SSC JBSFET is able to realize a higher conversion efficiency than a competing device which has body diode reverse recovery losses.

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reverse recovery losses results in a higher overall efficiency for the JBSFET as shown in Fig. 6. While the JBSFET does have other performance enhancements in addition to the integrated Schottky, the significant improvement in efficiency is due in large part to the clamping of the body diode and elimination of reverse recovery.

Conclusion

The effect of body diode conduction and reverse recovery on sync buck efficiency has been discussed. Reverse recovery not only affects the sync FET, but it also increases power dissipation in the control FET. The use of a JBSFET with integrated Schottky will minimize the effects of reverse recovery and bring a substantial improvement in efficiency.

References

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[2] C. L. Ma and P. O. Lauritzen, "A simple power diode model with forward and reverse recovery," IEEE Transactions on Power Electronics, vol. 8, no. 4, pp. 342-6, Oct. 1993.

[3] P. Markowski, "Switching transition of the synchronous buck," ECN, p. 11, May 15, 2003.