Predictive Gate Drive™ Boosts Synchronous DC/DC Power Converter Efficiency

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ABSTRACT

Predictive Gate Drive™ is a novel digital control-driven technique that optimizes MOSFET turn-on and turn-off delays in synchronous rectifiers. It uses a closed loop feedback system to detect body-diode conduction, and continuously adjusts dead-time delays to minimize the conduction time interval. Depending upon operating frequency and output voltage, the Predictive Gate Drive™ control method can improve overall converter efficiency by two to four percent and the synchronous rectifier MOSFET power dissipation by 20 to 40 percent over currently available drive techniques. This paper compares this innovative new control technique to previous and currently existing related technologies. The problem of body-diode conduction is discussed and used to demonstrate efficiency improvements when the Predictive Gate Drive™ technology is applied.

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TABLES

FIGURES

1 Introduction

Most power converters requiring high-efficiency use high-speed synchronous rectifiers in the power stage. However, lower output voltages and higher operating frequencies require rethinking the control method for synchronous rectifiers.

In a buck converter, when the main switch turns off, current remains flowing to the load through the output inductor. Since this current cannot be interrupted immediately without using infinite voltage, a rectifier or catch device is used to freewheel the load current until the main switch turns on again. This device can be either a conventional diode, or an active controlled device, if a control signal is available to drive it. Traditionally, fixed delay or adaptive delay schemes are used to generate this signal in a synchronous buck design, assuring that cross conduction does not occur. However, as operating frequencies increase and output voltages drop, the efficiencies start to decrease drastically. In addition to switching losses, a large portion of the MOSFET losses are due to the body-diode conduction and reverse recovery losses. Finite delays associated with the adaptive and fixed schemes start to become a significant part of the switching cycle.

Predictive Gate Drive™ is a digital control-driven technique that optimizes MOSFET turn-on and turn-off delays in synchronous rectifiers. It uses a closed-loop feedback system to detect body-diode conduction, and adjusts dead-time delays to minimize the conduction time interval. It is a precision-controlled cross-conduction algorithm that virtually eliminates body-diode conduction and associated losses, while actively compensating for temperature variations, load-dependent delays, and different MOSFET loads. The lower junction temperature in the synchronous MOSFET translates to increased component reliability. Since the power dissipation is minimized, a higher switching frequency can also be used, allowing for smaller component sizes. The reduced power dissipation also allows users to design for increased output current capability or for a higher efficiency for given MOSFET size/cost.

Predictive Gate Drive™ minimizes the efficiency loss associated with lower output voltage and higher frequency designs. This paper compares efficiencies between today's prevailing adaptive delay technology (known in various forms as overlapping drive protection, adaptive shoot-through protection, anti-cross conduction) and the Predictive Gate Drive™ technology. Results show that the Predictive Gate Drive™ method improves overall converter efficiency by two to four percent and the MOSFET power dissipation by 20 to 40 percent over the adaptive scheme.

In order to gain an appreciation for the benefits of the Predictive Gate Drive™ control technique, an understanding of the body-diode conduction problem should first be introduced.

2 Synchronous Rectifiers and Body-Diode Conduction Loss

The synchronous buck power stage shown in Figure 1 uses a high-efficiency predictive synchronous buck driver to generate the gate drive signals for Q1 and Q2.

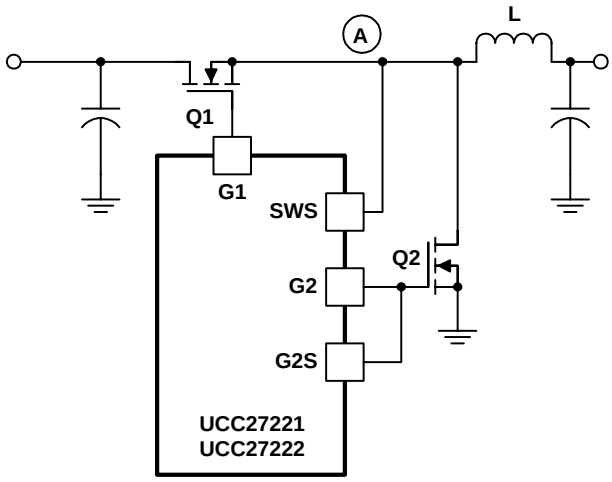

Figure 1. Synchronous Buck Power Stage

The point labeled “A”, shown in Figure 1, is commonly referred as the switch-node. Shown in Figure 2 and Figure 3 are the switch-node voltage waveforms from a typical synchronous buck application using Predictive Gate Drive™ control.

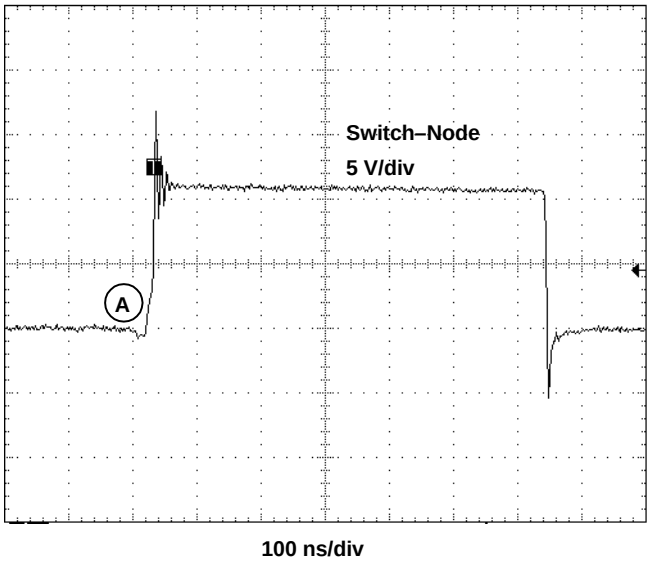

Figure 2. Switch-Node Voltage

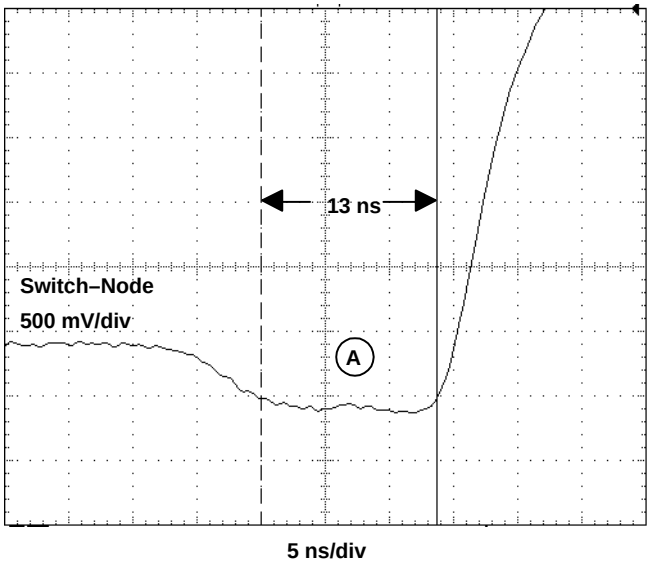

Figure 3. Close-Up: Switch Node A

Point A, shown in Figure 2 and Figure 3, is the time interval where neither the upper or lower MOSFET is conducting. During this brief time interval, the load current remains constant by flowing through the body-diode of the synchronous rectifier. A body-diode conduction time of 13 ns can be measured by zooming in on point A in a close up view as shown in Figure 2. For a synchronous buck converter not using Predictive Gate Drive™ technology, this time can be as long as 120 ns. Allowing the output current to flow through the body-diode of the synchronous rectifier has a degrading effect on overall efficiency. Predictive Gate Drive™ technology maximizes efficiency by reducing the delay time between turn-off of the high-side MOSFET and turn-on of the low-side MOSFET, in turn eliminating body-diode conduction time and minimizing reverse recovery loss. Minimizing this delay time to near zero keeps the load current flowing where it belongs, through the conducting MOSFET switches.

To fully appreciate the power savings offered by Predictive Gate Drive™, it is first necessary to understand how much power is dissipated in the synchronous rectifier body-diode. For the synchronous buck power stage shown in Figure 1, the power dissipated in the body-diode can be expressed as:

$$P_D = V_F \times I_{OUT} \times f_{SW} \times \left(t_{BD(rise)} + t_{BD(fall)}\right) \quad (1)$$

where:

- P_D = body-diode power dissipation
- V_F = synchronous rectifier body-diode forward voltage drop
- I_{OUT} = output current
- f_{SW} = switching frequency
- $t_{BD(rise)}$ = body-diode conduction time on switch-node rising edge
- $t_{BD(fall)}$ = body-diode conduction time on switch-node falling edge

If the assumption is made that the body-diode conduction time is the same on the rising and falling edges of the switch node, equation (1) can be simplified and rewritten as:

$$P_D = V_F \times I_{OUT} \times f_{SW} \times 2 \times t_{BD} \quad (2)$$

To further put the body-diode loss in perspective, Equation 2 needs to be expressed as a percent of total output power, P_{OUT}. Dividing both sides of Equation 2 by P_{OUT} and simplifying gives:

$$\frac{P_D}{P_{OUT}} \cong \frac{V_F}{V_{OUT}} \times f_{SW} \times 2 \times t_{BD} \quad (3)$$

For a constant body-diode conduction time, t_{BD}, and forward voltage drop, V_F, a relationship between the power loss due to body-diode conduction as a percent of total output power is shown graphically in Figure 4. For low-output voltage, high-frequency power stages, the additional loss due to body-diode conduction can be as high as 6% overall. When the body-diode conduction time is not fixed, but rather increases such as in response to varying line and load conditions or component tolerances differences, this loss may even exceed 6% for certain applications. However, from Figure 4, it can clearly be shown that the greatest potential efficiency savings is realized in low output voltage high frequency power applications.

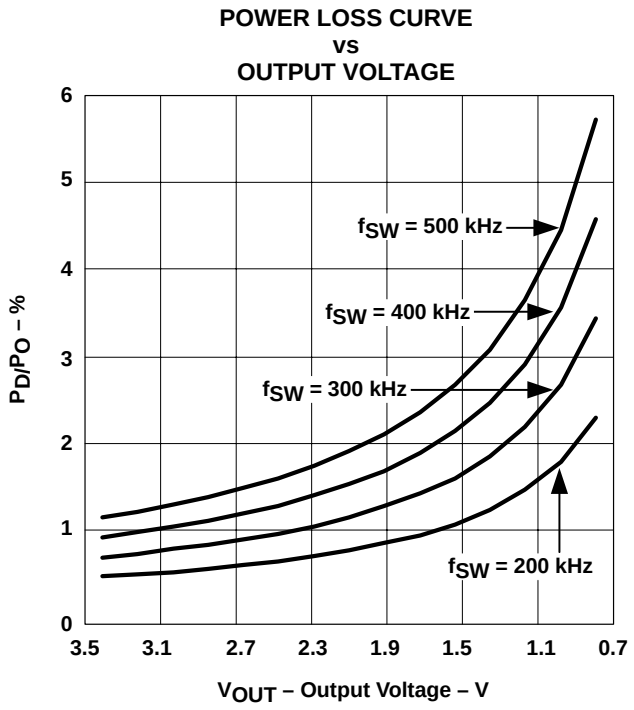

Figure 4.

Figure 5 shows a typical switch-node voltage waveform for any synchronous rectified buck converter. Illustrated are the relative effects of a fixed-delay drive scheme (constant, pre-set delays for the turn-off to turn-on intervals), an adaptive delay drive scheme (variable delays based upon voltages sensed on the current switching cycle) and the predictive delay drive scheme.

The period shown in Figure 5 as channel conduction is the time that the load current is flowing through the synchronous rectifier. During this interval, the synchronous rectifier is subject to conduction loss due to the product of the output current and the drain-to-source on-resistance. Note that the longer the time spent in diode conduction and hence the less time spent in channel conduction, the lower the efficiency.

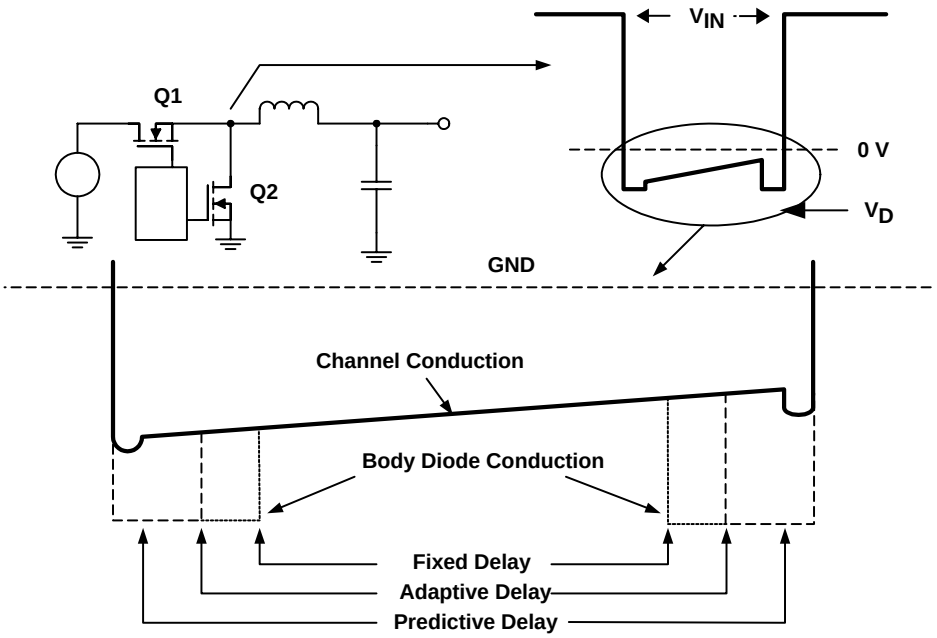

Figure 5. Switch Node Waveform for Synchronous Buck Converter

To numerically show the effect of output voltage on synchronous rectifier efficiency gain, both the channel conduction as well as body-diode conduction intervals must be considered. Assume:

- Q1 = OFF, Q2 = ON
- V_F = 1 V (body-diode forward voltage drop)
- V_{DS} = 0.1 V (MOSFET drain-to-source channel voltage)

Therefore the efficiency within the synchronous rectifier during the channel conduction interval is:

$$\eta_{CH} = \frac{V_{OUT}}{V_{OUT} + V_{DS}} \tag{4}$$

And likewise, the synchronous rectifier efficiency during the body-diode conduction interval is

$$\eta_{BD} = \frac{V_{OUT}}{V_{OUT} + V_F} \tag{5}$$

Taking several commonly used output voltages as an example, the following synchronous rectifier efficiencies are compared in Table 1.

Table 1. Efficiency Comparison

EFFICIENCY	V_O – OUTPUT VOLTAGE			
	5 V	3.3 V	1.8 V	0.9 V
During channel conduction (η_{CH})	$\frac{5}{5.1}$ = 98%	$\frac{3.3}{3.4}$ = 97%	$\frac{1.8}{1.9}$ = 95%	$\frac{0.9}{1.0}$ = 90%
During body-diode conduction (η_{BD})	$\frac{5}{6}$ = 83%	$\frac{3.3}{4.3}$ = 77%	$\frac{1.8}{2.8}$ = 64%	$\frac{0.9}{1.9}$ = 47%

As shown in Table 1, the voltage drop associated with the synchronous rectifier body-diode becomes a greater percentage of the total synchronous rectifier power loss at lower output voltages. In many instances, the second highest power loss in the design is caused by the lower, commutating MOSFET body-diode conduction after the switch is turned off. Until recently, there have been two dominant gate drive technologies to help reduce this loss; a fixed delay technology and an adaptive delay method. In principle, they should both work reasonably well, however that's rarely the case due to temperature variations and lot-to-lot manufacturing tolerance issues.

To understand the Predictive Gate Drive™ technology, previous and current technologies used to minimize cross-conduction in synchronous rectifiers must first be considered.

3 Previous and Current Technologies

3.1 First Generation – Fixed Delay

The first synchronous rectifier controllers had a fixed turn-on delay between the two gate drivers. The advantage of this well-known technique, shown in Figure 6, is its simplicity. The drawbacks include the need to make the delay times long enough to cover the entire application of the device and the temperature along with lot-to-lot variation of the time delay. Adding enough fixed delay dead time in order to avoid cross-conduction, results in a very non-optimal design. Since the body-diode of the synchronous rectifier conducts during this dead time, the efficiency of this technique varies with different MOSFETs, ambient temperature, and with the lot-to-lot variation of the dead time delay.

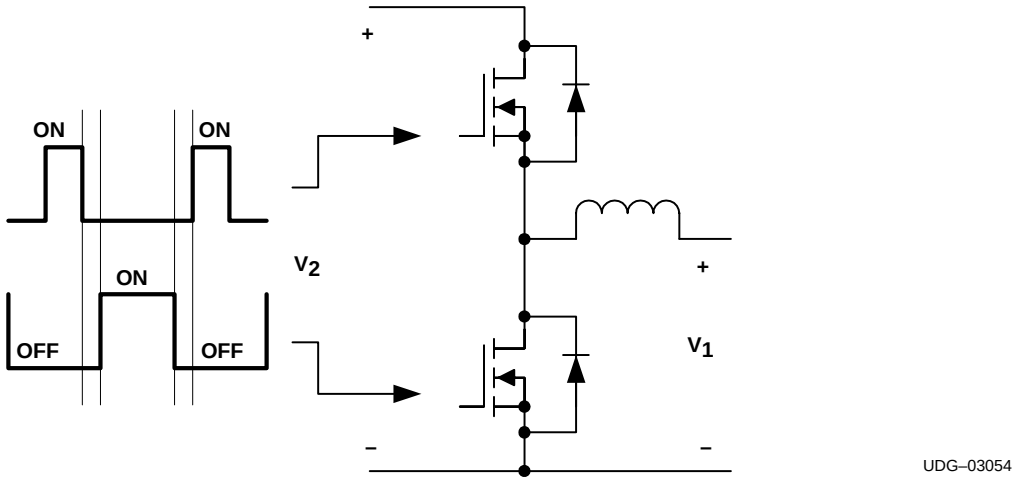

Figure 6. Fixed-Delay Gate Drive Technique

3.2 Second Generation – Adaptive Delay

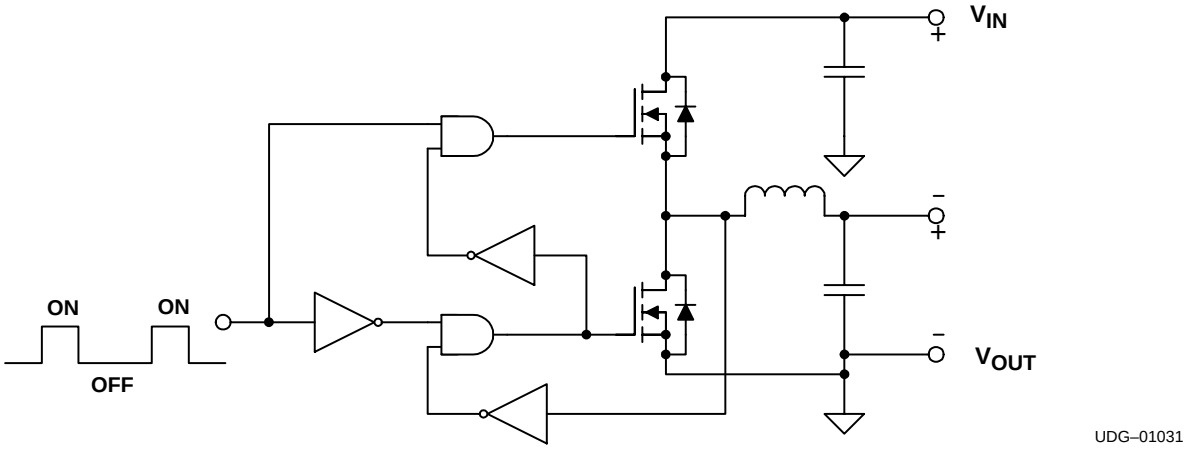

Figure 7. Adaptive Gate Drive Technique

The main advantage of the adaptive technique is the on-the-fly delay adjustment for different MOSFET's and temperature-variable time delays. The disadvantages include the body-diode conduction time intervals caused by delays in the cross-coupling loops and the inability to compensate for the delay to charge the MOSFET gates to the threshold levels. Additionally, it is difficult to determine whether the synchronous MOSFET channel is off by solely monitoring the switch-node voltage. Some devices actually add a programmable fixed delay between the turn-off of the synchronous rectifier and the turn-on of the main MOSFET via an external capacitor. This added delay directly affects the power stage efficiency through additional body-diode conduction losses. Since these losses are centralized in the synchronous MOSFET, the stress and temperature rise in this component becomes a major design headache.

The adaptive delay control technique has very definite advantages over the fixed delay method. However, it is clear that a better control technique is needed for future low output voltage converters. What if a feedback system were used to detect body-diode conduction, and actively adjust dead time delays to minimize it? Controlling the synchronous rectifier in this fashion would result in several key benefits, such as:

- Could virtually eliminate body-diode conduction.
- By eliminating body-diode conduction, reverse recovery losses would also be significantly reduced.
- System would adjust for different MOSFETs, temperature and load dependent delays.
- The body-diode efficiency losses shown in Table 1 could be recovered, resulting in overall efficiency increase of up to 4%.

3.3 Third Generation – Predictive Delay

The third-generation predictive control technique is different from the adaptive technique in that it uses information from the previous switching cycle to set the dead time for the current cycle. The adaptive technique on the other hand uses the current state information to set the delay times. The feedback loop propagation delays associated with the adaptive technique unavoidably results in some inherent body-diode conduction.

Referring to the synchronous buck power stage shown in Figure 1, the smaller the delay time between Q2 turn-off and Q1 turn-on and visa versa, the less time that the body-diode of Q2 conducts. Ideally, if the delay time were zero, there theoretically would be zero body-diode conduction. Rather than sense the switch-node voltage for body-diode conduction and then adjust the delay time accordingly, Predictive Gate Drive™ uses information from the previous switching cycle to *predict* the minimum delay time for the current cycle. This predictive concept is illustrated in Figure 8.

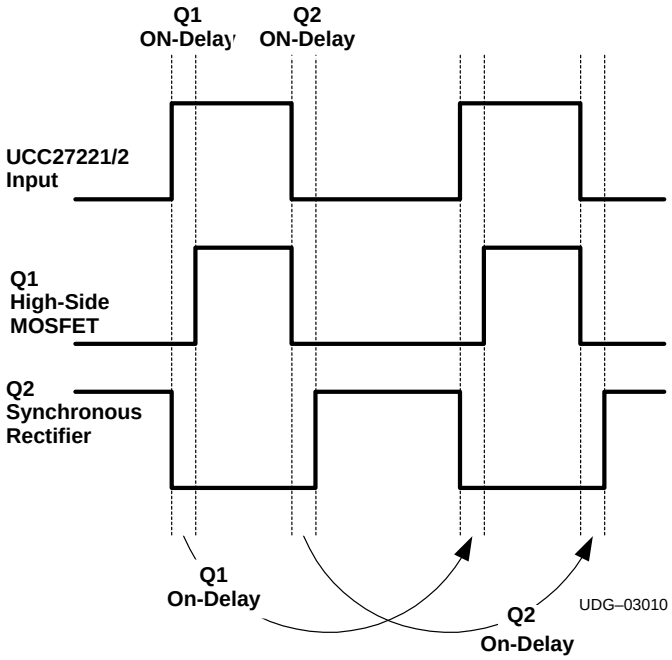

Figure 8. Predictive Gate Drive™ "Predictive" Timing

Predictive Gate Drive™ works on the premise that the delay time required for the next switching cycle will be close to what was required for the previous cycle. When this assumption does not hold true, as in the case during a sudden line or load transient, Predictive Gate Drive™ operation requires some time to adjust to the changing operating conditions. During the time Predictive Gate Drive™ is recalibrating, there may be a very brief period of body-diode conduction in Q2, but this does not affect steady state efficiency or performance.

During the time that the PWM input signal transitions from high to low, a NOR gate senses the drain-to-source and gate-to-source voltage of Q2. If the NOR gate output is HIGH, as shown in Figure 9, the delay is reduced by one bit of an N-bit buffer delay line. For the UCC27221/2, each delay bit in the 16-bit delay line represents a shift of approximately 4 ns. The delay is reduced by 4 ns intervals every switch cycle until the output of the NOR gate is low, as shown in Figure 10. When the NOR gate output is low, the delay advances forward one delay unit on the next switching cycle. The process of continually shifting the delay forward and backward each cycle is known as *dithering*. When Predictive Gate Drive™ is optimal, dithering should occur within an 8-ns (2-delay bits) window.

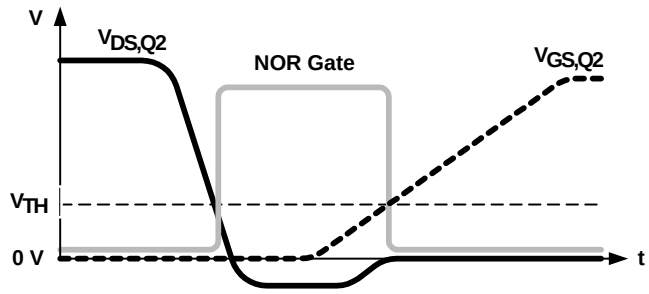

Figure 9. Non–Optimal Delay (NOR is HIGH)

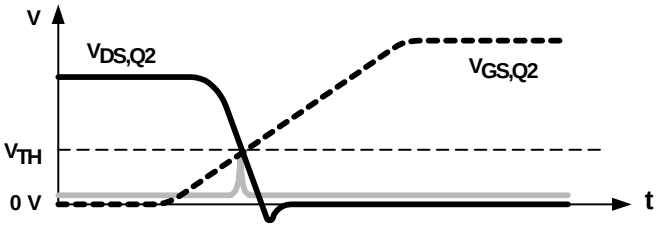

Figure 10. Optimal Delay (NOR is LOW)

Conversely, during the time the PWM input signal transitions from low to high, a comparator senses the drain-to-source and gate-to-source voltage of Q2. If body-diode conduction in Q2 is detected, the comparator output is HIGH, as shown in Figure 11, and the delay time is once again reduced by one delay bit. Once enough delay segments have been introduced, such that the comparator output remains LOW, body-diode conduction in Q2 is now virtually zero, as shown in Figure 12. From the optimal delay positioning of Figure 12, the delay time increases by one delay bit on the next successive switch cycle. Dithering within 8 ns of this optimal delay then becomes apparent.

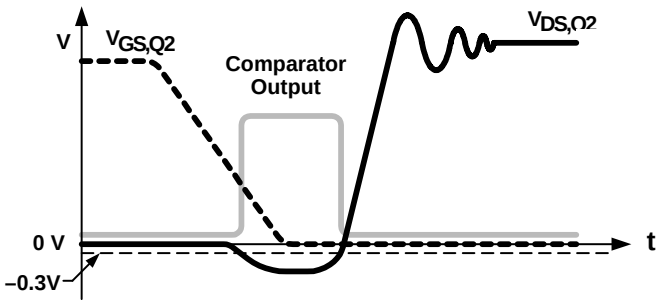

Figure 11. Body-Diode Conduction

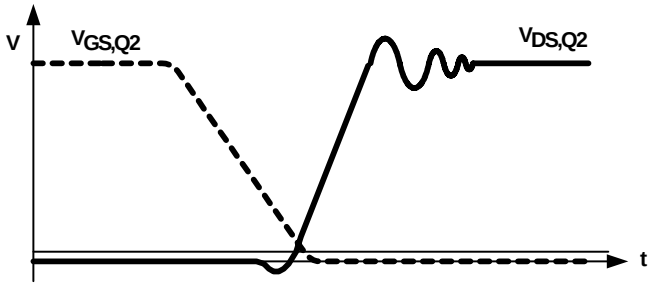

Figure 12. Optimal Delay

All of the shortcomings mentioned with first and second-generation control techniques are overcome using Predictive Gate Drive™ control. Using the Predictive Gate Drive™ technique, the idea of switching right at the cross-conduction boundary becomes quite feasible. Because the synchronous rectifier body-diode is not conducting, the P-N junction never becomes fully saturated, making the reverse recovery process much easier

4 Predictive Gate Drive Control Techniques

By utilizing a digital control feedback system to detect body-diode conduction, Predictive Gate Drive™ technology produces the precise timing signals necessary to operate near the threshold of cross-conduction. The Predictive Gate Drive™ control loops are stabilized internally and are therefore transparent to the user. These loops use no external components, so no additional design is needed to take advantage of the higher efficiency of these drivers

Two internal feedback loops in the predictive delay controller continuously adjusts the turn on delays for the two MOSFET gate drives G1 and G2. As shown in Figure 13, t_{ON},G1 and t_{ON},G2 are varied to provide minimum body-diode conduction in the synchronous rectifier MOSFET Q2. The turn-off delay for both G1 and G2, t_{OFF},G1 and t_{OFF},G2 are fixed by propagation delays internal to the device.

Since the predictive delay controller is implemented using a digital control technique, the time delays are therefore discrete. As mentioned previously, the turn-on delays, t_{ON},G1 and t_{ON},G2, are changed by a single step (typically 4 ns) every switching cycle.

For the UCC27222, the minimum and maximum turn-on delays for G1 and G2 are specified in the electrical characteristics table of the data sheet.

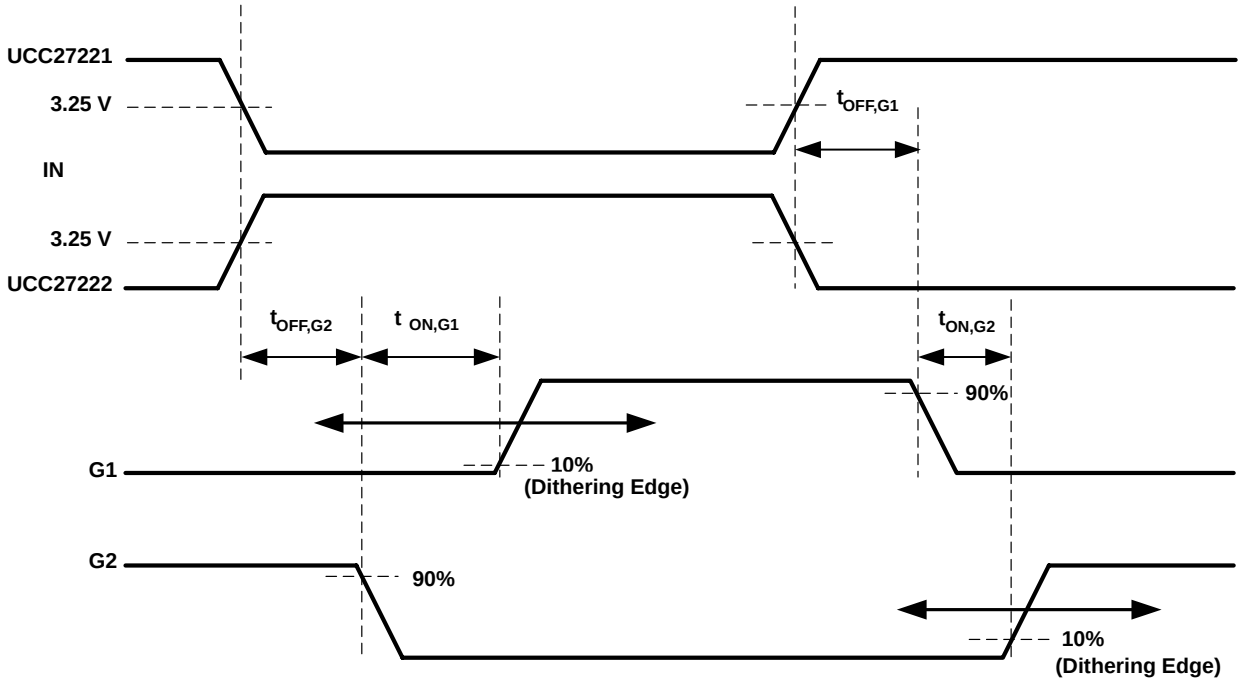

Figure 13. Predictive Gate Drive™ Timing Diagram

4.1 Predictive Gate Drive Benefits to the High-Side MOSFET

In addition to minimizing body-diode and reverse recovery losses in the synchronous rectifier, Predictive Gate Drive™ control reduces power dissipation on the main (forward) MOSFET as well, although the savings is not as significant as that in the synchronous rectifier MOSFET.

The reason is: during reverse recovery the body-diode is still forward biased, thus the reverse recovery current goes through the forward MOSFET while the drain-source voltage is still high, causing additional switching losses. During this transition, the switching losses in the high-side MOSFET are defined by the drain-to-source voltage and current as $V_{DS}=V_{IN}$ and $I_{DS}=I_{LOAD}+I_{RR}$, without Predictive Gate Drive™. When Predictive Gate Drive™ is utilized, these same loss parameters are now defined by $V_{DS}=V_{IN}$ and $I_{DS}=I_{LOAD}$. The reduction in drain-to-source current explains the power savings in the high-side MOSFET. This can further be supported by comparing the thermal image shown in Figure 22, with Predictive Gate Drive™, to the image of Figure 21, without Predictive Gate Drive™.

5 Performance Comparison Between Adaptive Control and Predictive Gate Drive Techniques

5.1 Adaptive vs. Predictive Waveforms

Figures 14 through16 illustrate the adaptive (left) vs. predictive (right) switching waveforms. Key comparison regions are denoted with (A), (B), (C), (D), and (E) for the adaptive control waveforms and (A′), (B′), (C′), (D′), and (E′) for the predictive control waveforms. Figures 15 and16 are close-ups of each transition edge.

At (A), the propagation delay from sensing the synchronous rectifier gate going low to the high-side gate going high results in approximately 60 ns of body-diode conduction shown at (B). With the predictive drive, as soon as the body-diode conduction of the synchronous rectifier MOSFET (B) is sensed, the high-side turn-on delay is adjusted to minimize the body-diode conduction time (B′).

At (A′), the high side gate-to-source voltage is increasing while the synchronous rectifier gate-to-source voltage is decreasing. A natural result of the precise timing of the high-side MOSFET turn-on is shown at (C) and (C′). The overshoot and ringing for the predictive drive (C′) has a much smaller amplitude than the adaptive drive (C) due a reduction in reverse recovery in the synchronous rectifier MOSFET body-diode. This reduction in reverse recovery is only possible with the extremely precise gate timing used in the predictive drive technique.

At (D), the propagation delay from the synchronous rectifier drain-to-source voltage falling to the gate-to-source voltage rising causes the body-diode of the synchronous rectifier MOSFET to conduct for approximately 60 ns (E). When the predictive drive is enabled (D′), the inherent delay is eliminated and virtually no body-diode conduction is shown at (E′).

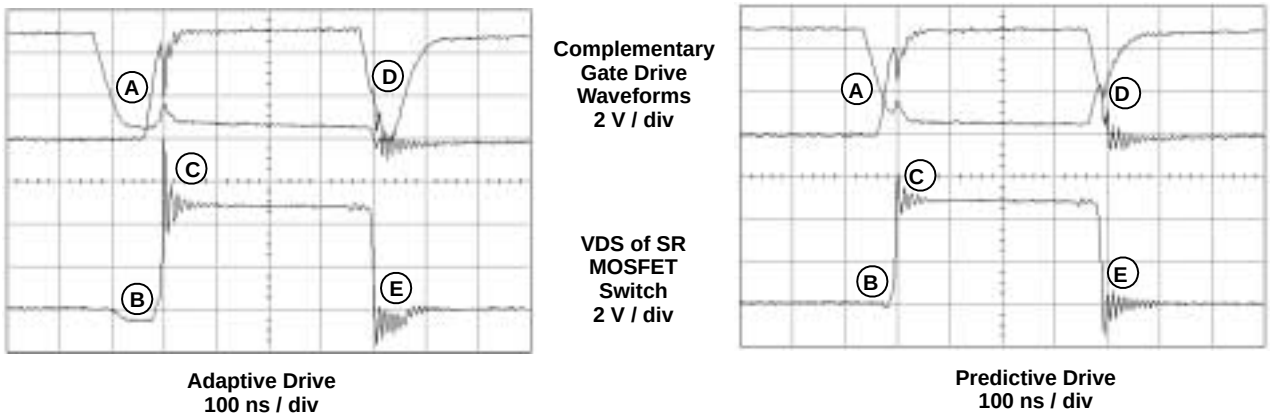

Figure 14. Adaptive vs. Predictive Switching Waveforms

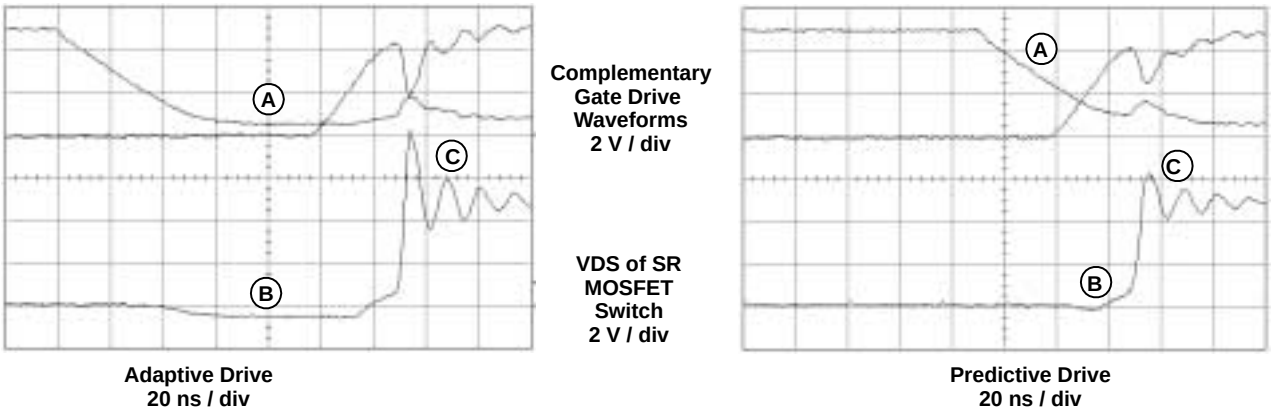

Figure 15. Close-Up: Turn-Off of Synchronous Rectifier Switch to Turn-On of Main Switch

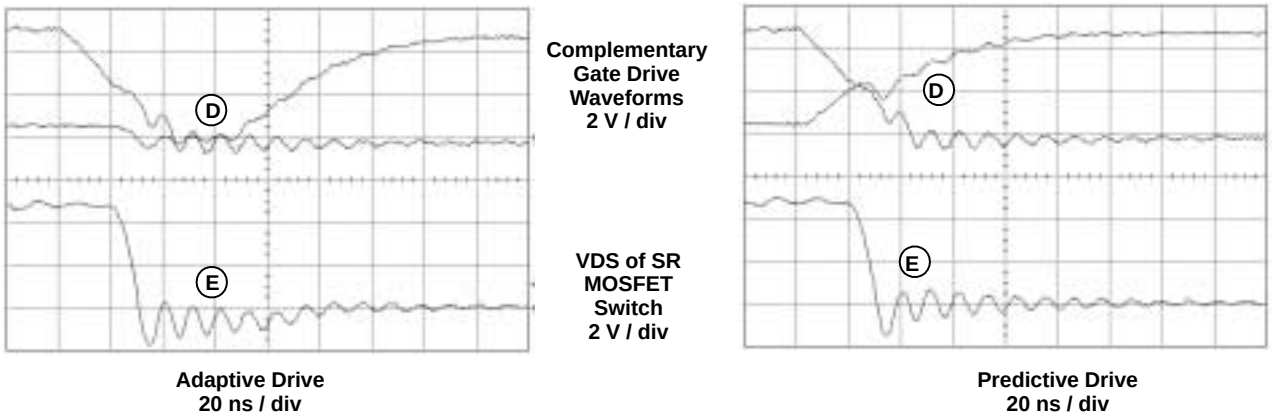

Figure 16. Close-Up: Turn-Off of Main Switch to Turn-On of Synchronous Rectifier Switch

5.2 Efficiency Comparison

Figures 17 through 20 show a series of efficiency measurements taken at two different output voltages (0.9 V and 1.8 V) and two different switching frequencies (250 kHz and 500 kHz) for both predictive and adaptive delay techniques. The efficiency gain using the predictive technique is 1% for a V_{OUT} level of 1.8 V and at a switching frequency of 250 kHz. Figure 18 and Figure 19 show the efficiency gain approximately doubles when V_{OUT} is lowered by a factor of two (to 0.9 V), or when the switching frequency is doubled to 500 kHz. With doubled frequency and one-half of the output voltage, the efficiency gain of predictive technology is about 4% over the adaptive technology (see Figure 20). Therefore, as the switching frequency increases and output voltages are lowered, the efficiency gains are higher, as supported by equation (3). This results in lower operational temperatures for increased reliability as well as smaller size designs for increased frequencies.

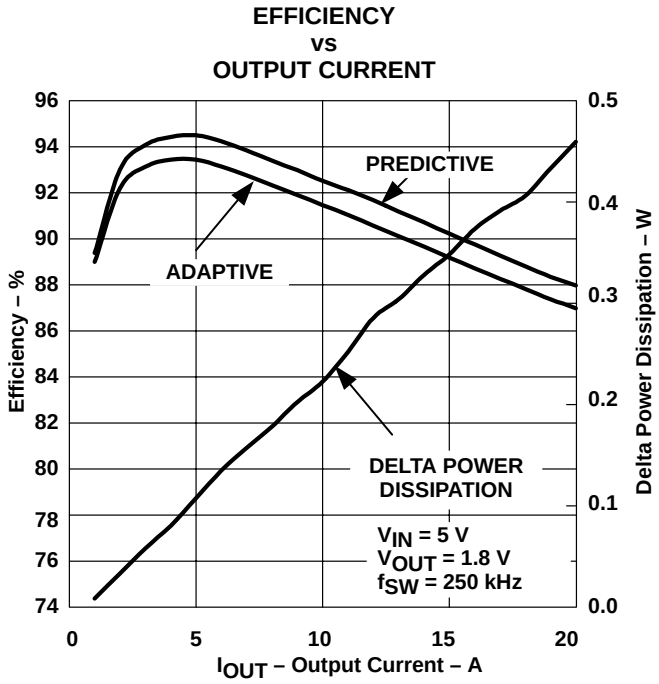

Figure 17.

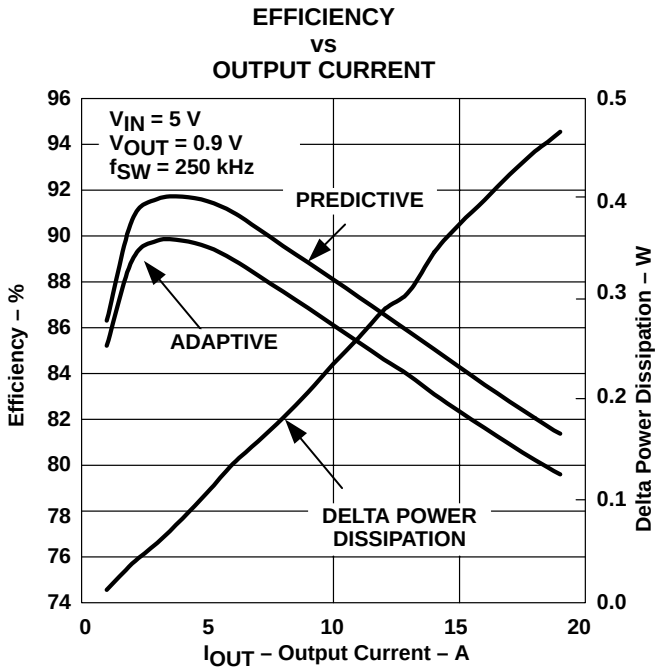

Figure 18.

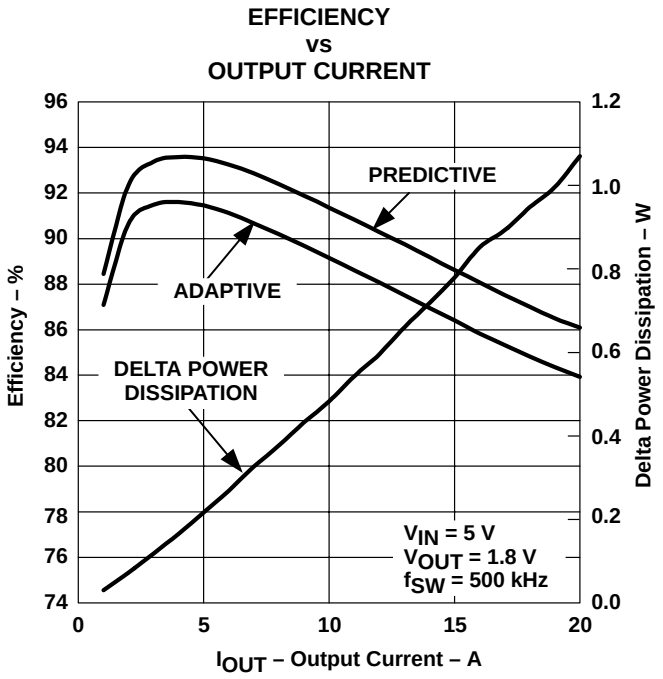

Figure 19.

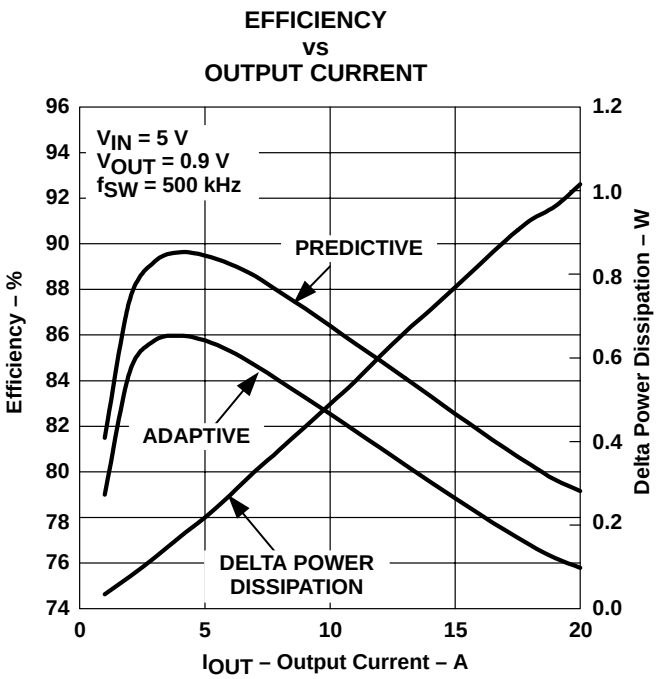

Figure 20.

5.3 Thermal Comparison

Both images shown in Figure 21 and Figure 22 were taken from identical synchronous buck power stages, operating at 500 kHz, from a 5-V input, with a 0.9-V output and a 20-A load. The converter also uses two Hitachi LF PAK MOSFET's in parallel for both the main MOSFET's and synchronous rectifiers.

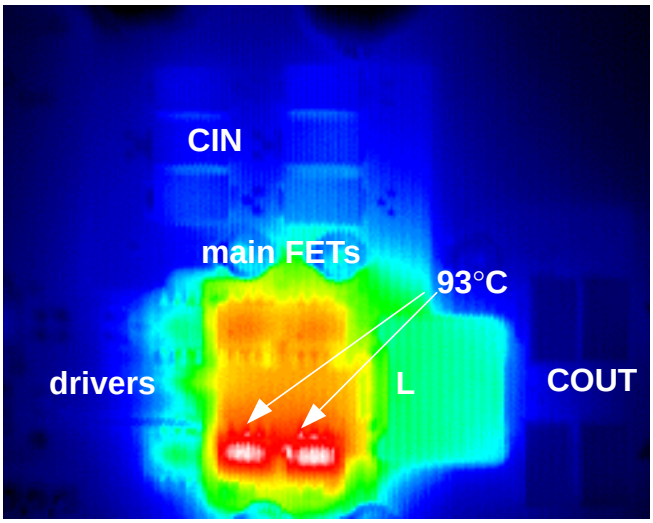

Figure 21. Adaptive Delay Control

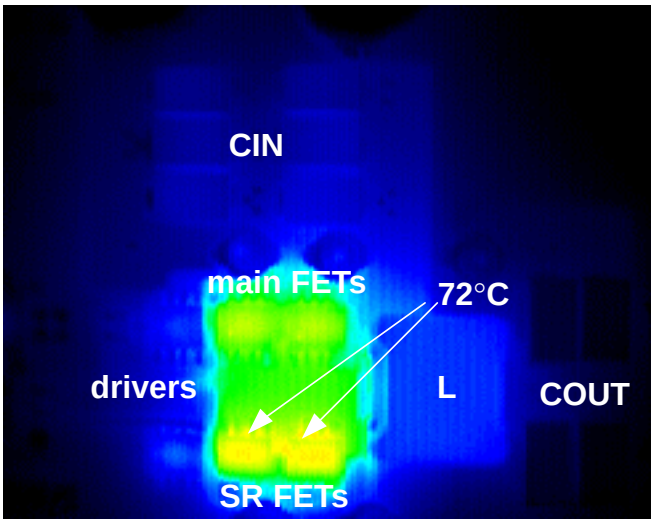

Figure 22. Predictive Gate Drive™ Technology

NOTE: White = 93°C, Yellow = 72°C, both images are scaled to the same unit measures. Approximately 21°C change in temperature rise in synchronous rectifier MOSFETs.

Comparing the Predictive Gate Drive™ control to the adaptive delay control, it can be seen that the power stage using Predictive Gate Drive™ operates approximately 21°C cooler than the same power stage controlled by adaptive delay. This represents a 22.5% reduction in thermal dissipation just in the synchronous rectifier switches. To the power supply designer, this increase in thermal efficiency translates to lower junction temperatures resulting in increased component reliability, lower failure rates and higher mean time between failure (MTBF). For both power stages operating at similar temperatures, the thermal efficiency gains of a converter using Predictive Gate Drive™ can also be realized in the form of higher output current capability and/or higher operating frequency meaning smaller power stage components.

6 Limitations of Predictive Gate Drive™

As shown in Figures 23 and 24, the benefits of Predictive Gate Drive™ technology become more significant at higher operating frequency and lower output voltage. Conversely, the benefits of the Predictive Gate Drive™ are minimal below 100 kHz of operating frequency and above 5-V output voltage. The reasons for both can be seen in equation (3), repeated here.

$$\frac{P_D}{P_{OUT}} \cong \frac{V_F}{V_{OUT}} \times f_{SW} \times 2 \times t_{BD} \quad (6)$$

Solving equation (3) for V_{OUT}:

$$V_{OUT} = \frac{P_{OUT}}{P_D} \times V_F \times f_{SW} \times 2 \times t_{BD} \quad (7)$$

And assuming a body-diode forward voltage drop of 0.8 V, with a total body-diode conduction time of 120 ns (2 x 60 ns), the following graphs are generated highlighting the output voltage and frequency limitations of Predictive Gate Drive™ technology.

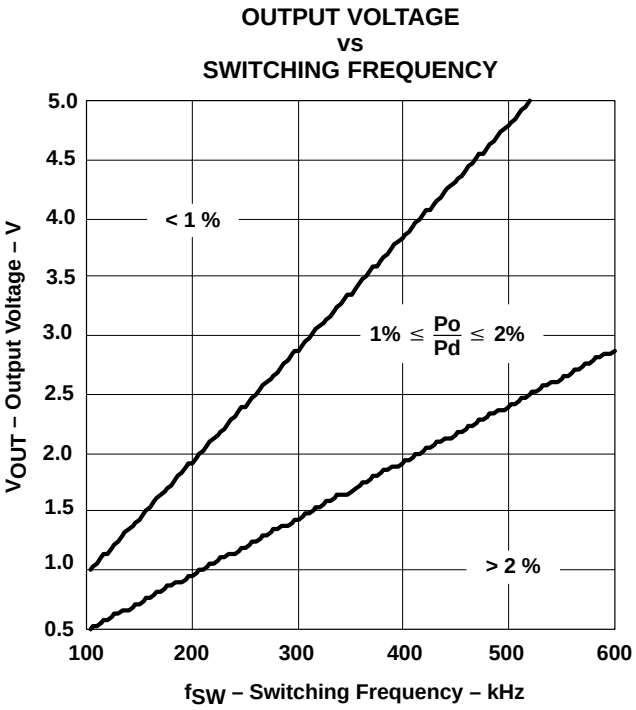

Figure 23. Frequency Voltage Limitations 1% to 2%

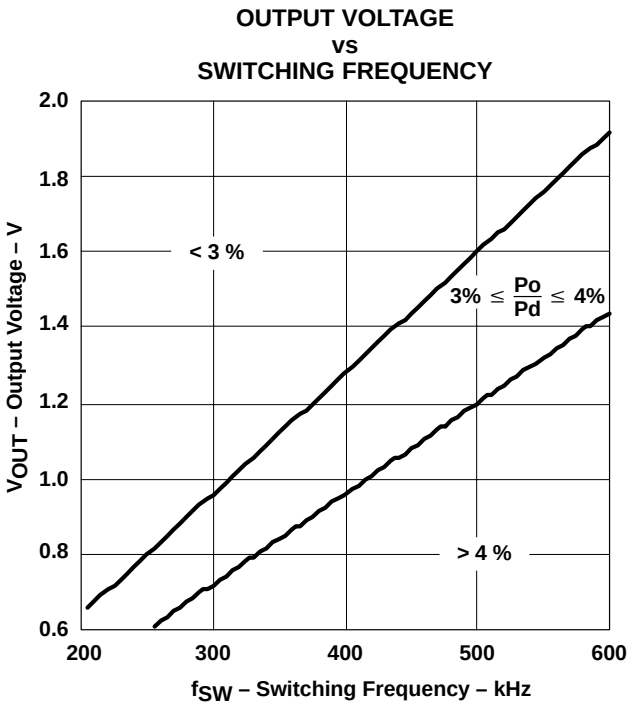

Figure 24. Frequency Voltage Limitations 2% to 4%

Figures 23 and 24 are helpful in understanding of how much benefit can be gained by using the Predictive Gate Drive™ technique. As can be seen from Figure 23, the benefit of Predictive Gate Drive™ becomes less than 1% at frequencies below 100 KHz. In terms of efficiency benefit only, an overall gain of less than 1% should be considered impractical from a Predictive Gate Drive™ point of view. Figure 24 shows the highest practical efficiency benefits. For instance a design with a 1-V output, switching at 500 KHz, should expect a 4% efficiency increase over a similar design using adaptive delay control. This can further be validated by referring back to Figure 20 which, based upon experimental measurements, shows a comparision of the overall efficiencies between the two control techniques operating at these specifications.

Another factor related to the amount of benefit derived from Predictive Gate Drive™ is the total amount of body-diode conduction time measured using any competitive technology. The measured data for adaptive delay control shown in Figure 14 produced total body-diode conduction times between 100 ns and 150 ns. As a result, 120 ns was entered into equation (7) to generate graphs shown in Figure 23 and 24. For higher total body-diode conduction times, the benefit of Predictive Gate Drive™ can be greater than that shown by those limits.

7 Reaping the Benefits of Predictive Gate Drive

The additional efficiency savings in the synchronous rectifier gained from Predictive Gate Drive™ can be used in several ways. Compared to a design using adaptive delay control, the efficiency savings from Predictive Gate Drive™ may come in the form of reduced operating temperatures translating to lower MTBF, increased output current for similar operating temperatures or higher operating frequency translating to smaller power stage components.

Within the synchronous rectifier, the power losses are comprised of three components: conduction loss, body-diode loss and reverse recovery loss. Because the synchronous rectifier turns on at zero voltage there are no switching losses associated with the simultaneous overlap of drain-to-source voltage and drain current. There are however associated gate charge losses, but because of higher internal impedance most of these are assumed to be in the driver and not the synchronous rectifier. That being the case, the three losses can be approximated by:

7.1 Conduction Loss

$$P_{COND} = \left(I_{OUT}\right)^2 \times R_{DS(on)} \times (1 - D) \tag{8}$$

7.2 Body-Diode Loss [Equation (2) Rewritten]

$$P_D = V_F \times I_{OUT} \times f_{SW} \times 2 \times t_{BD} \tag{9}$$

7.3 Reverse Recovery Loss

$$P_{RR} = \frac{1}{2} \times Q_{RR} \times V_{IN} \times f_{SW} \tag{10}$$

7.4 Total Synchronous Rectifier Loss

$$P_{SR} = P_{COND} + P_D + P_{RR} \tag{11}$$

Additionally, the power dissipation capability of a MOSFET is limited by the maximum allowable junction temperature for a given device, as specified in the manufacturers data sheet.

$$T_J = \left(P_{SR} \times \theta_{JA}\right) + T_A \tag{12}$$

8 Design Example

- Input Voltage: 12 V
- Output Voltage: 1.8 V
- Output Current: 10 A
- Switching Frequency: 300 KHz
- Operating Temperature: –40°C < T_A < 85°C

8.1 Siliconix Si7880DP Manufacturers Specifications

- Single Synchronous rectifier MOSFET device
- On-Resistance: 3 mΩ
- Reverse recovery charge: 130 nC
- Junction-to-ambient thermal resistance: 50°C/W
- Maximum junction temperature: 150°C

8.2 CASE 1 – Adaptive Delay Control

From equation (8), conduction loss in the synchronous rectifier is given as:

$$P_{COND(ADC)} = (10\ A)^2 \times \left(3 \times 10^{-3}\Omega\right) \times \left(1 - \frac{1.8\ V}{12V}\right) = 0.255\ W \quad (13)$$

Assuming the forward voltage drop of the body-diode is 0.8 V and is conducting for a total time of 120 ns (2 x 60 ns), the loss due to body-diode conduction is given by equation (2) as.

$$P_{D(ADC)} = 0.8\ V \times 10\ A \times \left(300 \times 10^3\ Hz\right) \times 2 \times \left(60 \times 10^{-9}\ s\right) = 0.288\ W \quad (14)$$

And the reverse recovery loss is calculated from equation (10) as:

$$P_{RR(ADC)} = \frac{1}{2} \times \left(130 \times 10^{-9}\ C\right) \times 12\ V \times \left(300 \times 10^3\ Hz\right) = 0.234\ W \quad (15)$$

Summing each of these results, the total power loss in a synchronous rectifier using adaptive delay control can be as high as:

$$P_{SR(ADC)} = 0.255\ W + 0.288\ W + 0.234\ W = 0.777\ W \quad (16)$$

With a total power loss in the synchronous rectifier of 0.777 W, and operating at a maximum ambient temperature of 85°C, the maximum operating junction temperature can be calculated from equation (12).

$$T_{J(ADC)} = 0.777\ W \times 50^{o}C/W + 85^{o}C = 123.85^{o}C \quad (17)$$

Or a 38.85°C rise in junction temperature contributed from power dissipation in the synchronous rectifier.

8.3 CASE 2 – Predictive Gate Drive™ Control Technique

Using the Predictive Gate Drive™ control technique, the conduction loss in the synchronous rectifier is the same as the adaptive delay case.

$$P_{COND(PGD)} = (10\ A)^2 \times \left(3 \times 10^{-3}\Omega\right) \times \left(1 - \frac{1.8\ V}{12V}\right) = 0.255\ W \quad (18)$$

And for these operating conditions, the body-diode conduction time has been measured to be approximately 20 ns total, giving a loss due to body-diode conduction of.

$$P_{D(PGD)} = 0.8\ V \times 10\ A \times \left(300 \times 10^{3}\ Hz\right) \times 2 \times \left(10 \times 10^{-9}\ s\right) = 0.048\ W \quad (19)$$

Using Predictive Gate Drive™, the body-diode never fully conducts. As a result, the loss associated with reverse recovery is reduced by as much as 50%. Reducing equation (11) by 50% gives an approximate value for the reverse recovery loss in the synchronous rectifier.

$$P_{RR(PGD)} = \frac{1}{2} \times \frac{1}{2} \times \left(130 \times 10^{-9}\ C\right) \times 12\ V \times \left(300 \times 10^{3}\ Hz\right) = 0.117\ W \quad (20)$$

Summing each of these results, the total power loss in a synchronous rectifier using Predictive Gate Drive™ can be given as:

$$P_{SR(PGD)} = 0.255\ W + 0.048\ W + 0.117\ W = 0.42\ W \quad (21)$$

Compared to Case 1, this represents a total power savings of 46% within the synchronous rectifier. With a total device loss in the synchronous rectifier of 0.42 W, and operating at a maximum ambient temperature of 85°C, the maximum operating junction temperature can be calculated from equation (12).

$$T_{J(PGD)} = 0.42\ W \times 50^{\circ}C/W + 85^{\circ}C = 106^{\circ}C \quad (22)$$

Or a 21°C rise in junction temperature contributed from power dissipation in the synchronous rectifier.

8.4 Increased MTBF by Reduced Junction Temperature

One of the most popular methods for calculating MTBF is by use of MIL–HDBK–217. Commonly use in commercial as well as military systems, MIL–HDBK–217 assigns failure rates for various components based upon operating environment, applied electrical stress and operating temperature. For semiconductor devices such as MOSFETs, knowing the maximum operating junction temperature is particularly important for accurately assigning the correct failure rate. Higher junction temperatures correspond to higher device failure rates, which in turn result in higher system failure rates. Likewise, higher failure rates result in lower MTBF meaning more repairs more often.

Keeping all operating parameters the same, and comparing adaptive delay control to Predictive Gate Drive™, a junction temperature reduction (38.85°C down to 21°C) of 46% is mathematically shown.

For operating in a maximum ambient environment of 85°C, a typical MIL–HDBK–217 failure rate calculation is:

$$\lambda_p = \lambda_b \times \pi_T \times \pi_A \times \pi_Q \times \pi_E \ \left(\frac{Failures}{10^6\ Hours}\right) \quad (23)$$

and

$$\text{MTBF} = \frac{1}{\lambda_p} \tag{24}$$

where:

- λ_p = device failure rate
- λ_b = base failure rate
- π_T = temperature factor
- π_A = application factor
- π_Q = quality factor
- π_E = environmental factor

Section 6.4 of MIL–STD–217F contains the base failure rate and various operating factors for a MOSFET device. The following constants are assigned:

- λ_b = 0.012 for MOSFET device
- $\pi_{T(ADC)}$ = 5.0 for adaptive delay control operating at 123.85°C junction temperature
- $\pi_{T(PGD)}$ = 3.9 for Predictive Gate Drive™ control operating at 106°C junction temperature
- π_A = 1.5 for power rating < 2 W
- π_Q = 8.0 for plastic component case
- π_E = 6.0 for ground fixed operating environment

All of the above constants are fixed and similar to both adaptive delay control and Predictive Gate Drive™, except for the temperature factor which varies based upon maximum junction temperature. Inserting the above constants into equation (23), the failure rate and MTBF for the synchronous rectifier can now be determined for each case:

8.4.1 For Adaptive Delay Control

$$\lambda_{p(ADC)} = 0.012 \times 5.0 \times 1.5 \times 8.0 \times 6.0 = 4.32 \left(\frac{\text{Failures}}{10^6 \text{ Hours}}\right) \tag{25}$$

$$\text{MTBF}_{(ADC)} = \frac{10^6}{5.05} = 231,481 \left(\frac{\text{Failures}}{10^6 \text{ Hours}}\right) \tag{26}$$

8.4.2 For Predictive Gate Drive

$$\lambda_{p(PGD)} = 0.012 \times 3.9 \times 1.5 \times 8.0 \times 6.0 = 3.37 \left(\frac{\text{Failures}}{10^6 \text{ Hours}}\right) \tag{27}$$

$$\text{MTBF}_{(PGD)} = \frac{10^6}{3.37} = 296,736 \left(\frac{\text{Failures}}{10^6 \text{ Hours}}\right) \tag{28}$$

Due to a 16.8% (106°C versus 123.85°C) increase in device junction temperature, the adaptive delay control driven synchronous MOSFET experiences a component failure rate 28.2% higher and an MTBF 22% lower than the same synchronous rectifier operating under the same conditions using the Predictive Gate Drive™ technique.

8.4.3 Increased Output Current

$$P_{SR(PGD)} = P_{COND(PGD)} = 0.048\ W + 0.117\ W = 0.777\ W \quad (29)$$

Solving for the conduction loss allowed using Predictive Gate Drive™ that would yield the same 123.85°C junction temperature as adaptive delay control:

$$P_{COND(PGD)} = 0.777\ W - 0.048\ W - 0.117\ W = 0.612\ W \quad (30)$$

Based upon an allowable conduction loss of 0.612 W, the amount of output current that the synchronous rectifier could now commutate can be calculated be rearranging equation (8) and solving for output current:

$$I_{OUT} = \sqrt{\frac{0.612\ W}{\left(3 \times 10^{-3}\Omega\right) \times \left(1 - \frac{1.8\ V}{12\ V}\right)}} = 15.5\ A \quad (31)$$

Compared to adaptive delay control, Predictive Gate Drive™ allows 55% (15.5 A vs. 10 A) more output current for the same junction temperature of 123.85°C.

8.4.4 Increased Switching Frequency

Since the synchronous rectifier switches at zero voltage, only the reverse recovery and body-diode conduction losses are a function of switching frequency. By adding equation (2) to equation (10), an expression can be derived to relate switching frequency to total body-diode loss:

$$P_{D(PGD)} + P_{RR(PGD)} \quad (32)$$

$$= \left(V_F \times I_{OUT} \times f_{SW} \times 2 \times t_{BD}\right) + \left(\frac{1}{2} \times Q_{RR} \times V_{IN} \times f_{SW}\right)$$

And solving equation (32) for f_{SW} gives:

$$f_{SW} = \frac{2 \times \left(P_{DISS(PDG)} + P_{RR(PGD)}\right)}{V_F \times I_{OUT} \times 4 \times t_{BD} + Q_{RR} \times V_{IN}} \quad (33)$$

Solving for the total body-diode loss (conduction and reverse recovery) allowed using Predictive Gate Drive™ that would yield the same 123.85°C junction temperature as adaptive delay control:

$$P_{D(PGD)} + P_{RR(PGD)} = P_{SR(PGD)} - P_{COND(PGD)} \quad (34)$$

$$= 0.777\ W - 0.255\ W = 0.522\ W$$

Using Predictive Gate Drive™ control and based upon an allowable total body-diode loss of 0.522 W, the maximum frequency that the synchronous rectifier could now switch at is calculated by substituting known values into equation (33):

$$f_{SW} = \frac{2 \times 0.522\ W}{0.8\ V \times 10\ A \times 4 \times \left(10 \times 10^{-9}s\right) + \left(130 \times 10^{-9}C\right) \times 12\ V} = 555\ kHz \quad (35)$$

Compared to adaptive delay control, Predictive Gate Drive™ allows an 85% (555 KHz vs. 300 KHz) increase in switching frequency for the same junction temperature of 123.85°C.

In addition to the synchronous rectifier switching at zero voltage, it is also subject to minimal frequency related body-diode losses when Predictive Gate Drive™ is employed. As such, this device is selected primarily based upon conduction loss (low $R_{DS(on)}$). Even so, because the total losses related to switching frequency are so low, the synchronous rectifier MOSFET is able to operate at very high switching frequencies compared to a similar device used in an adaptive delay control application. The limiting device however, will be the upper high-side MOSFET of the synchronous buck. This device is switching frequency limited and so it is typically selected based upon lowest gate charge requirements.

Using the Predictive Gate Drive™ technique, three means have been highlighted on how the additional efficiency savings in the synchronous rectifier can best be applied. A calculated comparison was performed between the Predictive Gate Drive™ technique and the adaptive delay control for identical operating conditions. Specifically the losses associated with the synchronous rectifier of a typical synchronous buck power stage were determined for each case. The results are summarized in Table 2.

Table 2. Synchronous Rectifier Benefits From Predictive Gate Drive™

	Parameter	Predictive Gate Drive™	Adaptive Delay Control	Predictive Gate Drive™ Benefits
1	Power Dissipation	0.42 W	0.777 W	46% reduction in synchronous rectifier power dissipation.
	Junction Temperature(1)	106°C	123.85°C	14.4% junction temperature reduction in +85 °C ambient.
	Failure Rate(1)	3.37 Failures/10^6Hours	4.32 Failures/10^6Hours	22% failure rate reduction for identical electrical specifications and operating environment.
	MTBF(1)	296,736 Hours/Failure	231,481 Hours/Failure	28.2% MTBF increase for identical electrical specifications and operating environment.
2	Output Current	15.5 A (T_J = 123.85°C)	10 A (T_J = 123.85°C)	55% more output current for same T_J.
3	Switching Frequency	555 KHz (T_J = 123.85°C)	300 KHz (T_J = 123.85°C)	85% increase in switching frequency for same T_J.

(1) These parameters are directly related to power dissipation and so all become benefits of choice 1.

Using equation (3), a check can be performed to estimate how much efficiency gain Predictive Gate Drive™ technology can offer over adaptive delay control for the design parameters used in this example.

$$\frac{P_D}{P_{OUT}} = \left[\frac{0.8\ V}{1.8\ V} \times \left(300 \times 10^3\ Hz\right) \times 2 \times \left(60 \times 10^{-9}\ s\right)\right] \times 100\% = 1.6\% \quad (36)$$

9 Summary

A significant portion of the total losses within a synchronous rectifier occurs as a result of internal body-diode conduction. Historically, there have been two prevailing technologies that have addressed this issue, fixed delay and adaptive delay control. While adaptive delay control has offered significant improvements over the fixed delay technique, it still has major shortcomings.

Recently an innovative new digital control technique has been introduced that effectively eliminates body-diode conduction in synchronous rectifiers. The Predictive Gate Drive™ control technique has been shown to offer major improvements over adaptive delay. The efficiency improvements become greater for higher frequency, lower output voltage applications.

It has been quantitatively shown that the efficiency savings over adaptive delay control can be translated to lower component failure rate, and higher MTBF, or increased output current for similar junction temperatures, or higher switching frequency for similar junction temperatures.

The Predictive Gate Drive™ control technique can be applied to either isolated or non-isolated power topologies. The advantages of Predictive Gate Drive™ control would be especially beneficial in multiphase power converters. The potential efficiency savings in these applications could have a cumulative effect where two to several synchronous buck power stages are operated in parallel.

10 References

1. *UCC27221/2 Predictive Gate Drive™ FAQ's* (SLUA280)
2. *Design and Application Guide for High Speed MOSFET Gate Drive Circuits* (SLUP169)
3. *Implication of Synchronous Rectifiers in Isolated, Single-Ended, Forward Converters* (SLUP175)
4. UCC27221/2 *High-Efficiency Predictive Synchronous Buck Driver* (SLUS486A)
5. TPS40000/1/2/3 *Low-Input Voltage-Mode Synchronous Buck Controller* (SLUS507A)
6. *UCC27222EVM, 12V to 1.8V, 20A High–Efficiency Synchronous Buck Converter Using UCC27222 with Predictive Gate Drive™ Technology*, (SLUU140)
7. Military Handbook, *Reliability Prediction of Electronic Equipment*, MIL–HDBK–217F, Department of Defense, Washington DC, 2 December 1991

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