# Analysis of a Self Turn-on Phenomenon on the Synchronous Rectifier in a DC-DC Converter 

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#### Abstract

: In the buck converter with MOS Fets, the low side switch, which must be still in cutoff state, becomes turn-on when the high side switch is turned-on and the current flows through the circuit of the power supply, the high side switch and the low side switch. We call this phenomenon self turn-on. The power dissipation by this current becomes higher when the switching frequency of the converter is high as $\mathbf{M H z}$. This self turn-on occurs easily in the converter of low output voltage and high voltage conversion ratio. We present the principle of self turn-on phenomenon on circuit simulation and experimental results.


### 1.0 Introduction

Supply voltages of logic circuits are gradually lowered for decreasing power loss and heat generation in the high speed logic operation. In buck converters of the low output voltage, a main part of power dissipation occurs in a freewheel diode and the conversion efficiency becomes low. For decreasing the diode loss, a Schottky barrier diode SBD of low forward voltage drop is used. And a MOS Fet as a low side switch is widely used in parallel with this SBD for higher conversion efficiency.
In some case, when the high side switch is turned on, the low side switch MOS Fet becomes turn-on which must be still off state. At this moment both switches of the high side and the low side are simultaneously in conduction state, and the high current flows through both switches from the power supply. Here we call this phenomenon self turn-on. The current of this phenomenon causes the heat generation of both switches and the voltage spike noise. The total conversion efficiency of the converter decreases as a result of the high-current conduction. The self turn-on occurs easily in the case of using high switching frequency with no soft switching and the high voltage conversion ratio of the low output voltage.

### 2.0 Analysis of Self Turn-on Phenomenon

Fig. 1 shows the DC-DC converter of the conventional buck type with a MOS Fet switch Q2 in parallel with a Schottky diode D. Fig. 2 shows the equivalent circuit for analyzing the self turn-on of the low side switch Q2. In this simulation, we use piecewise linear models for the MOS Fet and the Schottky diode. The reason for using piecewise linear models is to make the analysis simple and to get the effects of these parameters separately. For the MOS Fet, when the gate voltage vg becomes greater than the gate threshold voltage Vth, the drain current $\mathrm{id}=\mathrm{Gm}\left(\mathrm{vg}-\mathrm{V}_{\text {th }}\right)$, and when vg is less than


Fig. 1 DC-DC Converter of the Buck Type for Low Output Voltage


Fig. 2 Equivalent Circuit for Analyzing Self Tum-on of low side switch
$V_{\text {th, }}$ id $=0$. For the Schottky diode, when the anode forward voltage va becomes greater than the barrier voltage Vf, the diode current is $\mathrm{i}_{\mathrm{a}}=\mathrm{Gd}(\mathrm{Va}-\mathrm{Vf})$, and when va is less than Vf , $\mathrm{i}_{\mathrm{a}}=0$. In this circuit, $\mathrm{va}=-\mathrm{vd}$.
In Fig. 2, a constant current source Io is assumed for Lo , Co and Rt in Fig. 1 because of sufficiently low cut-off frequency of the load in comparison to the self turn-on phenomenon. L is stray inductances of the feeding wire and the high side switch Q1. Cgd is a gate-drain capacity of Q2. Cgs is a gatesource capacity. Cds is a drain-source capacity and includes a capacity of the diode D and a stray capacity of the drain.
We get the simulation results shown in Fig. 3 for i, vd and vg in the circuit shown in Fig. 2. Here, $i$ is the sum of the currents of Q2, D, Cds and Cgd. In this simulation, we use the following parameters.
$V_{s}=3 \mathrm{~V}, \mathrm{~L}=10 \mathrm{nH}, \mathrm{I}_{\mathrm{o}}=10 \mathrm{~A}, \mathrm{Vf}=1.0 \mathrm{~V}, \mathrm{~V} \mathrm{th}=1.0 \mathrm{~V}, \mathrm{Cds}=10 \mathrm{nF}$, $\mathrm{Cgd}_{\mathrm{g}}=10 \mathrm{nF}$ and $\mathrm{Cgs}=20 \mathrm{nF}$. And we use $\mathrm{Vb}=-0.4 \mathrm{~V}$. Here, Vb is the bias gate voltage which is the initial gate voltage of Q2 at the moment Q 1 turns on. We assume $\mathrm{Gm}=100$ and $\mathrm{Gd}=100$ for the simple analysis which do not affect the simulation wave forms.

Fig. 3 shows that four states occur after the high side switch turns on. We set the state name from (I) to (V) as in Fig. 3. These state names correspond to the names of the equivalent circuits in Fig. 4.
In the state (I) when Q1 is in cutoff, the output current Io flows the Schottky diode which is shown by Vf in Fig. 4(I). When Q2 turns on, the stage changes from (I) to (II).

In the state (II), Io consists of the diode current and the inductor current. As the diode is in conduction, vd=-Vf. We get the circuit equation in the state (II) as follows.

$$
\mathrm{L} \frac{\mathrm{di}}{\mathrm{dt}}=\mathrm{Vs}+\mathrm{Vf}
$$

and the initial condition of $\mathrm{i}(0)=-\mathrm{I}$.
From this equation, we get

$$
i(t)=-I o+\frac{V s+V f}{L} t
$$

The state changes form (II) to (III), when $\mathrm{i}(\mathrm{t})=0$ and the diode becomes off. C in the equivalent circuit (III) in Fig. 4 is a composite capacitor of $\mathrm{Cds}, \mathrm{Cgd}$ and Cgs , where Cds contains the diode capacitor and a stray capacity. We get the circuit equation in the state (III) as follows.

$$
\begin{aligned}
& \mathrm{L} \frac{\mathrm{~d} \mathrm{i}}{\mathrm{dt}}+\frac{1}{\mathrm{C}} \int \mathrm{idt}=\mathrm{Vs} \text { and initial conditions are } \\
& \mathrm{i}(0)=0 \text { and } \mathrm{vd}(0)=-\mathrm{Vf} .
\end{aligned}
$$

From these equations, we get

$$
i(t)=\frac{V s+V f}{Z o} \sin \omega_{0} t
$$

and $\mathrm{vd}(\mathrm{t})=\mathrm{Vs}-(\mathrm{Vs}+\mathrm{Vf}) \cos \omega_{0} \mathrm{t}$.
Here, $Z o=\sqrt{\frac{L}{\mathrm{C}}}, \omega_{0}=\frac{1}{\sqrt{\mathrm{LC}}}$.
In these equations, we set $t=0$ at the starting point of each state. The variation of vd , that is, $\mathrm{vd}+\mathrm{Vff}_{\mathrm{f}}$ is divided by Cgd and Cgs and is imposed to the initial voltage -Vb. So we get the equation for the gate voltage vg of $\mathrm{Q}_{2}$ as follows.

$$
\begin{aligned}
& \operatorname{vg}(\mathrm{t})=-\mathrm{Vb}+\frac{\mathrm{vd}(\mathrm{t})+\mathrm{Vf}}{\mathrm{n}} \\
& \text { and } \mathrm{n}=\frac{\mathrm{Cgd}+\mathrm{Cgs}}{\mathrm{Cgd}} .
\end{aligned}
$$



Fig. 3 Simulation Results for Self Turn-on
n is a voltage dividing coefficient from the drain to the gate of $Q_{2}$.

When vg rises up to the gate threshold voltage Vth at $\mathrm{t}=\tau, \mathrm{Q} 2$ becomes to the active state. When $\mathrm{vg}=\mathrm{V}_{\mathrm{th}}, \mathrm{vd}$ is given by $V \mathrm{dm}=\mathrm{n}(\mathrm{Vth}+\mathrm{Vb})-\mathrm{Vf}$.
At the same time, this $V d m$ is equal to $v d(\tau)$. We can get $\alpha=\omega_{0} \tau$ from the next equation.

$$
\mathrm{Vs}-(\mathrm{Vs}+\mathrm{Vf}) \cos \alpha=\mathrm{n}(\mathrm{Vth}+\mathrm{Vb})-\mathrm{Vf}
$$

We get $\operatorname{Im}$, that is, $\mathrm{i}(\mathrm{t})$ at the end of the state (III).

$$
\mathrm{Im}=\frac{\mathrm{Vs}+\mathrm{Vf}}{\mathrm{Zo}} \sin \alpha
$$

In the state (IV) after $\mathrm{vg}=\mathrm{V}$ th, vd is kept constant as $\mathrm{n}\left(\mathrm{V}_{\mathrm{th}}+\mathrm{V}_{\mathrm{b}}\right)$ - $\mathrm{Vf}_{\mathrm{f}}$ shown in Fig. 4 (IV). A reason for this is described in an appendix at the end of this paper. We get the circuit equations in the state (IV) as follows.

$$
\mathrm{L} \frac{\mathrm{di}}{\mathrm{dt}}=(\mathrm{Vs}+\mathrm{Vf})-\mathrm{n}(\mathrm{Vth}+\mathrm{Vb})
$$

and $i(0)=I m$
From these equations, we get

$$
i(t)=\operatorname{Im}-\frac{\mathrm{n}(\mathrm{Vth}+\mathrm{Vb})-(\mathrm{Vs}+\mathrm{Vf})}{\mathrm{L}} \mathrm{t}
$$

As the next state $(V)$ starts when $i\left(\tau_{2}\right)=0$, we get

$$
\tau 2=\frac{L \operatorname{lm}}{n(V t h+V b)-(V s+V f)}
$$

We will get the current I4 in the state (IV), that is, the current caused by the self turn-on.

From $\mathrm{I} 4=\frac{1}{\tau 2} \int_{0}^{\tau 2} \mathrm{i}(\mathrm{t}) \mathrm{dt}$, we get

$$
\mathrm{I} 4=\frac{\mathrm{L}}{2} \frac{\left(\frac{\mathrm{Vs}+\mathrm{Vf}}{\mathrm{Zo}} \sin \alpha\right)^{2}}{\mathrm{n}(\mathrm{Vth}+\mathrm{Vb})-(\mathrm{Vs}+\mathrm{Vf})} .
$$

As vd is kept constant $\mathrm{n}\left(\mathrm{V}_{\mathrm{th}}+\mathrm{Vb}_{\mathrm{b}}\right)-\mathrm{Vf}$ in the state (IV), the dissipation caused by the self turn-on is expressed by

$$
\mathrm{I} 4\left\{\mathrm{n}\left(\mathrm{Vth}_{\mathrm{t}}+\mathrm{V}_{\mathrm{b}}\right)-\mathrm{V}_{\mathrm{f}}\right\} .
$$

This dissipation occurs in one switching cycle, so the dissipation P4 of Q2 operating on switching frequency fs is expressed as follow.

$$
\mathrm{P}_{4}=\mathrm{I} 4\{\mathrm{n}(\mathrm{Vth}+\mathrm{Vb})-\mathrm{Vf}\} \mathrm{fs}
$$

This equation leads to the next.

$$
\begin{aligned}
\mathrm{P} 4 & =\frac{\mathrm{C}}{2} \frac{(V s+V f)^{2}-(\mathrm{nVth}+V b-V s)^{2}}{\mathrm{n}(\mathrm{Vth}+V b)-(V s+V f)}\{n(V t h+V b)-V f\} f s \\
& =\operatorname{Pc} \frac{\mathrm{x}^{2}(2-x)}{x-1}=\mathrm{Pc}^{*} \gamma
\end{aligned}
$$

Here, $P c=\frac{C}{2}(V s+V f)\left\{V s+\left(1-\frac{1}{x}\right) V f\right\} f s$

$$
\approx \frac{C}{2}(V s+V f)^{2} f s
$$

$$
x=\frac{n(V t h+V b)}{V s+V f} \text { and } \gamma=\frac{x^{2}(2-x)}{x-1}
$$

Pc is nearly equal to the power dissipated in repeating charge and discharge of C with the voltage $\left(\mathrm{Vs}+\mathrm{Vff}_{\mathrm{f}}\right.$ ) in frequency fs .

For example, $\mathrm{P}_{\mathrm{c}}=0.05 \mathrm{~W}$ in the case $\mathrm{C}=20 \mathrm{nF},(\mathrm{Vs}+\mathrm{Vf})=5 \mathrm{~V}$ and $\mathrm{fs}_{\mathrm{s}}=200 \mathrm{kHz}$.
$\gamma$ is an increasing coefficient of dissipation. Fig. 5 shows a relation of $\gamma$ vs. x . The power dissipation $\mathrm{P}_{4}$ caused by self turn-on increases sharply when $x$ is getting near to 1 . In the region of $x \leq 1$ which is not shown in Fig. 5, $\mathrm{vd}(=\mathrm{Vdm})$ in the state (IV) is less than the supply voltage Vs. As the low side switch cannot block $V_{s}$ in this condition, the current from Vs increases as time goes on. In the region of $x \geq 2$, the gate voltage vg doesn't reach to the threshold voltage and the state (IV) does not appear in the switching sequence.


(III)

(IV)


Fig. 4 The Equivalent Circuits for States from (I) to (V)

(a) $\boldsymbol{\gamma}$ for $1 \leq \mathrm{x} \leq 2$

(b) $\gamma$ for $1 \leq \mathrm{x} \leq 1.1$

Fig. 5 Multiplying Coefficient $\gamma$ of the Dissipation due to Self Turn-on of Low Side Switch


Fig. 6 Experimental Circuit for Self Turn-on of Low Side Switch

### 3.0 Experimental Circuit and Results

Fig. 6 shows an experimental circuit to verify the self turnon phenomenon. The high side switch Q 1 is controlled by PWM generator as the output voltage is keeping $5 \mathrm{~V}(2.5 \mathrm{~A}$, 12.5 W ). The low side switch is not driven. A capacitor 560 pF between the drain-gate of the low side switch Q2 decreases $n$, that is, the voltage dividing coefficient from drain to gate and makes the self turn-on easy to occur. Fig. 7 shows the experimental results on the total dissipation Pl vs. the supply voltage V s. We can see $\mathrm{P}_{1}$ increases abruptly when Vs exceeds 19V. Fig. 8 shows that this dissipation characteristic is depending to the self turn-on. Waveforms in Fig. 8 show vd, vg and iin Fig. 6 just after Q1 turns on. The upper cursor lines in vgs' waveforms are the threshold voltage Vth( 4.0 V ). When the input voltage $\mathrm{V}_{\mathrm{s}}$ is 17 V , Fig. 8(1) shows that the self turn-on time Ts is very short. When $\mathrm{V}_{\mathrm{s}}=18 \mathrm{~V}$, Fig. 8(2) shows Ts increases but the current i becomes 0 soon. When $\mathrm{V}_{\mathrm{s}}=19 \mathrm{~V}$, Fig. 8(3) shows Q2 cannot block the current because vg is over Vth slightly. When $\mathrm{V}_{\mathrm{s}}=20 \mathrm{~V}$, Fig. 8(4) shows the current i flows through $\mathrm{V}_{\mathrm{s}}, \mathrm{Q} 1$ and Q2 for a whole period when Q1 is turn on. This increment of the current makes the dissipation high and the conversion efficiency low.
Capacities of Cgd and Cgs depend on the drain-source voltage Vds. In the case of 2SK 1500 used in the experiment, a data book shows Ciss and Crss are 3.0 nF and 400 pF respectively when $\mathrm{V}_{\mathrm{ds}}=10 \mathrm{~V}$. From these values, we get $C_{g d}=400 \mathrm{pnF}$ and $\mathrm{Cgs}_{\mathrm{g}}=2.6 \mathrm{nF}$. Here evaluating the voltage dividing ratio n with 560 pF in the experimental circuit shown in Fig. 6, we get $\mathrm{n}=3.71$ as a theoretical value. From the experiment results, the variations of $\mathrm{vg}_{\mathrm{g}}$ and vd are 5.7 V and 18 V respectively as shown in wave form of Fig. 8(2). So the experimental result of $n$ is equal to 3.16 . A difference between the theoretical value and the experimental one for $n$ is small and acceptable error.


Fig. 7 Power Dissipation Pl caused by Self Turn-on vs. Supply Voltage Vs


To reduce the self turn-on dissipation, the conversion ratio of the converter from the supply voltage to the output voltage should be small and the gate threshold voltage of the MOS Fet should be high.

## References

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## Appendix

In Fig. 4(IV) when the low side switch Q2 is active, the drain voltage vd of Q 2 is kept constant. Fig. A(1) shows the block diagram for analyzing the mechanism where vd becomes constant. vd is given by subtracting the induced voltage vl of the inductor L from the input supply voltage Vs . $\mathrm{vd}^{*}$ is a variation of vd from $-\mathrm{Vf}_{\mathrm{f}}$, that is, $\mathrm{vd}^{*}=\mathrm{vd}^{2}+\mathrm{Vf}$. And $\mathrm{vd}^{*}$ is divided by Cdg and Cgs , that is, $\mathrm{vg}^{*}=\mathrm{vd}^{*} / \mathrm{n} . \quad \mathrm{vg}$ is given by $\mathrm{vg}^{*}$ imposed the initial voltage -Vb of the gate, that is, $\mathrm{vg}=\mathrm{vg}{ }^{*}-\mathrm{Vb}$. When vg exceeds the threshold voltage V th, the drain current id flows as proportional to $\mathrm{vg}^{* *}(=\mathrm{vg}-\mathrm{V}$ th $)$ where the proportional constant is Gm (transfer conductance).
Simplifying a block diagram shown in Fig. A(1), we get a next block diagram shown in Fig. A(2). Supposing Gm has a high value, the input signal $\mathrm{vg}^{* *}$ of Gm is nearly equal to 0 .

$$
\frac{1}{n}(v d+V f)-(V t h+V b) \approx 0
$$

We get $v d \approx n(V t h+V b)-V f$ from the above equation, that is, vd is almost constant when $\mathrm{vg} \geq \mathrm{Vth}$ and Q 2 is in active state.

(1) Precise Block Diagram showing the Mechanism for Evaluation of vd

(2) Block Diagram Simplified from (1)

Fig. A Block Diagrams showing the Mechanism where vd is kept Constant when the Low Side Switch Q2 is in Active State

