Applying SG6902 to Control a CCM PFC and Flyback/PWM Power Supply **AN6902**

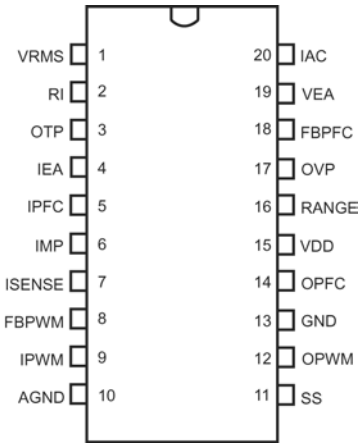
ABSTRACT

This application note shows a step-by-step design for a 120W/24V power adapter. The equations also can be used for different output voltages and wattages.

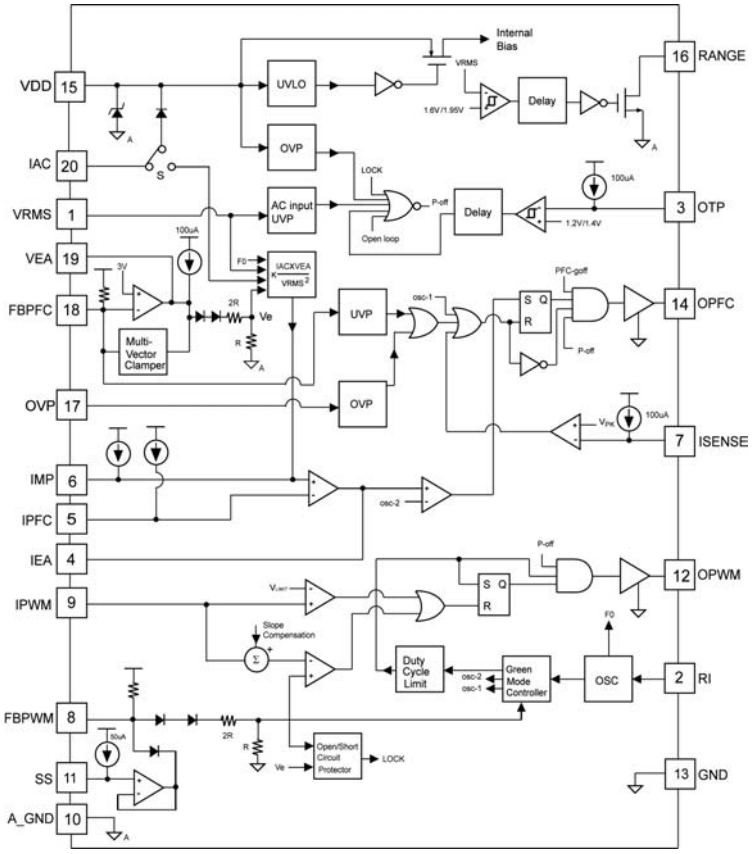
FEATURES OVERVIEW

- Interleaved PFC/PWM switching
- Green mode PFC and PWM operation
- No PFC switching at light loads for power saving
- Low start-up and operating current
- Innovative *Switching-Charge*® multiplier-divider
- Multi-vector control for improved PFC output transient response
- Average-current-mode control for PFC
- Programmable two-level PFC output voltage to achieve the best efficiency
- PFC over-voltage and under-voltage protections
- PFC and PWM feedback open-loop protection
- Cycle-by-cycle current limiting for PFC/PWM
- Slope compensation for PWM
- Maximum power limit for PWM
- Brownout protection
- Over temperature protection
- Power on sequence control and soft-start

PIN CONFIGURATION



BLOCK DIAGRAM



DESCRIPTION

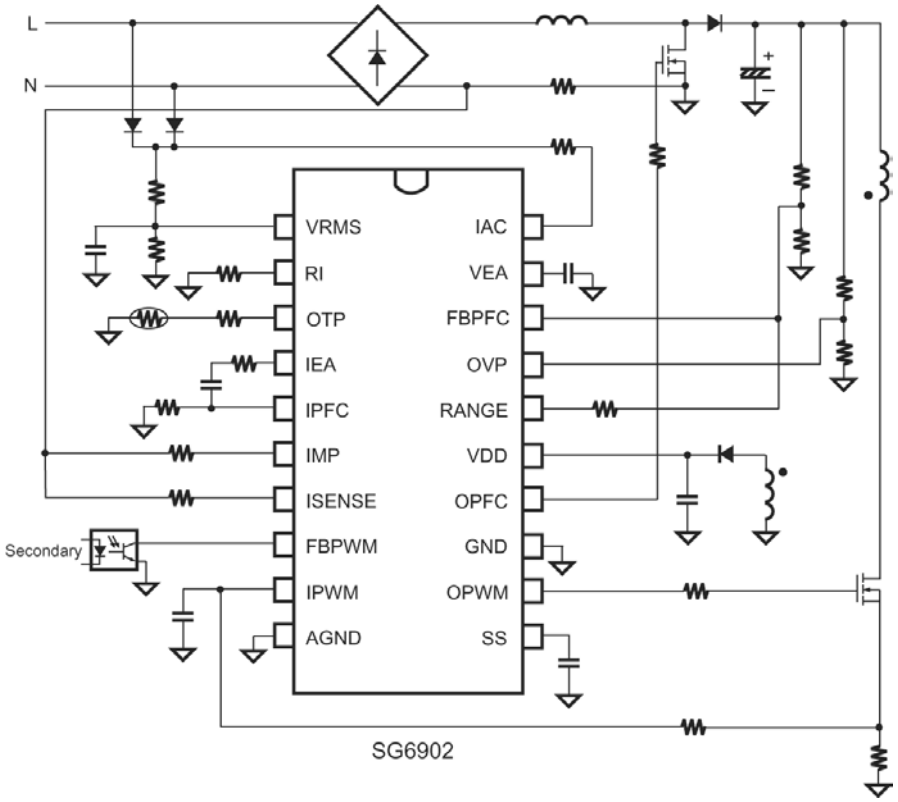
SG6902 is specially designed for power supplies consist of boost PFC and Flyback PWM. It requires very few external components to achieve green-mode operation and versatile protections/compensations. It is available in 20-pin DIP and SSOP packages.

The patented interleave-switching synchronizes the PFC and PWM stages and reduces switching noise. At light load, PFC stage will be turned off to save the power, and the PWM switching frequency is decreased in response to the decrease of the load.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop. Besides, the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, SG6902 will shut off the switching to protect the power supply and its load.

For the Flyback PWM stage, the synchronized slope compensation ensures the stability of the current loop. Furthermore, the Hiccup operation limits a maximum output power during the overloaded situations.

TYPICAL APPLICATION



PFC SECTION

SG6902 Power On Sequence

SG6902 is active once the line voltage is higher than the brownout threshold. The PWM stage is switching first, and then following an 11.5mS delay time after FBWM voltage is higher than a threshold voltage V_{TH}, the PFC stage is enabled.

PFC inductor

The switching frequency fs, the output power P_{out}, the efficiency η, maximum ripple current ΔI and the minimum input voltage $V_{in.min}$ should be defined before determining the inductance the of PFC inductor. Following equations are utilized to determine the inductance of the PFC inductor. Normally, the maximum ripple current is set as 20% ~ 30% of maximum input current.

$$\Delta I = \frac{(P_{out}/\eta)\times 0.3}{V_{in.\min}} \quad \text{---------- (1)}$$

$$D = 1 - \frac{V_{in.\min}\times\sqrt{2}}{V_O} \quad \text{---------- (2)}$$

$$V = L\frac{di}{dt} \quad \text{---------- (3)}$$

$$L = \frac{V_{in.\min}\times\sqrt{2}\times D_{\max}/f_S}{\Delta I} \quad \text{---------- (4)}$$

For a 120W Adapter power, η=0.85, $V_{in.min}$=90V_{AC}, fs=65KHz, Vo=250V

ΔI=0.47A, D=0.49, L=2mH

PFC capacitor

An advantage of using interleaving switching for PFC and PWM stage is to reduce the switching noise. The ESR requirement of boost capacitor is also reduced.

The boost capacitor value is chosen to remain a hold-up time of output voltage in the event line voltage is removed.

$$C_o > \frac{2\times(P_{out}/\eta_{PWM})\times T_{hold-up}}{(V_{o(normal)} - V_{ripple})^2 - V_{o.\min}{}^2} \quad \text{----- (5)}$$

$V_{O.min}$ means the minimum output voltage in accordance with the requirement of the specification.

For a 120W power supply, the capacitor is determined as follow:

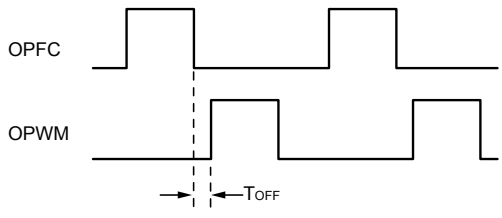


Fig.1 Interleaving Switching

$$C_O > \frac{2\times(120W/0.85)\times 15mS}{(250-20)^2-60^2} = 86uF$$

Because the capacitor include ±20% variation, the capacitor 100uF is chosen

Boost rectifier and switch

The fast reverse-recovery time of the boost diode is required to reduce the power losses and the EMI. Besides, a 500V voltage rating is chosen to withstand 400V boosts potential. The average current and peak current flow through the boost diode and the switch respectively are given by:

$$I_{avg} = \frac{2\times\sqrt{2}\times P_{out}/\eta}{\pi\times V_{RMS(Brownout)}} \quad \text{---------- (6)}$$

$$I_{avg} = \frac{2\times\sqrt{2}\times 120/0.8}{\pi\times 75} = 1.8A$$

$$I_{peak} = \sqrt{2}\times\frac{P_{out}/\eta}{V_{RMS(Brownout)}} \quad \text{---------- (7)}$$

$$I_{peak} = \sqrt{2}\times\frac{120/0.8}{75} = 2.82A$$

Oscillator & Green Mode Operation

The resistor R_I connected from R_I pin to GND programs the switching frequency of SG6902.

$$f_S = \frac{1560}{R_I(K\Omega)}(KHz) \quad \text{---------- (8)}$$

For example, a 24kΩ resistor R_I results a 65 kHz switching frequency. The recommended range for the switching frequency of SG6902 is 33kHz ~ 130kHz.

SG6902 provides an off-time modulation to reduce the switching frequency in light-load and no-load conditions. The feedback voltage of FBPWM pin is taken as reference. When the feedback voltage is lower than about 2.1V, the switching frequency will be decreased accordingly. The most of losses in a switching mode power supply are proportional to the switching frequency. Therefore, the off-time modulation of SG6902 will reduce the power consumption of the power supply in light-load and no-load conditions. For a typical case of R_I = 24KΩ, the switching frequency is 65kHz at nominal load, and decreases to 20kHz at light load. The switching signal will be disabled if the switching frequency may fall below the 20KHz, which avoids the acoustic noise.

For stability issue, a capacitor connecting from RI pin to GND is not suggested.

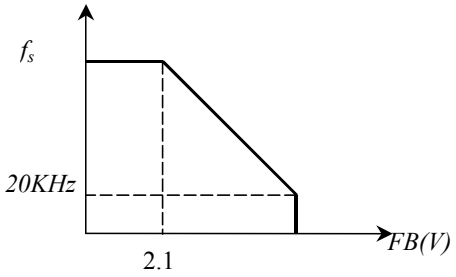


Fig2. Switch frequency versus FB voltage

In order to save the power, the PFC stage is enabled only when the feedback voltage of FBPWM pin is higher than a threshold voltage V_{TH}. The threshold voltage V_{TH} is 2.1V to 2.45V at low line voltage input, and it is 1.95V at high line voltage. Therefore the threshold voltage V_{TH} determine an output power threshold to turn on/off the PFC stage for the power saving. The output power P_{OUT} can be expressed as:

$$P_{out} = \frac{\eta \times (V_{in} \times T_{ON})^2}{2 \times L_p \times T}$$

$$V_{FB} = 1.2V + 3 \times \{\frac{V_{in(peak)}}{L_p} \times R_S \times T_{ON} + \frac{V_{SL}}{T} \times T_{ON}\} \quad \text{---------- (9)}$$

Where V_{SL} means a synchronized 0.5V ramp.

Equation (9) shows that, through the feedback loop, the on-time T_{ON} will be changed in response to the change of the switching period T and/or the inductance L_P (the primary inductance of the transformer) for providing a same output power. Because the feedback voltage V_{FB} controls the on-time T_{ON}, a lower V_{FB} causes a narrow on-time T_{ON}. Therefore, by changing the switching frequency (the switching period T) and the inductance L_P will affect the output power threshold to on/off the PFC stage.

I_{AC} signal

Figure 3 shows that the I_{AC} pin is connected to the input voltage via a resistor. A current I_{AC} is used for PFC multiplier.

$$I_{AC(peak)} \approx \frac{V_{in(peak)}}{R_{AC}} \quad \text{---------- (10)}$$

For wide range input,

$$V_{in(peak)} = 264V \times \sqrt{2} = 374V$$

The linear range of I_{AC} is 0~360uA, A 1.2M resistor is suggested for a wide input range (90VAC ~ 264VAC).

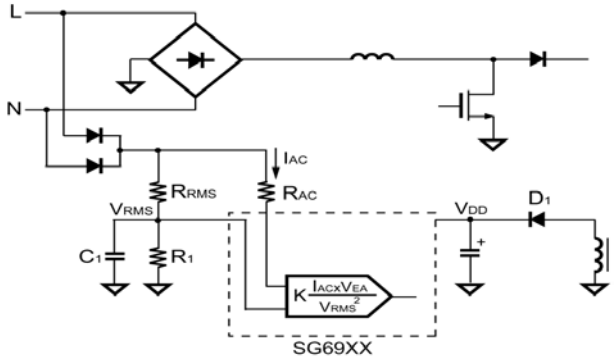


Fig. 3

Line Voltage Detection (V_{RMS})

Figure 3 shows a resistive divider form a low-pass filter connected to V_{RMS} pin for line-voltage detection. The V_{RMS} input is used for the PFC multiplier and brownout protection.

For a sine wave input voltage, the voltage on VRMS pin is directly proportional to input voltage. In order to achieve the brownout protection, the PFC stage of SG6902 is disabled after a 195mS time delays once the V_{RMS} Voltage drops below 0.8V. The PWM stage will be protected through the open loop detection on the FBPWM pin when the output voltage of the PFC stage is too low. After that, SG6902 will be turn off. When V_{RMS} voltage is higher than 0.98V, the SG6902 will be restarted in accordance with power on sequence of PFC and PWM stages.

For example, a brownout protection is set as 75VAC. The R_{RMS} and R1 can be determined as below:

$$V_{in(Mean)} = V_{in} \times \sqrt{2} \times \frac{2}{\pi} \quad \text{---------- (11)}$$

$$V_{RMS} = \frac{R1}{R1 + R_{RMS}} \times Vin \times \sqrt{2} \times \frac{2}{\pi} \quad \text{----------(12)}$$

The threshold of V_{RMS}=0.8V; assume R_{RMS}=4.8MΩ and Vin=75V_{AC}, then the value of R1 will be 56.8KΩ.

PFC Operation

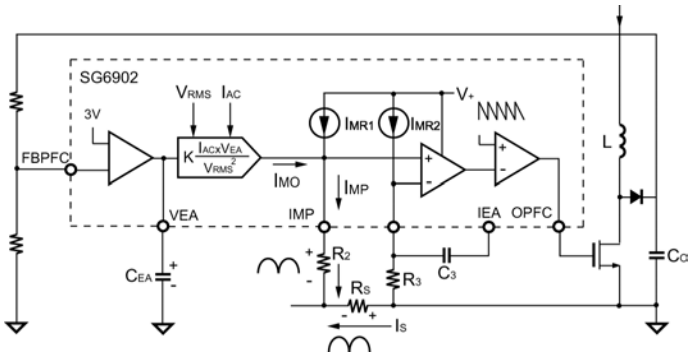


Fig. 4

The current output from the *Switching Charge*® multiplier/divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^{\ 2}} (uA) \quad \text{---------- (13)}$$

Refer to Fig. 4, the current output from IMP pin, I_{MP}, is the summation of I_{MO} and I_{MR1}. The resistor R_2 is equipped as same as R_3. The constant current source I_{MR1} is identical with I_{MR2}. They are used to bias (pull high) the operating point of the IMP and IPFC pins since the voltage across R_S goes negative with respect to ground.

Through the differential amplification of the signal across Rs, a better noise immunity is achieved. The output of IEA compared with an internal sawtooth generates a switching signal for PFC. Through the feedback loop of the average current mode control, the input current I_S is proportional to I_{MO},

$$I_{MO} \times R_2 = I_S \times R_S \quad \text{---------- (14)}$$

According to equation 14, the minimum value of R2 and maximum value of Rs can be determined. The I_{MO} should be estimated under its specified maximum value.

Other concerns in determining the value of the sense resistor Rs are a lower resistance Rs will cause a lower power consumption a higher resistance Rs has a higher resolution to achieve lower THD (total harmonic distortion) of the input current. Recommend using a current transformer (CT) instead of Rs to improve the efficiency of high power converters.

For a 120W Adapter, the power consumption of R_S=0.36Ω is :

$$P_{RS} = (\frac{120W/0.85}{90})^2 \times 0.36 = 0.885W \quad \text{---------- (15)}$$

R2 and R3 can be determined as follow:(The brownout protection threshold is 75V)

$$I_{MAX} = \frac{120W/0.8}{75V} \times \sqrt{2} = 2.83A \quad \text{---------- (16)}$$

$$I_{MO} = \frac{R_S \times I_{MAX}}{R_2} \quad \text{---------- (17)}$$

$$I_{MO} = \frac{0.36 \times 2.83}{3.3K} = 308uA \quad \text{---------- (18)}$$

The result shows that R_S, R2 and R3 values are fit for providing 120W output.

Cycle-by-cycle Current Limiting

SG6902 provides cycle-by-cycle current limiting for both PFC and PWM stages. Fig. 5 shows the peak current limit for the PFC stage. The switching signal of PFC stage will be turned off immediately once the voltage on ISENSE pin goes below the threshold voltage V+.

The voltage of V_{RMS} determines the threshold voltage V+. The correlation of the threshold voltage V+ and VRMS is shown in Fig. 5.The amplitude of the constant current I_P shown in Fig. 5 is determined by a reference current I_T, in accordance with the following equation:

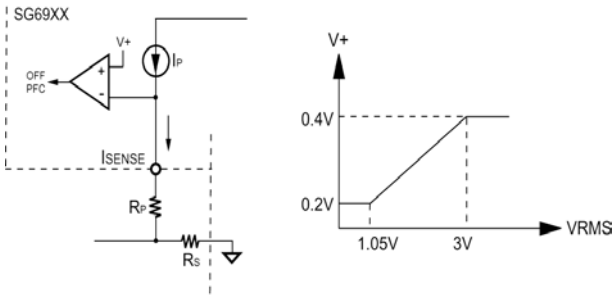


Fig. 5 Current limit

$$I_P = 2 \times I_T = 2 \times \frac{1.2V}{R_I} \quad \text{---------- (19)}$$

Therefore the peak current of the I_S can be expressed as:

$$I_{S\_PEAK} = \frac{(I_P \times R_P) - 0.2V}{R_S} \quad \text{---------- (20)}$$

Multi-vector Error Amplifier

To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as DC-value according to equation (12). In other words, a low-pass RC filtering for V_{RMS} and a narrow bandwidth (lower than the line frequency) of PFC voltage loop are suggested to achieve better input current shaping. The trans-conductance error amplifier has output impedance R_O (>90kΩ). A capacitor C_{EA} (1uF ~ 10uF) is suggested to connect from the output of the error amplifier to ground (Fig. 6). A dominant pole f_1 of the PFC voltage loop is shown as:

$$f_1 = \frac{1}{2\pi \times R_O \times C_{EA}} \quad \text{---------- (21)}$$

The average total input power can be expressed as:

$$Pin = Vin_{(RMS)} \times Iin_{(RMS)}$$

$$\propto V_{RMS} \times I_{MO}$$

$$\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^{\ 2}}$$

$$\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}^{\ 2}} \propto V_{EA} \quad \text{---------- (22)}$$

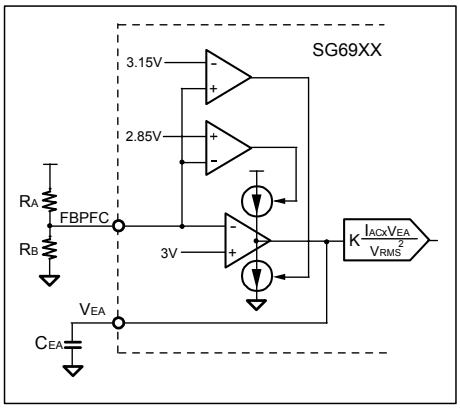


Fig. 6 Multi-vector Error Amp

The equation (22) shows the output of the voltage error amplifier, V_{EA}, controls the total input power and the power delivered to the load.

Although the PFC stage includes a low bandwidth loop to reach a better power factor, the innovated *Multi-Vector Error Amplifier* provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Fig. 6 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage (FBPFC) exceeds ± 5% of the reference voltage (3V), the trans-conductance error amplifier will program its output current to speed up the loop response. If R_A is open circuit, SG6902 will turn off immediately to prevent over-voltage on the output capacitor.

Two-level PFC output voltage

For universal input (90VAC ~ 264VAC), the output voltage of PFC is usually designed to 250V at low line and 400V at high line. This is to improve efficiency of the power converter for low-line input. The RANGE pin (open-drain) of SG6902 is used for the two-level output voltage setting.

Fig. 7 shows the RANGE output that programs the PFC output voltage. The RANGE output is shorted to ground when the V_{RMS} voltage exceeds 1.95V. It is a high impedance output (open) whenever the V_{RMS} voltage drops below 1.6V. The output voltages can be determined using below equations.

$$Range = Open \Rightarrow V_O = \frac{R_A + R_B}{R_B} \times 3V \quad \text{---------- (23)}$$

$$Range = Gnd \Rightarrow V_O = \frac{R_A + (R_B // R_c)}{(R_B // R_c)} \times 3V \quad \text{---- (24)}$$

Determine the resistor divider ratio R_A/R_B

$$\frac{R_A}{R_B} = \frac{V_O}{3} - 1 \quad \text{---------- (25)}$$

$$\frac{R_A}{R_B} = \frac{250}{3} - 1 = 82.33$$

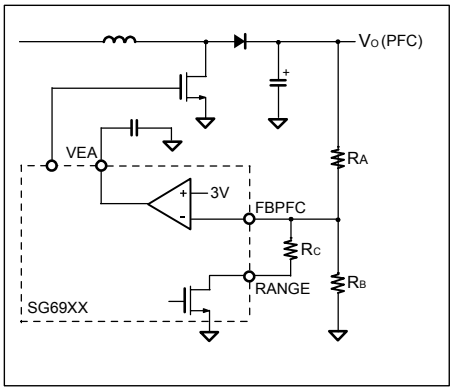


Fig 7. Feedback voltage of PFC

Assume R_A is 3MΩ, R_B=36.5KΩ and R_C=60KΩ. Refer to Fig.6 .At high line input the maximum output voltage is:

$$V_{O(MAX)} = 3.15 \times (\frac{R_A}{R_B // R_C} + 1) = 420V$$

Beside, another circuit provides further over-voltage protection to inhibit the PFC switching once the feedback voltage exceeds the 3.25V the output voltage is clamped at:

$$V_{O(OVP)} = 3.25 \times (\frac{R_A}{R_B // R_C} + 1) = 433V$$

PWM SECTION

Soft start of the PWM stage

The soft-start pin is developed to control the rising time of the output voltage and to prevent the overshoot during power on. The soft-start capacitor value for the soft start period t_{SS} is given by:

$$C_{SS} = t_{SS} \times \frac{I_{SS}}{V_{OZ}} \quad \text{---------- (26)}$$

Where V_{OZ} means the zero-duty threshold of FBPWM voltage.

Leading Edge Blanking

A voltage signal develops on the current-sense resistor R_S represents the switching current of MOSFET. Each time the MOSFET turned on, a spike will be produced, which is caused by the diode reverse recovery time and by the parasitic capacitances of the MOSFET, inevitably appears on the sensed signal. The SG6902 has a build-in leading edge blanking time about 350nsec to avoid premature termination of MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100ohm + 47pF) is still required between the IPWM pin and R_S to prevent negative spike into the IPWM pin. A non-inductive resistor for the R_S is recommended.

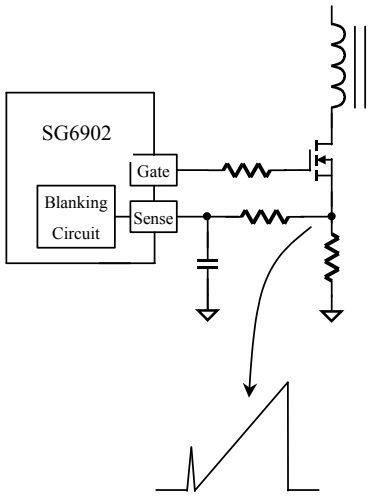


Fig. 8 Turn on spike

Flyback PWM and Slope Compensation

As shown in Fig.9, peak-current-mode control is utilized for Flyback PWM. The SG6902 inserts a synchronized 0.5V ramp at the beginning of each switching cycle. This built-in slope compensation reduces the current loop gain and ensures stable operation for current-mode operation.

When the IPWM voltage, across the sense resistor, reaches the threshold voltage, 0.65V or 0.7V selected by RANGE, the OPWM will be turned off after a small propagation delay T_{PD-PWM}. This propagation delay will introduce an additional current proportional to $T_{PD-PWM}*V_{PFC}/Lp$, where V_{PFC} is the output voltage of PFC and Lp is the magnetized inductance of Flyback transformer. Since the propagation delay is nearly constant, higher V_{PFC} will result in a larger additional current and hence the output power limit is higher than that of the low V_{PFC}. To compensate this variation, the peak current threshold is modulated by the RANGE output. When RANGE is shorted to GND, the PFC output voltage is higher and the corresponding threshold is 0.65V. When RANGE is opened, the PFC output voltage is lower and the corresponding threshold is 0.7V. On the other hand, we also can increase the inductance of transformer to improve this phenomenon.

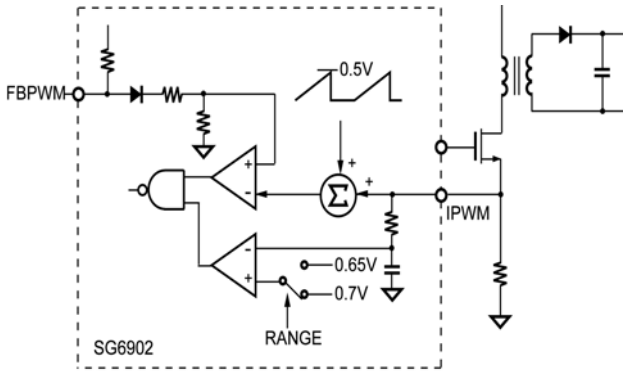


Fig. 9 Gate drive

Output driver of OPFC & OPWM

SG6902's OPFC & OPWM is a fast totem-pole gate driver that is able to directly drive external MOSFET. An internal zener diode clamps the driver voltage under 18V to protect MOSFET from over voltage.

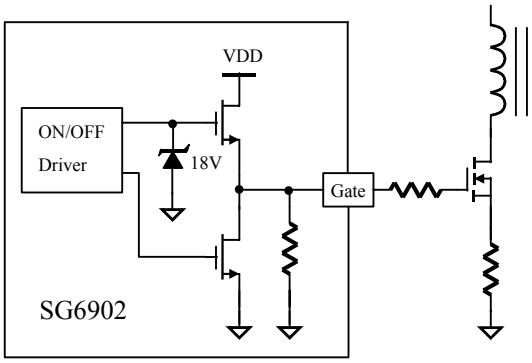


Fig.10 Gate drive

OCP & SCP

SG6902's OCP & SCP is developed base on the detection of feedback signal on FBPWM pin. Shown as Fig. 11, over current or short circuit occurred, FBPWM will be pulled high through the feedback loop. If the FB voltage is higher than a threshold 4.5V, and longer than 56ms debounce time, SG6902 will be turned off. Once the Vdd is lower than the turn-off threshold voltage such as 10V, SG6902 will be UVLO (under voltage lockout) shut down. By the start up resistor, V_{DD} will be charged (up to the turn-on threshold voltage 16V) until SG6902 is enabled again. If the over loading condition still exists, the protection will take place repeatedly. This will prevent the power supply from being overheated under over loading condition. The 650ms time-out signal prevents SG6902 from being latched off when the input voltage is fast on/off.

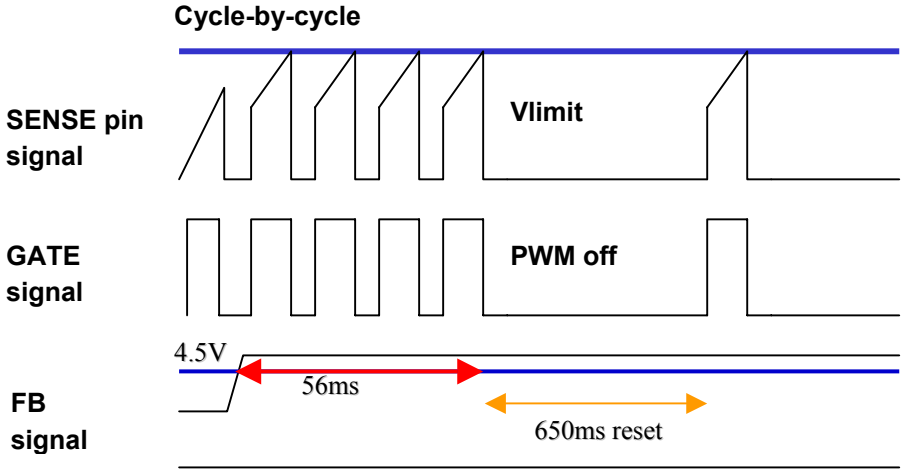


Fig. 11

OTP

SG6902 provides an OTP pin for over-temperature protection. A constant current is outputted from this pin. If RI is equal to 24kΩ, then the magnitude of the constant current will be 100uA. An external NTC thermistor must be connected from this pin to ground shown as Fig.12 When the OTP voltage drops below 1.2V, SG6902 will be disabled, until OTP voltage exceeds 1.4V.

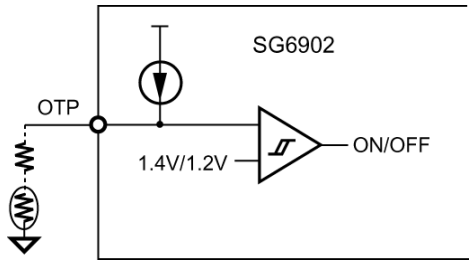


Fig.12

Flyback transformer design

The turn ratio n = Np/Ns, is an important parameter for a flyback power converter. It affects the maximum duty of the switching signal when the input voltage is in minimum value. Moreover, it also influences the voltage stresses of the MOSFET and the secondary rectifier.

Refer to equation (27) and (28), if n increases, the voltage stress of the MOSFET will be increased. However, the voltage stress of the secondary rectifier will be decreased accordingly.

$$V_{DS.\max} = V_{in.\max} + n \times (V_o + V_f) \quad \text{---------- (27)}$$

$$V_{AK.\max} = \frac{V_{in.\max}}{n} + V_o \quad \text{---------- (28)}$$

Where, V_f is the forward voltage of output diode. $V_{in.max}$ =400V

Refer to the maximum duty cycle and minimum input voltage at full load, the transformer inductance can be calculated as:

$$D_{\max} = \frac{n \times (V_o + V_f)}{V_{in.\min} + n \times (V_o + V_f)} \quad \text{---------- (29)}$$

$$L_p = \frac{\eta \times (V_{in.\min} \times D_{\max})^2}{2 \times P_{out} \times f_s \times Br} \quad \text{---------- (30)}$$

Where, Br is how much percentage of the output power will into CCM in low line input voltage. Normally, the Br is set as 30% ~ 50%. $V_{in.min}$=250V

Figure 13 shows the primary current waveform. Once the inductor Lp is determined, the primary peak current I_{pk} and average current I_{av} at the full load and low line input voltage can be expressed as:

$$I_{av} = \frac{P_o}{\eta \times V_{in.\min} \times D_{\max}} \quad \text{---------- (31)}$$

$$\Delta I_p = \frac{V_{in.\min}}{L_p} \times D_{\max} \times T_s \quad \text{---------- (32)}$$

$$I_{pk} = \frac{\Delta I_p}{2} + I_{av} \quad \text{---------- (33)}$$

$$I_{sq} = I_{pk} - \Delta I_p \quad \text{---------- (34)}$$

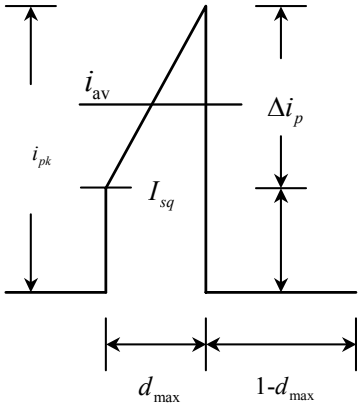


Fig. 13 Primary Current Waveform

From Faraday's law, the turns of primary side can be expressed as:

$$N_p = \frac{L_p \times I_{pk}}{B_{\max} \times A_e} \cdot 10^8 \quad \text{---------- (35)}$$

The turns of auxiliary winding can be expressed as:

$$N_{aux} = \frac{N_p \times (V_{dd} + V_{fa}) \times (1 - D_{\max})}{V_{in.\min} \times D_{\max}} \quad \text{---------- (36)}$$

where, V_{dd} is set to around 12V and V_{fa} is the forward voltage of V_{dd} rectifier diode.

Transformer winding structure

The auxiliary winding of the transformer is developed to provide a power source (VDD voltage) to the control circuit. In order to produce a regulated VDD voltage, the reflected voltage of the auxiliary winding is designed to correlate to the output voltage of secondary winding. However a switching voltage spike caused by the leakage inductance of the primary winding would be coupled to the auxiliary winding to increase the VDD voltage in response to the increase of the load.

When the VDD voltage is increased higher than the voltage of the over-voltage protection 24.5V, the control circuit will turn off the PWM and PFC stage to protect the power supply. Therefore, the transformer windings should prevent the auxiliary winding from primary winding interference.

Figure 14 shows a transformer winding structure, in which primary winding (Np1), copper layer (shield), secondary winding (Ns), auxiliary winding (AUX), copper layer (shield), and primary winding (Np2). Because the auxiliary winding is placed between secondary winding and shield windings, so it can alleviate the variation of VDD voltage and avoid the VDD voltage reach the over-voltage threshold 24.5V for a normal operation.

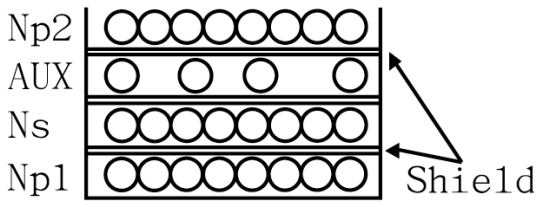


Fig. 14 winding structure

Lab Note

Before rework or solder/desolder on the power supply, it is suggested to discharge primary capacitors by external bleeding resistor. Otherwise the PWM IC may be destroyed by external high voltage during solder/desolder.

This device is sensitive to ESD discharge. To improve production yield, production line should be ESD protected according to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

Printed Circuit Board Layout

Note that SG6902 has two ground pins. Good high-frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate decoupling capacitors near the SG6902. A resistor (5 ~ 20Ω) is recommended connecting in series from the OPFC and OPWM to the gate of the MOSFET.

Isolating the interference between the PFC and PWM stages is also important. Figure15 shows an example of the PCB layout. The *ground trace* connected from the AGND pin of SG6902 to the decoupling capacitor, which should be low impedance and as short as possible. The *ground trace 1* provides a signal ground. It should be connected directly to the decoupling capacitor V_{DD} and/or to the AGND pin of the SG6902. The *ground trace* 2 shows that the AGND pins should connect to the PFC output capacitor C_O independently. The *ground trace 3* is independently tied from the PGND to the PFC output capacitor C_O. The ground in the output capacitor C_O is the major ground reference for power switching. In order to provide a good ground reference and reduce the switching noise of both the PFC and PWM stages, the *ground traces 6 and 7* should be located very near and be low impedance.

The IPFC pin is connected directly to R_S through R_3 to improve noise immunity (Beware that it may incorrectly be connected to the ground trace 2). The IMP and ISENSE pins should also be connected directly via the resistors R_2 and R_P to another terminal of R_S. Due to the *ground trace 4 and 5* is PFC and PWM stages Current loop, which should be as short as possible.

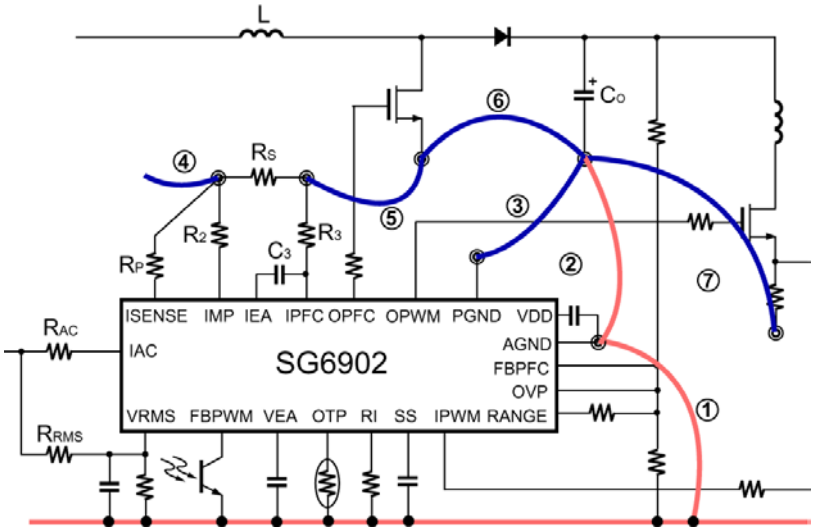


FIG. 15 PCB layout

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