

UC3907 LOAD SHARE IC SIMPLIFIES PARALLEL POWER SUPPLY DESIGN

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INTRODUCTION

Many power supply manufacturers have found it economically feasible to make standard modular power supplies which are easily paralleled for higher current applications. If special provisions are not made to equally distribute the load current among the paralleled supplies, then one or more units will hog the load current leaving the other units essentially idle. This results in greater thermal stresses on specific units and a reduction in the system reliability. For example, reliability predictions will indicate that a component operating at 50 degrees above ambient will have one-sixth the lifetime of the same component operating at 25 degrees above ambient [1].

This paper will examine methods for load sharing presently being implemented discrete/y and then cover Unitrode's single chip solution, the UC3907 Load Share Controller, in several parallel power applications.

SYSTEM REQUIREMENTS

The basic requirements of a power supply system consisting of a number of sources paralleled to increase the total load current are:

- Maintain a regulated output voltage under variations in line or load.
- Control the output current of each supply so they share the total load current equally.

To maximize reliability of the system, there are the following features:

- Achieve redundancy, so that a failure of any one supply can be tolerated as long as there is sufficient current capacity available from the remaining power units.
- Implement a load sharing method without any external control system.

In addition, these are the following desirable features:

- To have a common, low bandwidth share bus interconnecting all power units.
- Achieve good load sharing transient response.
- The ability to margin the system output voltage with one control.

In other words, the combination of power supplies behave like one large supply with equal stress on each of the units. Also, reliability can be optimized by taking advantage of load sharing to incorporate modular redundancy.

LOAD SHARING TECHNIQUES

There are a number of schemes to achieve load sharing. Five approaches are discussed here, with an attempt made to investigate their application, highlighting features and concerns.

THE DROOP METHOD

The simplest method to load sharing is referred to as the droop method. It is an open loop technique which programs the output impedance of the power supplies to obtain load sharing. This method exhibits very poor current sharing at low currents and improves at higher currents, but can still have large current imbalances between supplies. An example of this method is shown in Fig 1 where as the individual supply current increases, the feedback voltage will decrease. This will allow other supplies to distribute more current. The programmed output impedance is given by:

$$R_{out} = 0.01 R_s N$$

The disadvantages to the droop method are: degradation of load regulation, each module must be individually tweaked to achieve good current sharing, and difficulty in current sharing between parallel modules with different power ratings.

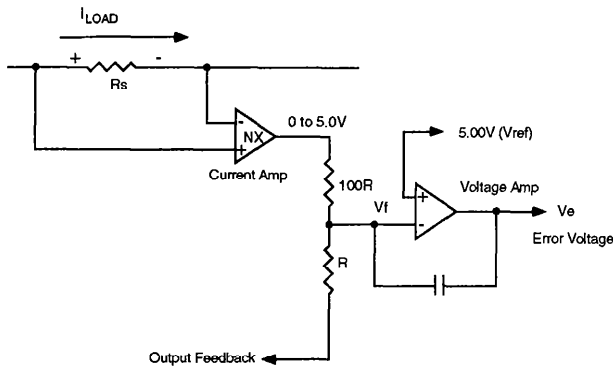


Fig 1 - The Droop method programs the output impedance of the power supplies to achieve load sharing. It is a simple open loop method, but is not accurate.

DEDICATED MASTER

Current mode supplies can accommodate several configurations to achieve a form of load sharing. One approach is to select a master module to perform the voltage control and force the remaining modules (slaves) to act as current sources, as shown in Fig. 2. This technique is facilitated with current mode control, since the error voltage is proportional to load current. If the units were similar in design then a given error voltage on the output of the voltage, or error amplifier will force all units to source the same load current. This technique achieves load sharing but does not achieve redundancy, since if the master fails, the entire system becomes disabled. Another concern with this technique is that the high bandwidth voltage loop is being bussed around the system and is prone to noise pick-up.

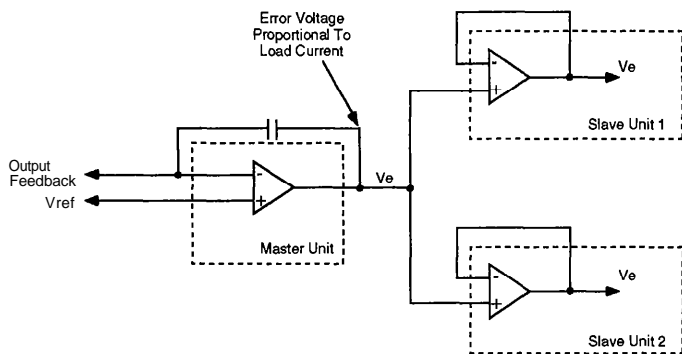


Fig 2 -A dedicated Master approach with current mode supplies will facilitate current sharing but does not achieve redundancy.

EXTERNAL CONTROLLER

Another method is to use an external controller to perform the load sharing. This is achieved by comparing all load sharing signals from the individual power units and adjust the corresponding feedback signal to balance the load currents. This system does perform well but requires an additional controller and multiple connections between the controller and each supply.

AUTOMATIC CURRENT SHARING - AVERAGE CURRENT METHOD

For Automatic current sharing no external controller is required and a single share bus interconnects all the supplies. This requires an adjustment amplifier that compares a current signal from the share bus to the individual units current, and adjusts the reference of the voltage amp until equal load current distribution is achieved.

The average Current method is a patented technique where each power module's current monitor drives a common share bus via a resistor, as shown in Fig 3. The adjust amplifier will sense if there is a differential across the resistor, equating to a load current imbalance, and adjusts the reference accordingly. The node where all resistors connect is a representation of the average load current contribution. While this scheme performs accurate current sharing, it can result in specific application problems. An example is when a supply runs into current limit, causing the share bus to be loaded down and the output voltage to regulate to the lower adjust limit. A similar failure mode will exist if the share bus is shorted or if any unit on the share bus is inoperative.

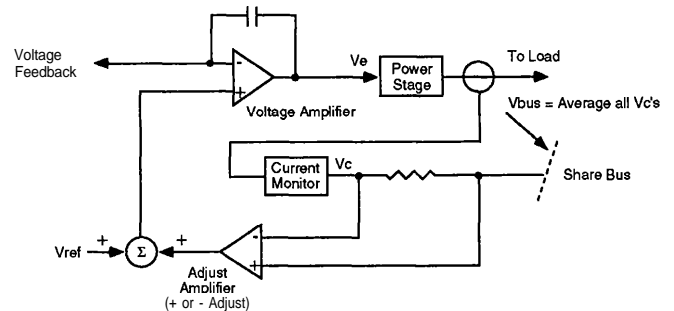


Fig. 3 - The average current method compares the individual load currents to the average load current.

AUTOMATIC CURRENT SHARING - HIGHEST CURRENT METHOD

This technique for automatic current sharing shown in Fig 4 compares the highest current module to each individual current, and adjusts the reference voltage accordingly to correct the imbalance of load current. This technique is similar to the average current method except that the resistor is replaced with a diode, allowing only one unit to communicate on the share bus. This method provides for excellent sharing among the slaves with an error in the master's load current contribution because of the diode.

The UC3907 Load Share Regulator has improved on this method by replacing the diode with a unidirectional buffer to reduce the master's error. An inoperative or insufficient capacity supply will not effect the sharing of the operational units. A shorted share bus will disable the reference adjustment section used for load sharing, making the units operate as stand alone.

THE VOLTAGE LOOP

THE VOLTAGE AMP

This Amplifier is the feedback control gain stage for the power modules output voltage regulation, and the overall voltage loop compensation will normally be applied around this amplifier. The output swing is limited to 2 Volts to improve the large signal response of the system. The voltage amplifier accomplishes the high impedance positive sensing, and the ground amp, the high impedance negative sensing.

THE GROUND AMP

This amplifier is a unity gain buffer with a 0.250V offset. The offset allows the amplifier negative headroom to return all control bias and operating currents while maintaining a high impedance negative sense input (pin 4) where this input is referred to as "true" ground. The output of this amplifier is referred to as Artificial Ground. The 0.250V offset is

added to the 1.750V bandgap reference to obtain the 2.00V reference, as seen by the voltage amp, and is trimmed to +/-1.25%.

The ground return (pin 5) should be the most negative voltage available and can range from zero to 5V below the negative sense input. All the IC's current will return through the ground return pin.

THE DRIVE AMP

This amplifier is an inverting amplifier with a gain of -2.5, which couples the feedback signal to the power controller. The Current setting resistor Rset helps to establish the forward transfer function of the control loop and the maximum drive current. The polarity of the drive amp stage is such that an increasing voltage at the plus sense input (pin 11) will increase the opto-couplers current, thereby reducing the primary side PWM's duty cycle. This will insure proper startup since there is no energy on the secondary side during initialization of the power system.

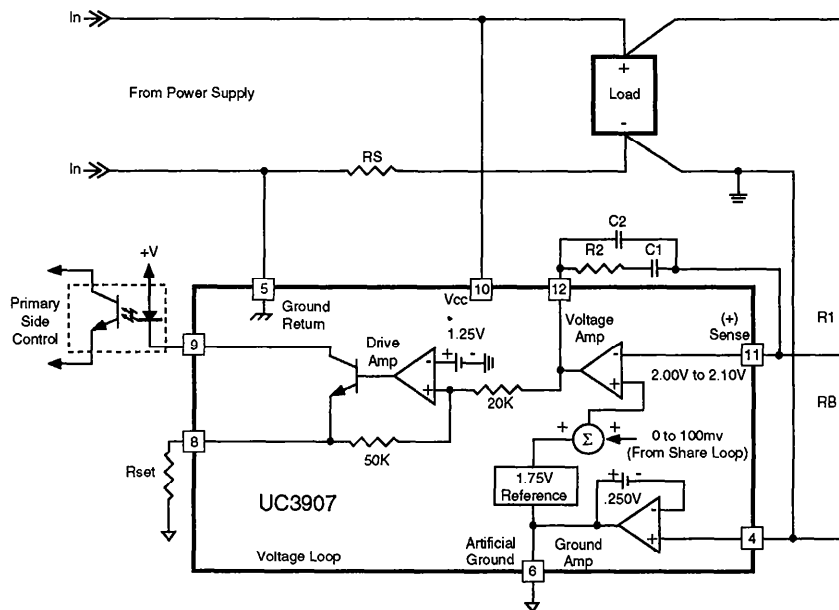


Fig. 7 - The UC3907 Voltage Loop achieves high impedance differential sensing along with optical coupler driving capability.

THE CURRENT LOOP

THE CURRENT AMP AND BUFFER AMP

The current sharing portion of the IC utilizes the current amp, the buffer amp, and the adjust amp as shown in Fig. 8. The Output of the current amp is an analog representation of individual load current, where the output voltage is given by: $V_{ca} = 20 \cdot R_s \cdot I_{out}$. The current amp output feeds an input of a unidirectional buffer which drives the current share bus. Since the buffer amp only sources current, it insures that the module with the highest load current will be the master, or communicator to all other modules, and drives the bus through a low-impedance. All other buffer

amplifiers will be inactive with each exhibiting a 10K ohm load impedance to ground.

THE ADJUST AMP

The adjust amplifier will compare its own load current with that of the highest current module, and force a command to adjust the individual modules reference voltage, (as seen by the voltage amp) to maintain equal current sharing. It is a transconductance type amplifier in order that its bandwidth may be limited, and noise kept out of the reference adjust circuitry, with a simple capacitor to artificial ground. The ground referenced compensation will act similar to that of integral compensation, but without the non-inverting signal feedthrough problems, thereby filtering both inputs from

unwanted noise. The adjust amplifier has a built in 50 millivolt offset on its inverting input, which forces the unit acting as a master to have a low output resulting in a zero adjust command. While the 50mv offset represents an error in current sharing, the gain of the current amplifier reduces it to 2.5 millivolts across the sense resistor. This results in all slave modules sharing equally and the master module running a few percent higher. The offset also provides some immunity from cycling, or fighting for master position due to low frequency noise.

STATUS INDICATE

The status indicate pin is designed to indicate which unit is acting as the master. Its open collector output is activated when the adjust amp output is in the low state. In a case of an overcurrent fault with one of the many paralleled units, this pin will indicate the unit with the highest current which will help diagnose the faulted module. A zero current or low current fault is transparent to the other supplies' and has no effect on voltage regulation and current sharing.

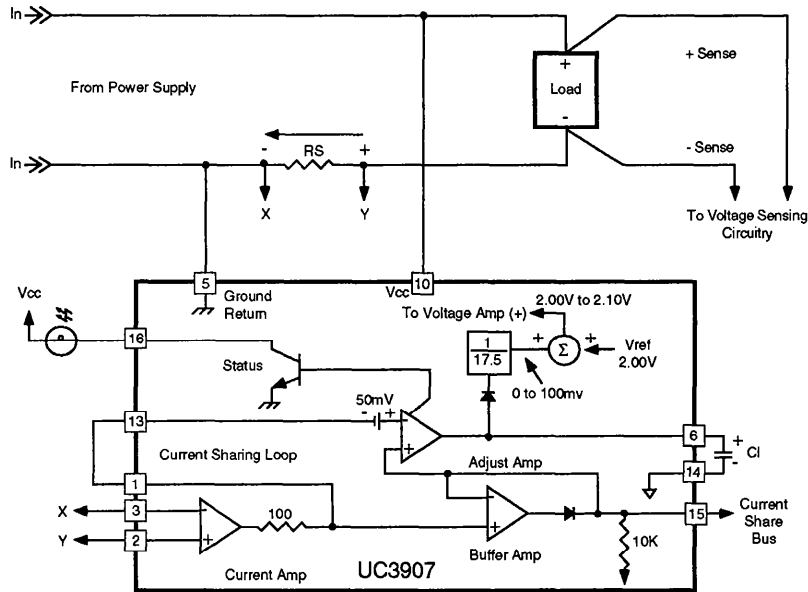


Fig. 8 - Current sharing is achieved with the UC3907 by comparing the individual module's current to that of the highest current module. The necessary adjust command increases the voltage amp reference to accomplish equal load sharing.

START-UP FOR A PARALLEL POWER SYSTEM

Start-up conditions need to be considered in a parallel power supply architecture. A start-up timing example of four 5V power modules in parallel is shown in Fig. 9. Once the primary power is applied, the power stage will be requesting maximum duty cycle until the individual units feed back a signal to regulate the output voltage. At time t1, supply #1 has become the master due to its higher reference voltage. This forces the output voltage to regulate above the other units. The other units will feedback a zero duty cycle signal to the power stage and remain idle. At this point the master unit is supplying all the supply current, and outputting the corresponding current signal on the share bus. The other units' adjust amplifiers sense the difference between their individual load currents and the master's, and start to slew up the adjust amp output to increase their references. At the same time the master's adjust amplifier output remains clamped below the adjust threshold having no effect on its original reference. At time t2 the other three adjust amps have exceeded the adjust threshold and have started to effect the reference as seen by the voltage amp.

At time t3 the unit with the closest reference to the master, supply #2, has reached the point where its references is essentially equal to the master's and the load current becomes equally distributed between the two. The other two modules, #3 and #4, are still adjusting their references and are not yet contributing to the load current. At time t4 the 3rd unit has reached the desired reference and the load current has been equally split between the three, and at time t5 the final unit has completed its reference adjustment, thereby completing the load sharing. If it is necessary to have the units come up sharing, then a soft-start scheme will need to be implemented on the primary side modulator which needs to be much slower than the adjust time. The total adjust time from t1 to t5 for this example is given by:

$$t = \frac{C1 Va}{I}$$

where C1 = adjust amp compensation
 Va = adjust amp swing
 I = Adjust amp max current - 220ua

APPLICATION NOTE

CI is chosen from the desired bandwidth

$$C_I = \frac{g_m}{2\pi F}$$

where $g_m = 3\text{mS}$ and $F = \text{Adjust amp bandwidth}$.

If the required adjust amp bandwidth were 500 Hz, then C_I will be 1 μF . The adjust amp output for the lowest reference will adjust to a voltage calculated as follows:

$$V_{adj} = (V_{REF_{max}} - V_{REF_{min}}) 17.5 + 1$$

$$= (30\text{mv} \cdot 17.5) + 1 = 1.53$$

The adjust amp must slew from approximately 0.7V to 1.53V at a slew rate of 220mV/ms which equates to a complete sharing delay time of 3.8 ms.

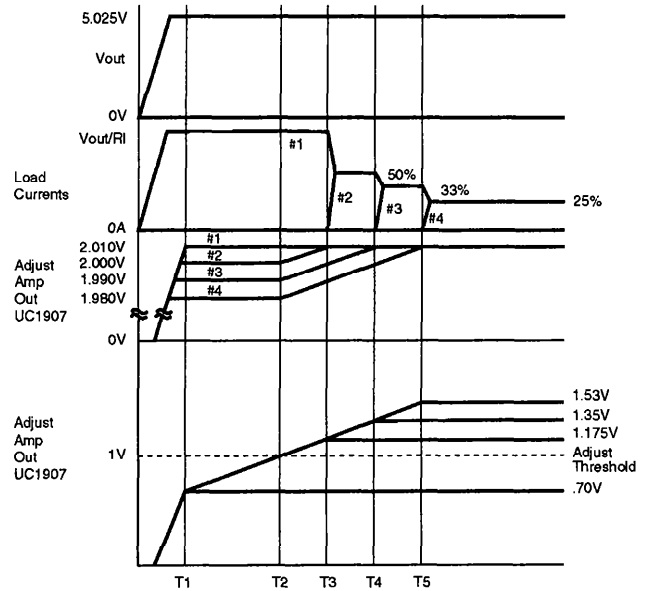


Fig. 9 - Start-up timing of a four module power system using the UC3907 (without soft-start).

THE VOLTAGE AND SHARE LOOP DESIGN

A load sharing system is composed of two loops, the voltage loop and the current share loop. As in conventional designs, the voltage loop regulates the output voltage and is the faster responding loop. The current sharing loop is a lower bandwidth loop to eliminate noise pick-up on the share line, and should be low enough in bandwidth to eliminate interactions with the voltage loop.

A complete loop diagram is shown in Fig. 10. The voltage amp transfer function is designed to optimize the voltage loop response, which is determined by the modulator topology, filters, and other gain functions in the loop. We will work through each gain block for a flyback converter example using the UC3907, and from this the user should be able to expand the design to any topology.

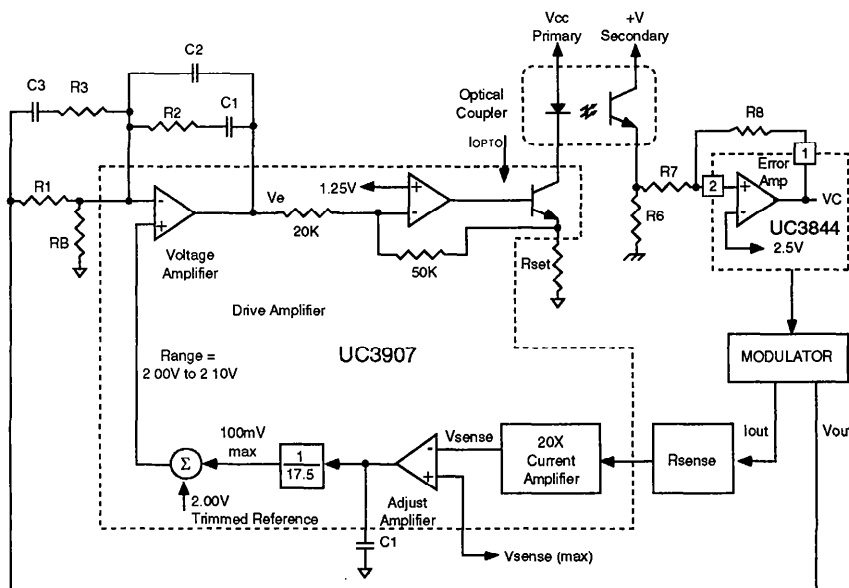


Fig. 10 - The UC3907 can be easily implemented to perform voltage control, and optical coupler drive for isolated applications.

Compensated as shown, the voltage amp response is given by:

$$UGF = \frac{1}{2\pi R_1(C_1 + C_2)} \quad \text{Pole} = \text{Origin}$$

UGF = Unity Gain Frequency.

$$\text{Pole 2} = \frac{1}{2\pi R_1 C_3} \quad \text{Pole 3} = \frac{1}{2\pi R_2 \left(\frac{C_1 C_2}{C_1 + C_2} \right)}$$

$$\text{Zero 1} = \frac{1}{2\pi R_2 C_1} \quad \text{Zero 2} = \frac{1}{2\pi (R_1 + R_3) C_3}$$

The drive amp will convert the output of the voltage amp to an error current to be applied to the opto coupler. The current is given by:

$$I_{\text{opto}} = \frac{(1.25 - V_e)2.5 + 1.25}{R_{\text{set}}}$$

where V_e = output of the voltage amp - error voltage and the small signal gain is:

$$\frac{I_{\text{opto}}}{v_e} = \frac{-2.5}{R_{\text{set}}}$$

The control voltage for the UC3844 pulse width modulator is given by:

$$V_c = (2.5 - I_{\text{opto}} \text{CTR} R_6) \left(\frac{R_8}{R_6 + R_7} \right) + 2.5$$

where CTR is the current transfer ratio of the opto coupler. and the small signal gain is given by:

$$\frac{v_c}{I_{\text{opto}}} = -\text{CTR} R_6 \left(\frac{R_8}{R_6 + R_7} \right)$$

therefore the UC3907 error voltage to PWM control voltage gain is given by:

$$\frac{v_c}{v_e} = \text{CTR} R_6 \left(\frac{R_8}{R_6 + R_7} \right) \left(\frac{2.5}{R_{\text{set}}} \right)$$

The CTR spread can vary from 0.4 to 2 on a given device type, but many manufacturers can sort them out to a +/- 30% tolerance. The CTR is also a function of the driving current and therefore introduces a non-linearity in the feedback gain.

The control to output gain of the modulator for various topologies is referenced in the Unitrode power supply design seminar book. For example, the control to output gain for the discontinuous flyback with current mode control is:

$$\frac{v_o}{v_c} = \sqrt{\frac{R_o L F}{2}} \frac{\left(1 + \frac{s}{wz} \right)}{\left(1 + \frac{s}{wp} \right)}$$

$$\text{Where } wz = \frac{1}{R_c C} \quad wp = \frac{1}{R_o C}$$

R_c = esr of C's in parallel
 R_o = Load resistance
 C = Total output Capacitance
 L = Primary inductance
 F = Switching frequency

The total voltage loop gain is given by:

$$G(S) = A(s) \left(\frac{v_c}{v_e} \right) \left(\frac{v_o}{v_c} \right)$$

where $A(s)$ is the voltage amp transfer function

To bandwidth limit the share loop, the adjust amplifier is compensated where the unity gain frequency of the adjust amp is given by :

$$F = \frac{gm}{2\pi C_1}$$

where typical $gm = 3mS$.

AN OFF-LINE LOAD SHARE APPLICATION

An off-line power supply application utilizing the UC3907 Load Share Controller is shown in Fig. 11 for a flyback regulator. The UC3844 is the modulator and its switching frequency is determined by $F_s = 1.72/(R_t C_t)$. The resistor R_5 will sense the primary inductor current, where the maximum peak current for the UC3844 is given by $I_{Smax} = 1.0V/R_5$. Startup is achieved with R_1 and C_5 until bootstrap winding W_2 can feedback to power the UC3844. The snubber network D_3 , C_4 , and R_2 prevents turn-off voltage spikes from exceeding the FET breakdown voltage. The primary soft-start circuit is comprised of Q_1 , R_9 and C_{10} .

Note that the resistor Rset and adjust compensation is connected to artificial ground (pin 6). Artificial ground is a replica of the "true" ground voltage on pin 4, negative sense, plus a 0.250V level shift. This allows a low impedance point for ground referenced elements to connect.

A master indicator lamp is included in the design so that the unit supplying the most load current and determining the output regulating voltage can be detected. There are many useful applications for this pin as in supply voltage margining or determination of a faulted supply which is supplying an excess voltage/current.

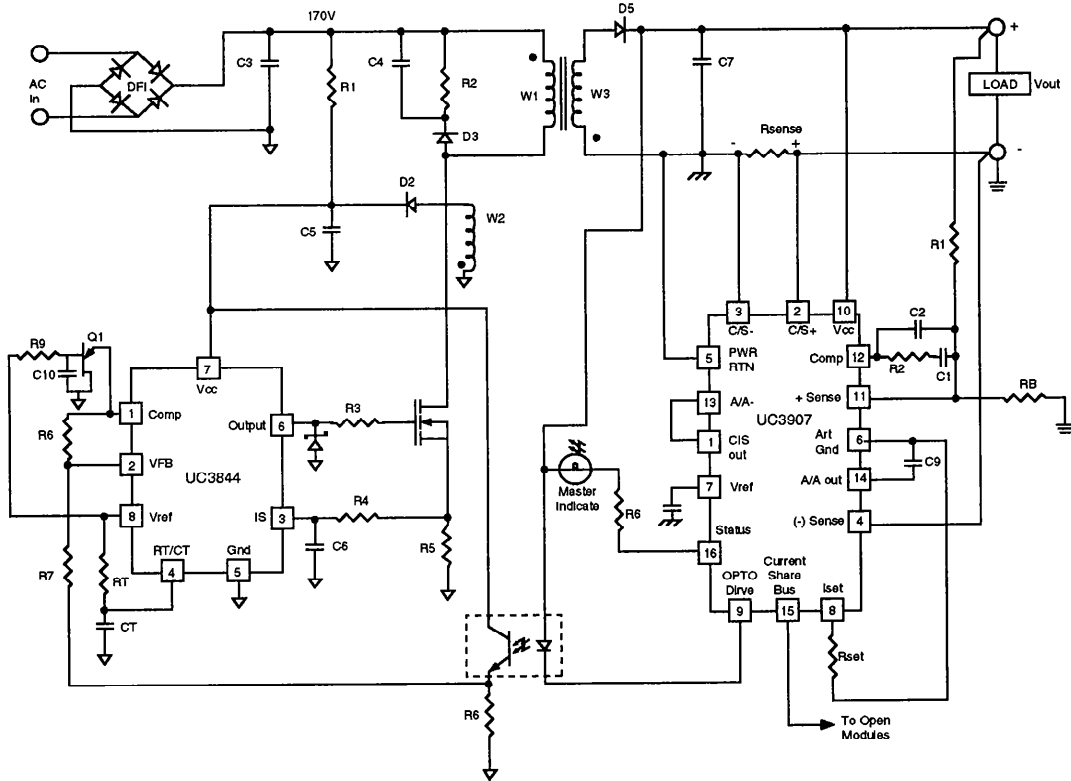


Fig. 11- The UC3907 in an off-line isolated application.

NON-ISOLATED CONVERTER APPLICATIONS

There are applications where non-isolated DC to DC converters are paralleled to make a power system. Fig. 12 shows a step down, or buck, regulator utilizing the UC3524A voltage mode PWM and the UC3907 Load share IC. For non-isolated parallel power supply applications the current sensing must be done on the high side. The reason for this is that if the sensing was performed on the low side where the power supply inputs and outputs are common, then all the current sense resistors will end up in parallel, defeating the individual sensing and load sharing. The only limitation to high side current sensing in a non-isolated application is that the current amplifier of the UC3907 has a common mode range of 0V to Vin -2V, therefore a form of level shifting or average current sensing would be required.

Since the opto-coupler is not required, an inversion has been eliminated which the driving scheme must accommodate for. The Iset voltage is a gained up inverted error voltage from the UC3907 voltage amp. The UC3524A error amp is set up as an inverter and cancels out the drive amp inversion leaving the error voltage of the UC3907 to be transposed to the UC3524A in proper phase. The Iset voltage will swing from 0v to 3.8V min. Current limiting is achieved by taking the current amp output signal from the UC3907 and feeding it in to the UC3524A current limit amplifier, where the current limit is given by:

$$I_{cl} = \frac{5 \left(\frac{R_{12}}{R_{11} + R_{12}} \right) + 0.2}{20 R_{sense}}$$

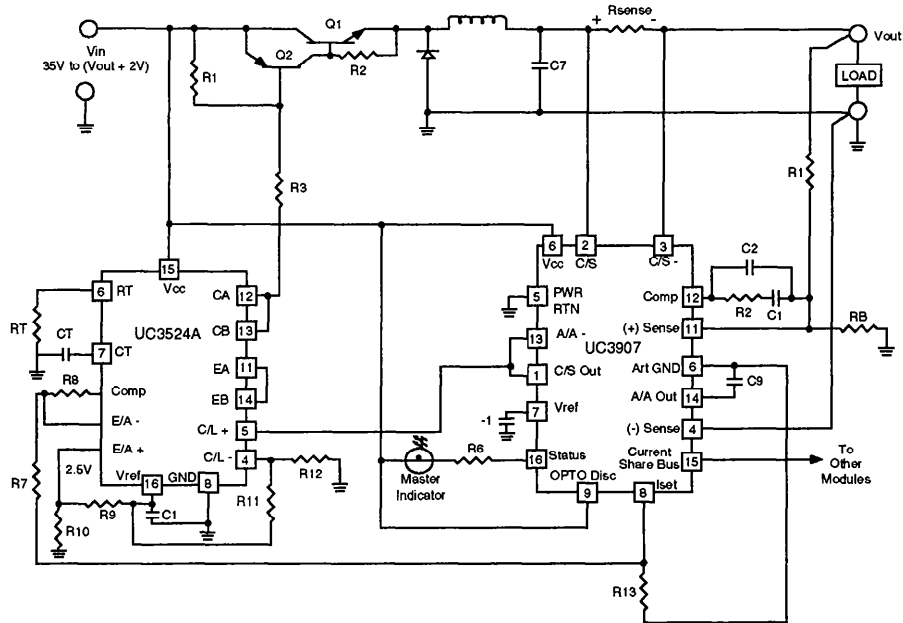


Fig. 12 - The UC3907 in a non-isolated DC to DC converter application.

LINEAR REGULATOR EXAMPLE

A simple linear regulator with load sharing using the UC3907 IC and a few external components is shown in Fig. 13. The phasing of the opto drive pin facilitates darlington drive, and supply current limiting is achieved by Q3, C1, R11, and R12 with the current limit given by:

$$I_{cl} = \frac{V_{BEQ3} \left(1 + \frac{R_{11}}{R_{12}} \right)}{20 R_{sense}}$$

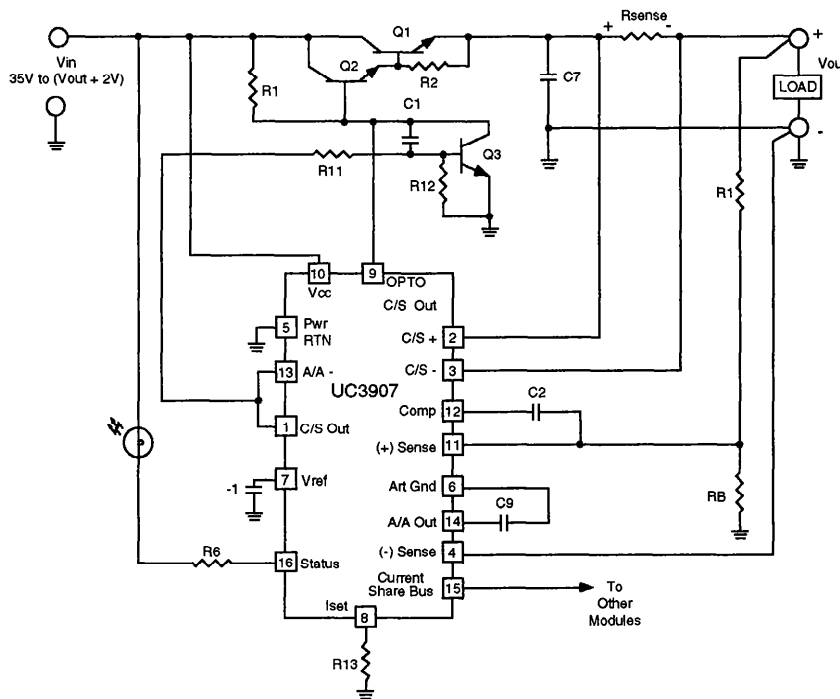


Fig. 13 - With a few external components the UC3907 can make a simple linear regulator with load sharing.

EXTERNAL LOAD SHARING

The UC3907 can be easily incorporated outside the power module to achieve load sharing, as shown in Fig 14. The load sharing loop is similar to previous examples, but instead of adjusting the internal reference of the UC3907, this technique adjusts the (+) sense line of the power module to

force equal current sharing. The maximum adjust voltage is given by:

$$V_{adj_{max}} = 1.75 \left(\frac{R_1}{R_2} \right)$$

LOAD SHARING CAN BE EXTERNALLY ADDED TO EXISTING POWER MODULES

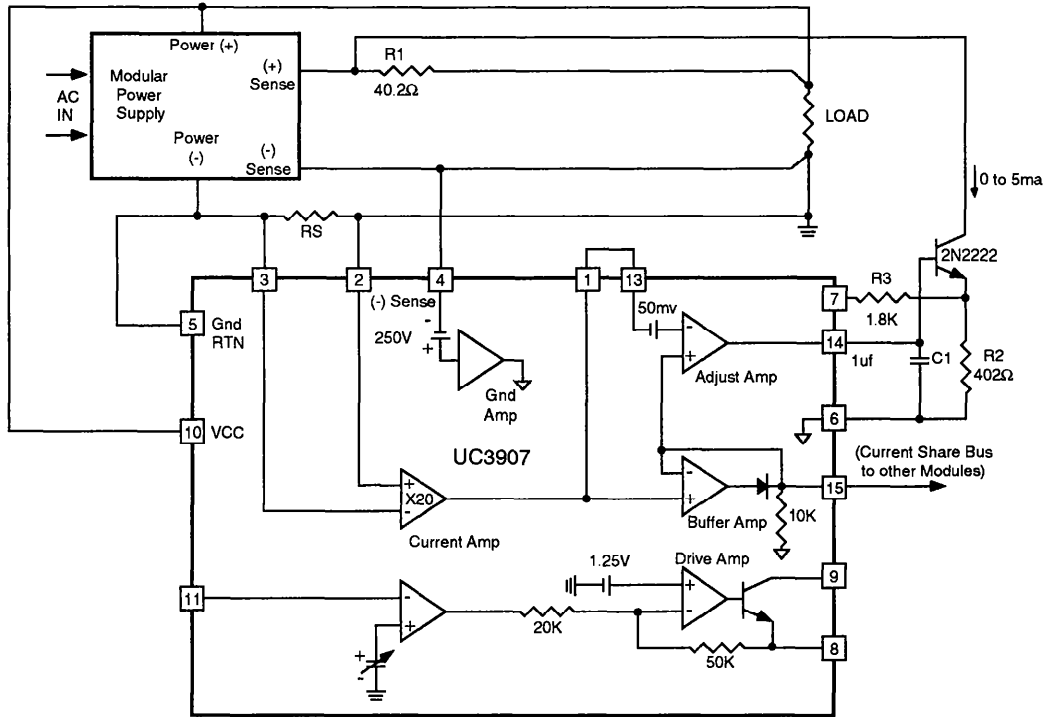


Fig. 14 - The power supplies remote sense inputs are used to facilitate load sharing.

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