AnaPass

fast Mobile Serial Link™

AnaPass, Inc.

Jan. 2006

anapass

AnaPass, Inc.

❑ Company Profile

– **AnaPass, Inc.** is a fabless semiconductor company founded in 2003, which designs, develops, and markets cost-effective and innovative mixed-mode IC and IP solutions focused on **high-speed serial link technology specialized in display and handset market.**

– **Employees**

- Totally 29, including 18 engineers, all who hold MS/Ph.D degree from Seoul National University, and have a work-experience at Samsung, LG, Hynix.

– **Technology:**

- Since the middle of 1990s, AnaPass has developed state of the art **Serial Link Technology**. Based on a prior experience, AnaPass has introduced innovative **LVDS/TCON** solutions for large flat panel display applications, and **Mobile Serial Link** solutions for mobile handset applications. Also, AnaPass has developed various **LCD Driver/Controller** solutions for mobile display applications.

Business Area/Product Portfolio

ANA3XXX
LVDS/TCON
for Flat Panel Display of LCD Monitor, LCD TV, Notebook

- **ANA30XX** LVDS Core AiPi Core
- **ANA33XX/34XX** LVDS Tx/Rx
- **ANA35XX~38XX** TCON for FPD

ANA5XXX
Mobile Serial Link
for Multimedia Mobile Application

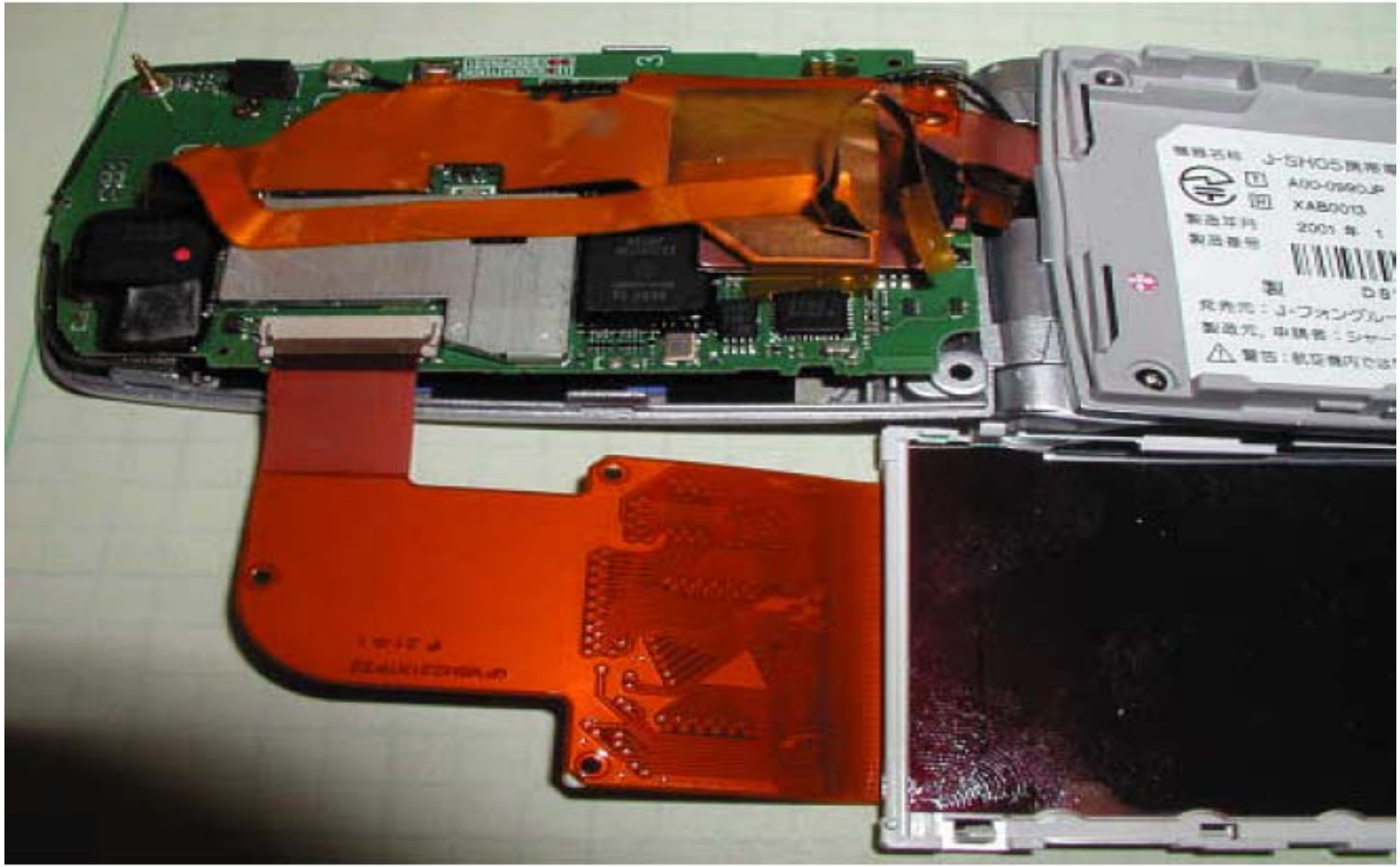
- **ANA50XX** *f*-MSL Core
- **ANA5XXX** *f*-MSL Tx/Rx for Multimedia Mobile Application

ANA6XXX
LCD Driver/Controller
for TFT-LCD Display Panel

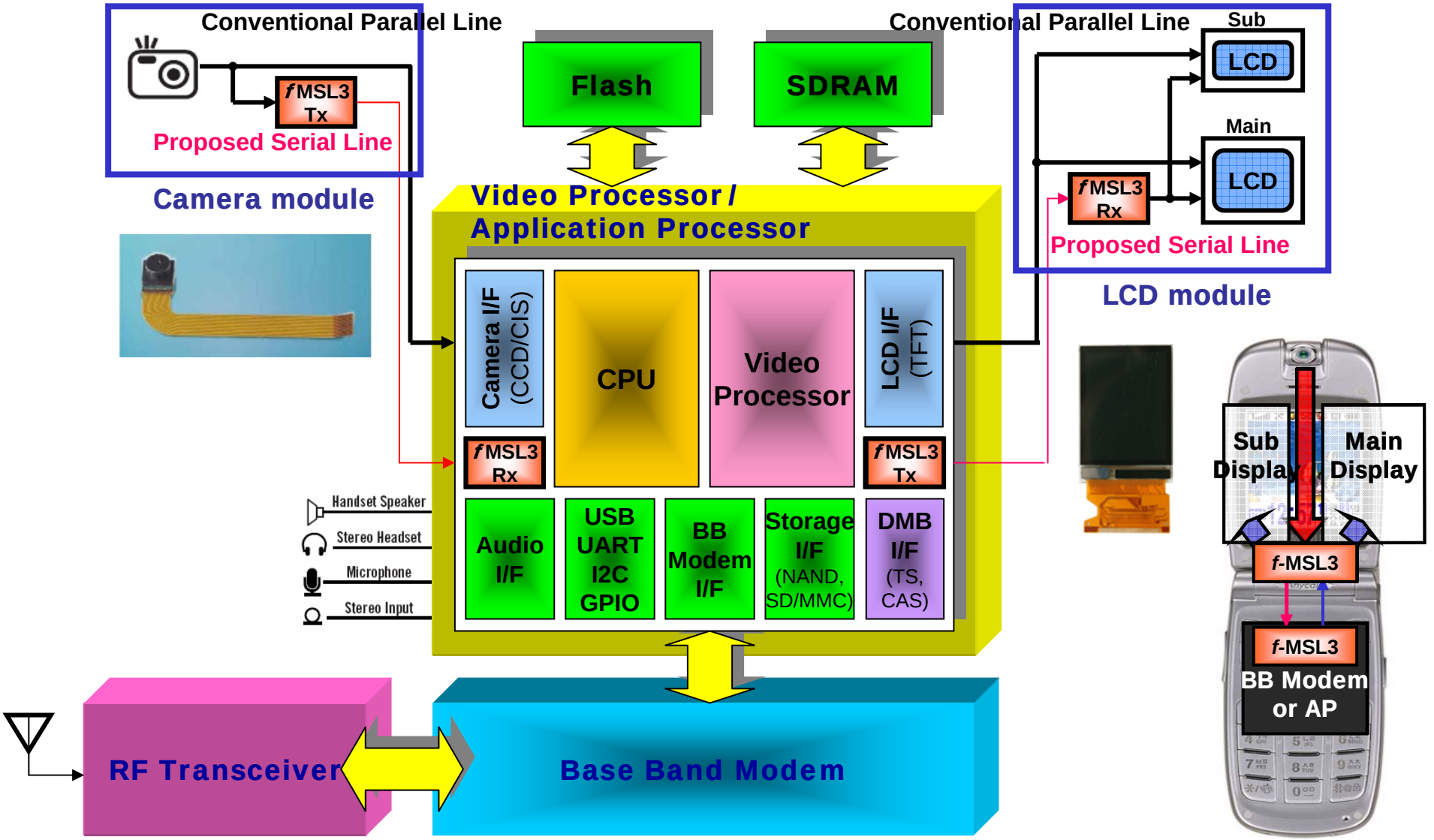
- **ANA62XX** LDI w/ *f*-MSL for Mobile Display

❑ *f*-MSL for Mobile Applications

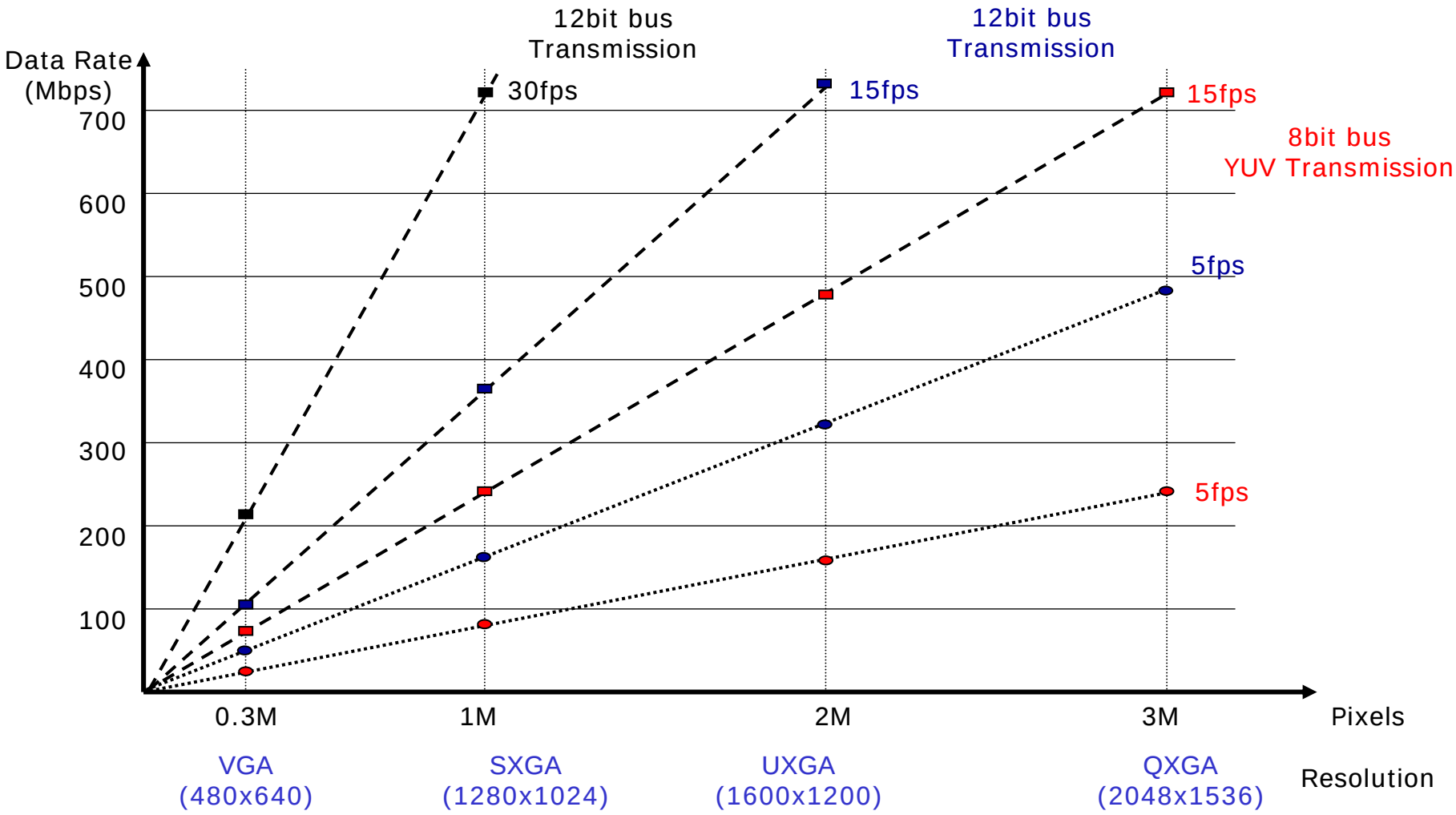
Multimedia Mobile Handset Application



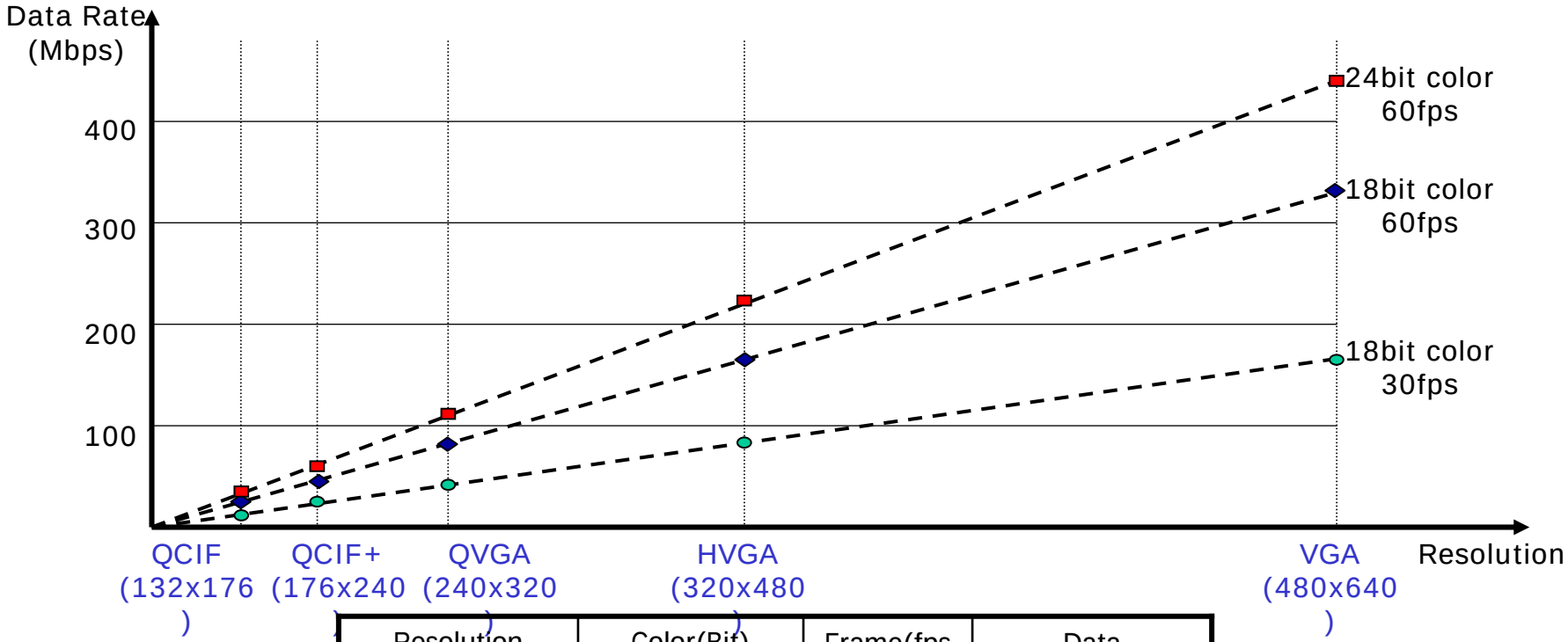
Serial Link for Mobile Handset Application



Camera Data Transmission Rate



LCD Image Data Transmission Rate

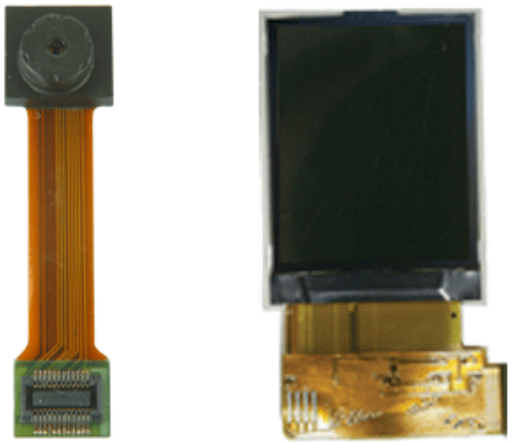


Resolution	Color(Bit)	Frame(fps)	Data Rate(Mbps)
QCIF(132X176)	16	30	**11.2**
QCIF+(176X240)	16	30	**20.3**
QVGA(240X320)	18	30	**41.5**
HVGA(320X480)	18	30	**83.0**
VGA(480X640)	18	30	**165.9**
VGA(480X640)	18	60	**331.8**
VGA(480X640)	24	60	**442.4**

Advantage of Serial Link for Mobile Apps.

❑ The necessity of Serial Link interface

- Higher LCD Resolution/Larger Camera Image
  - Image Data Size Increase
- Faster Data Rate required
  - Wider bus (PCB size, FPC size, Connector, Wiring of hinge)
  - Difficulty in mechanical design, Stress of FPC
  - Higher cost of FPC, Connector & Camera/LCD Module
- EMI, Power Consumption Increase
  - Degradation of RF Performance
  - High drivability I/O required
  - Limit of lower operation voltage



❑ The main benefits of Serial Link interface

- High-speed data transmission
- Reduced data transmission lines, Simple interface
  - Lower Gate count, PCB size, FPC size, Connector
  - Flexible Design
- Low voltage swing
  - Lower power consumption
  - Lower EMI noise
- Total BOM Reduction

→ High speed serial link will be indispensable and mandatory !!!

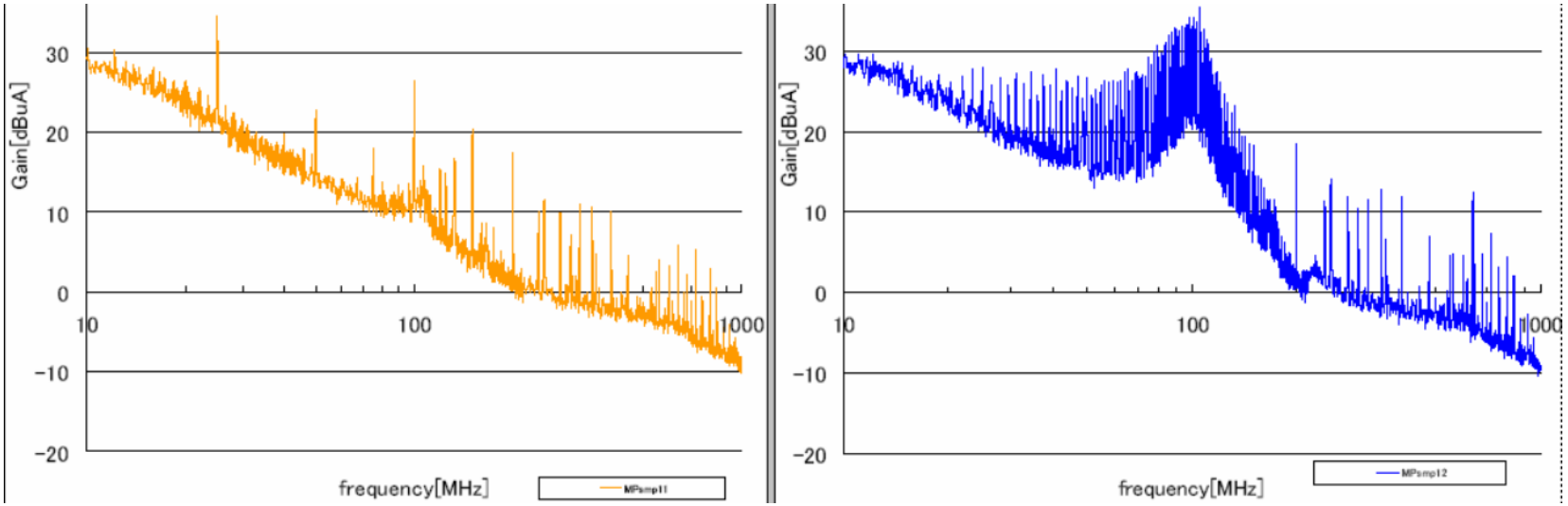
Advantage of Serial Link for Mobile Apps.

❑ Less number of wiring

Interface	Legacy Interface Active Signals	*f*- MSL Active Signals (2 differential pairs)	Savings Ratio
YUV 8-bit Camera	12	4	3 : 1
RGB 18-bit display	21	4	5.3: 1
RGB 24-bit display	28	4	7 : 1
16-bit CPU	22	4	5.5 : 1

❑ Lower EMI Noise

– **Serial Link Interface** **vs.** **CMOS Interface**



Mobile Serial Link Comparison (I)

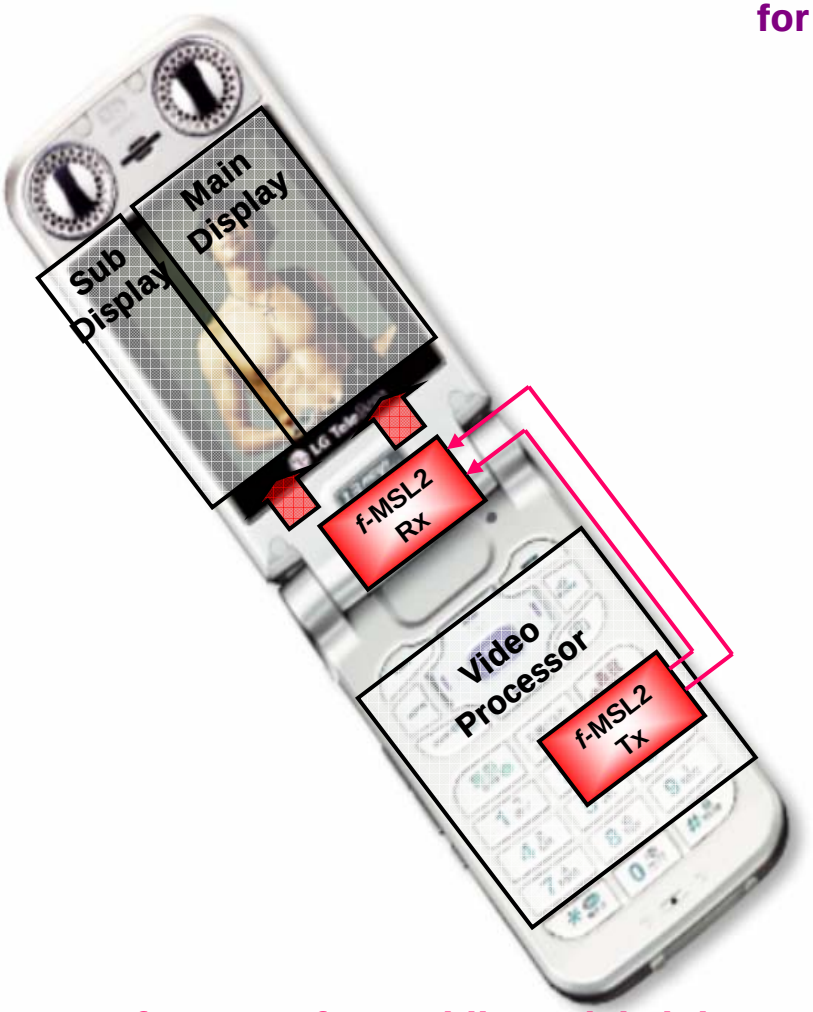
	Product / Scheme / Applications		Throughput per channel	Total Throughput	Power	Etc
MIPI /SMIA Standard	**CSI ver1.0**: Camera Serial Interface 2kinds/2chips for Tx, Rx	**Sub LVDS**, 1way 1 data: 8bit, V/H SYNC 1 clock: ~208MHz	**208Mbps/ch**	**208Mbps /w 1ch**	**DC: 3~4mA** AC: 2.5~3.5uA/MHz Supply: 1.4~1.95V Logic: 1.0~1.95V	Mar/'04
	CSI ver2.0: Camera Serial Interface	On-going	**670Mbps/ch**	**670Mbps /w 1ch**		
	DSI ver1.0,2.0: Display Serial Interface	On-going	TBD	TBD		
VESA Standard	**MDDI** :LVDS-like, Differential 2kinds/2chips for Host, Client	Data: Bi-directional Strobe: Host to Client Types I/II/III/IV: 1 Strobe pair plus 1/2/4/8 data pairs	**400Mbps/ch**	**TI:400Mbps/1ch** **TII:800Mbps/2ch** **TIII:1.6Gbps/4ch** **TIV:3.2Gbps/8ch**		Serial interface between MSM6150, 6550, 7XXX
Samsung MC	**MC4**: Media coprocessor, LCD Ctrl for QVGA/QCIF, /w Frame buffer (230KB), 16bit GPIO, 32bit AMBA, 4ch PWM, SPI	**Type-1 MDDI** Display Client Serial interface Half-Duplex /w Differential & Bi-directional 1 data: 18bit 1 strobe: Host to Client	**150Mbps/ch** 50MHz(AHB bus)	**150Mbps /w 1ch**	Internal: 1.40~1.60V External: 2.70~3.00V 5 PD_mode: Gated clock	0.13um LP Process, MP @ 4Q/'04 100-pin FBGA (8mmX8mm), 96-pin COF (4.24mm X 4.14mm)
NEC MCMADS	**uPD161451**: LCD (RGB I/F mode) Interface, Bridge IC **uPD161832/33**: Low Temperature p-Si TFT LCD Driver IC	**Current Mode Differential Signaling** Half-Duplex /w Differential & uni-directional 1 data: 16/18bit 1 clock: ~62.5MHz	**125Mbps/ch**	**125Mbps /w 1ch** **250Mbps /w 2ch**	**DC: 1.2mA @60Mbps** Internal: 1.5V interface: 1.85V	62.5 MHz Max (4mmX4mm),

Mobile Serial Link Comparison (II)

	Product / Scheme / Applications		Throughput per channel/ Total	Power	Etc
NS MPL	**LM2501**: Camera 1kind/2chips configurable as a Serializer or Deserializer	**Current-mode/Single ended, Unidirectional**, Half duplex 1 data: 8bit, V/H SYNC 1 clock for PCLK (4~16MHz) 1 WCLK (4~28MHz)	**160Mbps/ch** **160Mbps /w 1ch**	**650uA/ch** **PD-mode: ~10uA** Supply: 1.7~3.1V & 2.9~3.1V Logic: 1.8~3.0V	3.5mm X 4.5mm X 0.6mm 24-Lead Ultra Thin CSP
	LM2502: LCD Display 1kind/2chips pin selectable as a Master or Slave	**Current-mode/Single ended, Bi-directional**, Half duplex 2 data: 16bit, CPU mode 1 clock: PCLK	**160Mbps/ch** **320Mbps /w 2ch**	**650uA/ch** **PD-mode: ~10uA** Supply: 1.7~3.3V & 2.9~3.3V Logic: 2.9~3.3V	4.0mm X 4.0mm X 1.0mm, 0.5mm pitch 49(40) Lead FBGA style
Fairchild µSerDes	FIN12A(C):12bit SerDes FIN22A(C) 22bit SerDes FIN24(C):24bit SerDes	LpLVDS/CTL 1 data 1 clock	Data: 780MB/s	typical operating conditions: 5mA Standby mode: 100nA	3.5mm X 3.5mm BGA 6mm X 6mm MLP
Rohm MSDL	**BU7280GLU**: 1kind/2chips configurable as a Serializer or Deserializer	**Current-mode/Differential**, Bi-directional, Half duplex 2 data 1 clock: ~10MHz	**1st: 100Mbps/ch** 2nd: 200Mbps/ch **1st: 200Mbps /w 2ch** 2nd: 200Mbps /w 1ch	**IO: 2mA, Core:5mA @ 6MHz** **PD-mode: ~10uA** H-sink: 600uA, V-sink:250uA Supply: 1.70~2.05V Logic: 2.55~3.15V	5.0mm X 5.0mm X 1.0mm, 0.5mm pitch VBGA063T050
Seiko-Epson/ Renesas MVI	1kind/2chips Full duplex SERDES for Camera/Display	**Sub LVDS**, Full-/Half- duplex 1f-data,1clock : ~200MHz 1 r-data,1 strobe clock	**1st: 200Mbps/ch** 2nd: 400Mbps/ch **1st: 400Mbps /w 2ch** 2nd: 800Mbps /w 4ch	**1.4mA/ch (2.85V)** H-sink: 500uA V-sink:100uA	
Anapass *f*-MSL	**ANA5321/5331**: LCD Display Interface 2kind/2chips for Tx or Rx	**Sub LVDS**, Unidirectional, 1 data: 16/18/24bit 1 clock: ~800MHz I2C for CPU mode	**800Mbps/ch** **800Mbps/w 1ch**	**1.0mA/ch** **PD-mode: ~10uA** UMC 0.25um, 2.5V	Wide bandwidth, Ultra fast mode, Low Power, Low EMI, Slim Architecture
	ANA5521: Camera/LCD Display 1kind/2chips for SERDES configurable	**Sub LVDS**, Full-/Half- duplex 1f-data,1clock : ~800MHz 1 r-data,1 strobe clock			

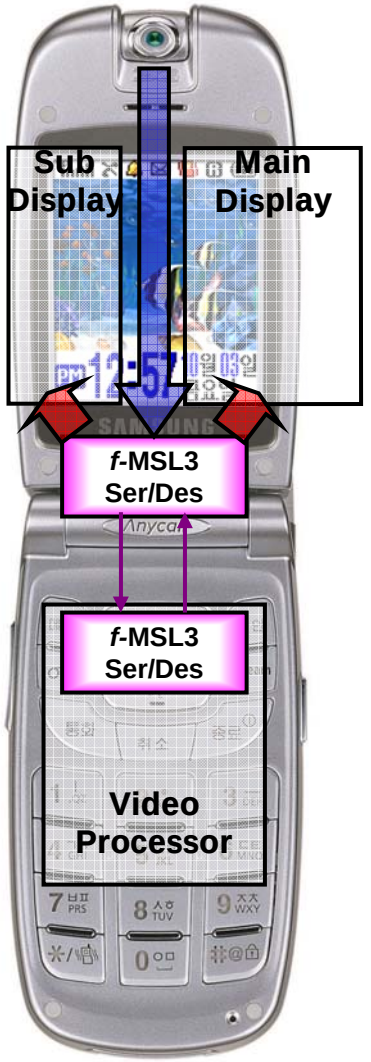
AnaPass *fast* Mobile Serial Link (*f*-MSL)

***f*-MSL1 : *fast* Mobile Serial Link for Camera Module**



***f*-MSL2 : *fast* Mobile Serial Link for LCD Module**

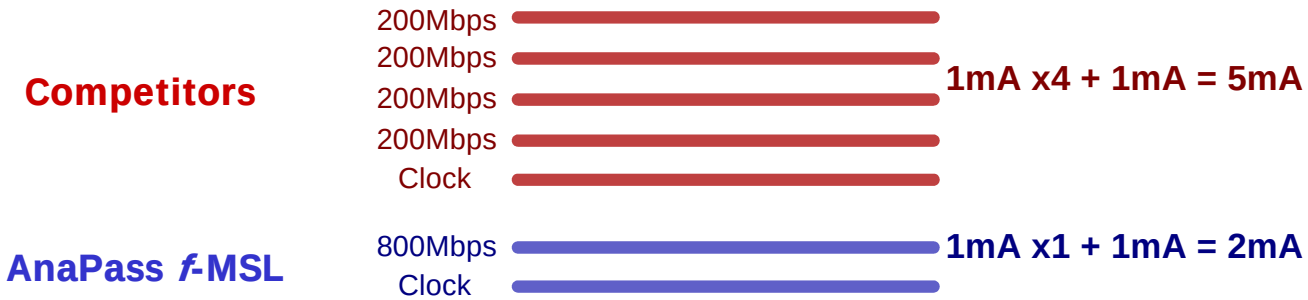
***f*-MSL3 : *fast* Mobile Serial Link for Camera/LCD Module**



AnaPass *fast* Mobile Serial Link(*f*-MSL)

❑ Features

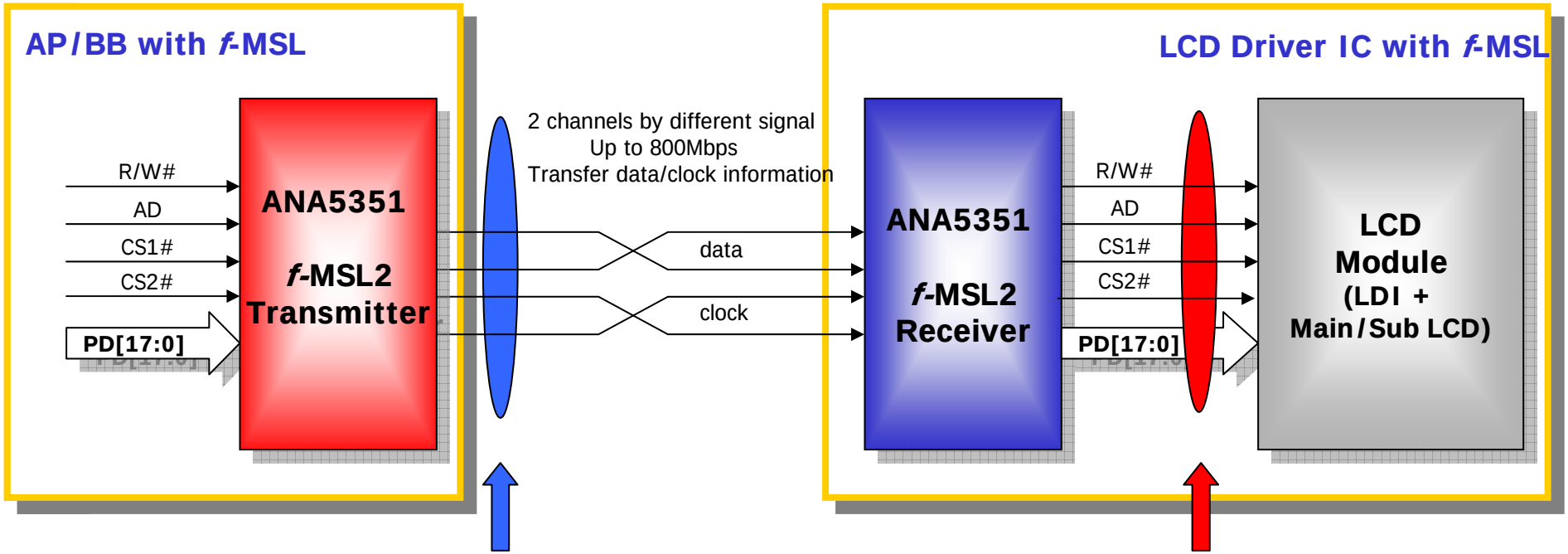
- **Ultra fast mode Operation(Wide-bandwidth/High-speed)**
  - Up to 800Mbps with single channel
- **Sub-LVDS type, Full/Half Duplex, 2 channels**
  - 4 lanes = 2 lanes for Data + 2 lanes for Clock
  - Master/Slave Selectable
  - 50~100mV Swing, 2.5V/3.3V, 0.25um Process
- **Lower Power, Lower EMI noise**
  - Multi lanes for speed-up will multiply the link power by # of channels.
  - Multi lanes for speed-up will bring much higher EMI noise.



- **Supporting Clock Deskew, Spread Spectrum Clocking**
  - More timing margin for high speed operation, in case that PCB trace doesn't match
- **Packet based**
  - Byte synchronization is embedded with HSYNC and VSYNC.
  - False synchronization protection algorithm (MIPI-like)

AnaPass *f*-MSL2 for LCD Module Interface

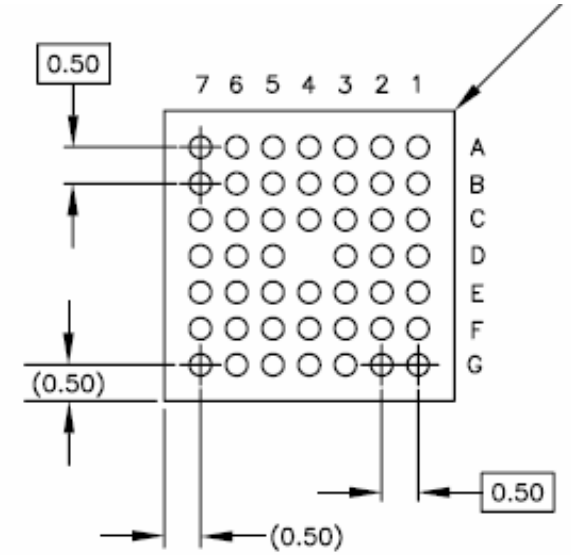
❑ ANA5351



Serial Line (Proposed Scheme)
- Low EMI by small-swing different signal
- Low Cost with small lines
- Small Size with small lines

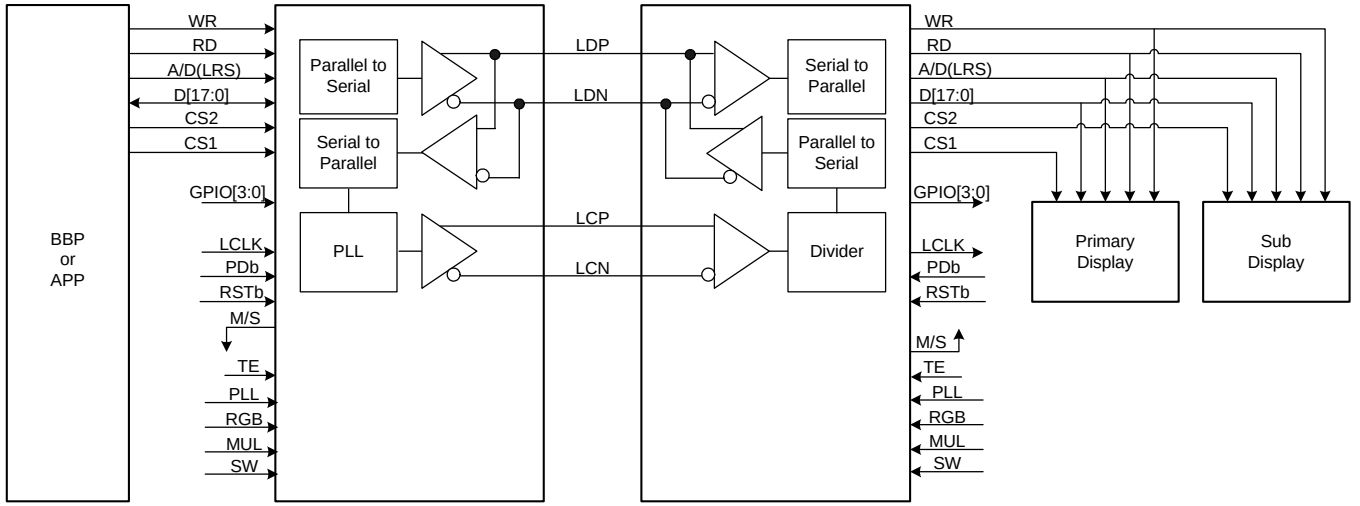
Parallel Line (Conventional Scheme)
- High EMI by full-swing signal as high frequency
- High Cost with parallel lines
- Large Size with parallel lines

AnaPass *f*-MSL2 for LCD Module Interface



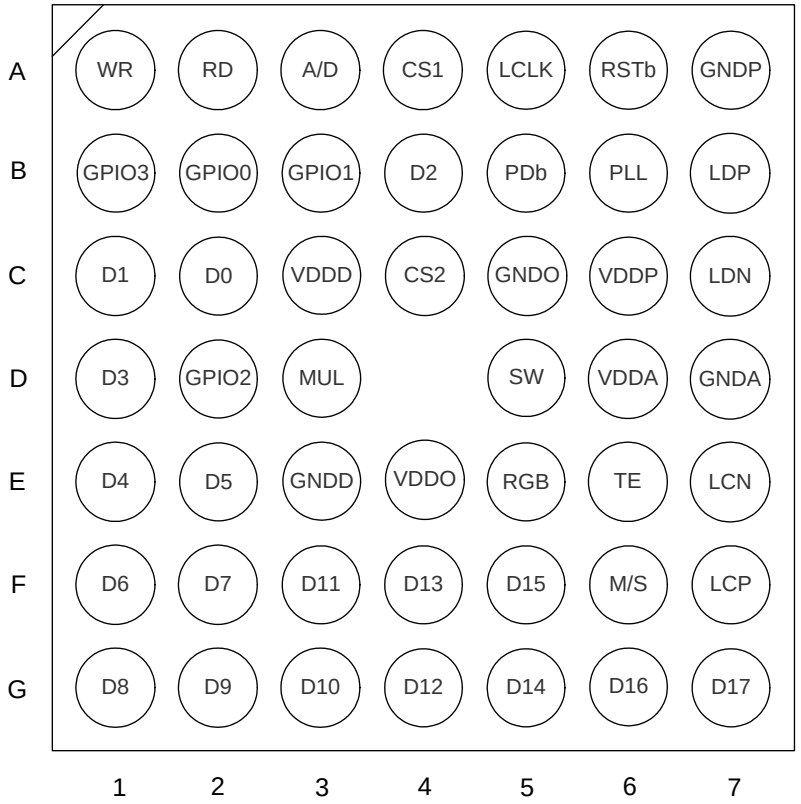
❑ ANA5351

- **SERDES one chip for LCD module interface**
  - Master/Slave selectable
  - Bi-directional
- **RGB Interface / CPU Interface**
- **Highest data throughput with single channel**
  - Slow mode: up to 100Mbps for QVGA/HVGA, 18bit @ 30fps
  - Normal mode: up to 200Mbps for VGA, 18bit @ 30fps
  - Fast mode: up to 500Mbps for VGA, 24bit @ 60fps
- **0.25um Mixed CMOS process (2.5V/1.8V)**
- **BGA 48 (4 X 4 X 0.5 X 1.0 mm) /TAPP 48 (5 X 5 X 0.5 X 0.8 mm)**
- **Sample available @ May/'05**



AnaPass *f*-MSL2 for LCD Module Interface

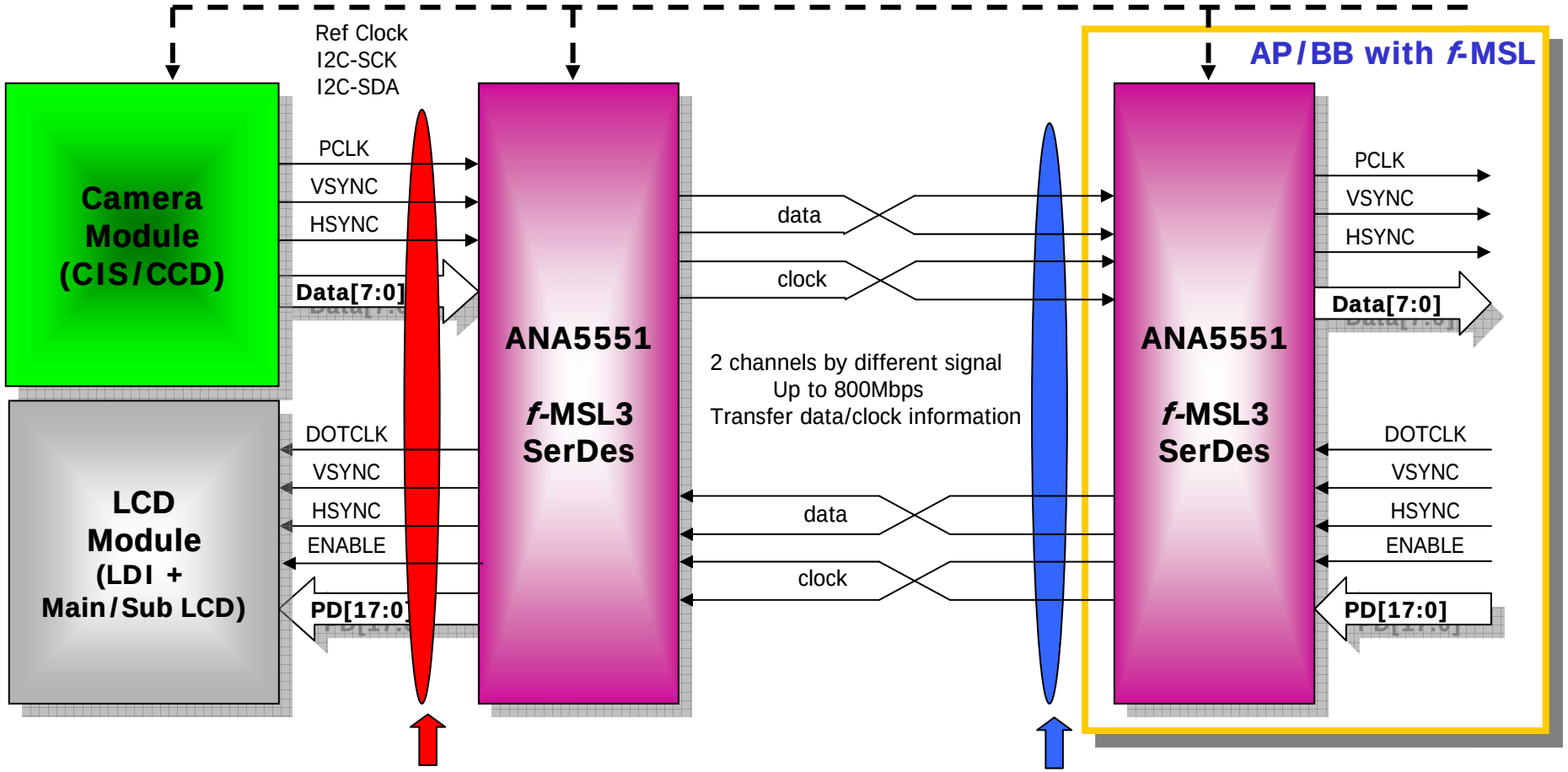
❑ ANA5351



Pin Name	I/O Type	Description
***f*-MSL PINS (4)**		
LDP, LDN	I/O	LCD positive/negative data
LCP, LCN	I/O	LCD positive/negative clock
Parallel Interface (24)		
D0~D17	I/O	18 bit LCD data bus
WR	I/O	Write strobe
RD	I/O	Read Strobe
A/D	I/O	Address/Data selection signal for LCD interface
CS1,CS2	I/O	Chip select 1, 2 for LCD interface
LCLK	I/O	PLL input clock for CPU mode/LCD PCLK for RGB mode
Configuration (12)		
M/S	I	Master/Slave selection (L: Master, H: Slave)
RSTb	I	LCD reset signal input (L: reset enable)
PDb	I	LCD power down
PLL	I	PLL range configuration (L: High frequency , H: Low frequency)
RGB	I	CPU/RGB mode selection (L:CPU mode, H:RGB mode)
MUL	I	Multiplying factor of LCLK (L:1x, H:1.5x) (Master) WR strobe extension (L:2 clock, H:3 clock) (Slave)
TE	I	Test mode enable
SW	I	Swing range configuration (L:100mV, H:150mV)
GPIO[3:0]	I/O	GPIO signals
POWER/GROUND PINS(8)		
VDDA, GNDA	PWR, GND	Power for transmitter and receiver
VDDP, GNDP	PWR, GND	Power for PLL
VDDD, GNDD	PWR, GND	Power for digital circuitry
VDDO, GNDO	PWR, GND	Power for LCD I/O

AnaPass *f*-MSL3 for Camera/LCD Interface

❑ ANA5551



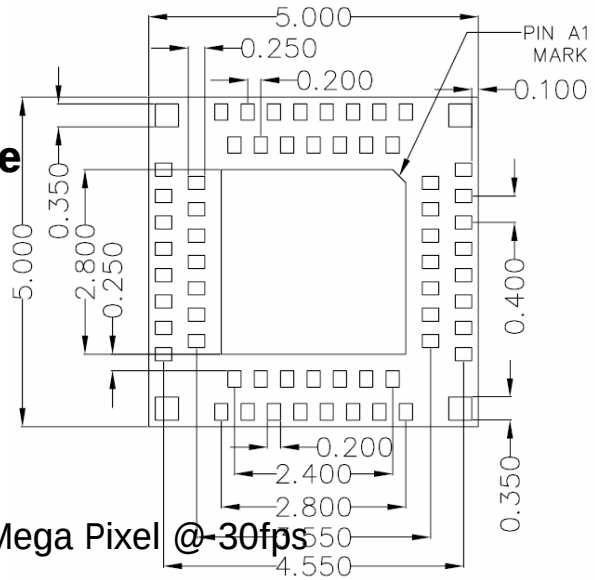
Parallel Line (Conventional Scheme)
- High EMI by full-swing signal
- High Cost with parallel lines
- Large Size with parallel lines

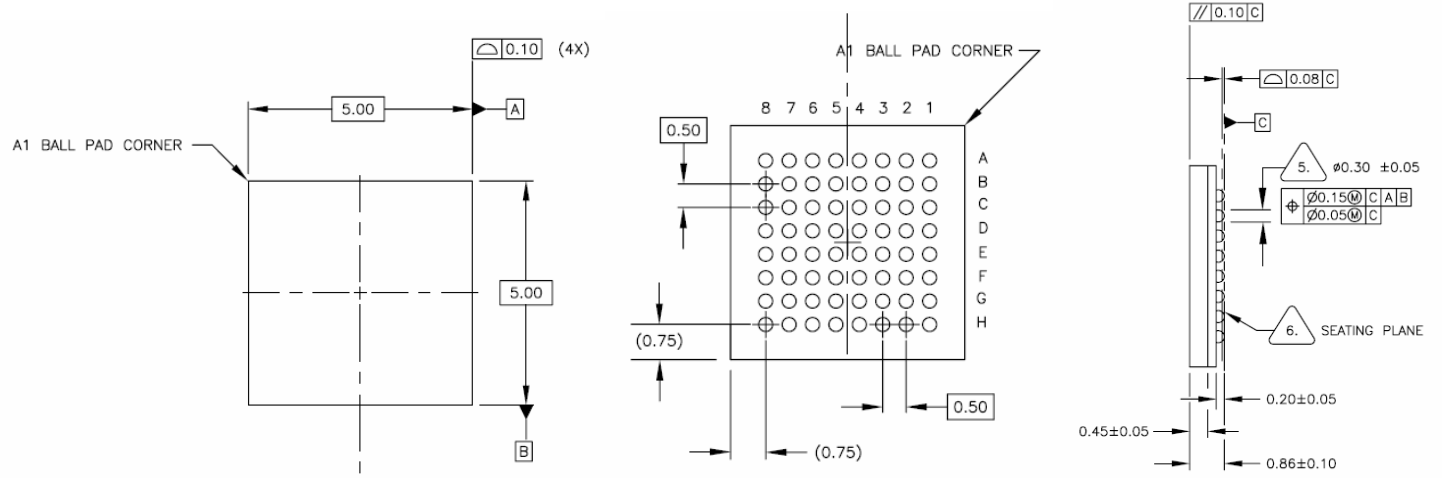
Serial Line (Proposed Scheme)
- Low EMI by small-swing different signal
- Low Cost with small lines
- Small Size with small lines

AnaPass *f*-MSL3 for Camera/LCD Interface

ANA5551

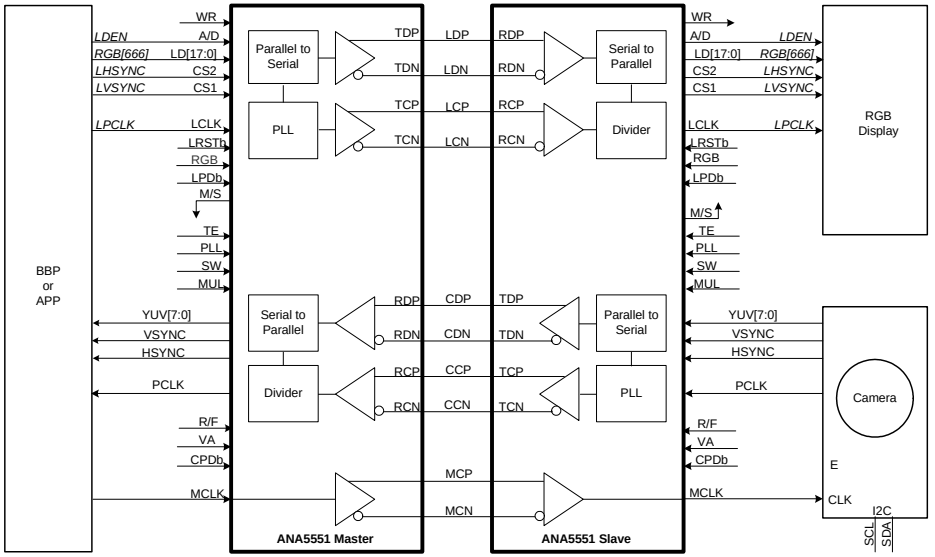
- **SERDES one chip for Camera/LCD module interface**
  - Master/Slave selectable
  - Bi-directional
- **Support RGB Interface / CPU Interface for LCD**
- **Highest data throughput with single channel**
  - Slow mode: up to 100Mbps for 0.3Mega Pixel @ 15fps
  - Normal mode: up to 250Mbps for 1Mega Pixel @ 15fps
  - Fast mode: up to 500Mbps for 2Mega Pixel @ 15fps
  - Ultra fast mode: up to 800Mbps for 3Mega Pixel @ 15fps, 1Mega Pixel @ 30fps
- **0.25um Mixed CMOS process (2.5V/1.8V)**
- **BGA 64 (5 X 5 X 0.5 X 1.0 mm) /TAPP 64 (5 X 5 X 0.4X 0.8 mm)**
- **Sample available @ May/'05**



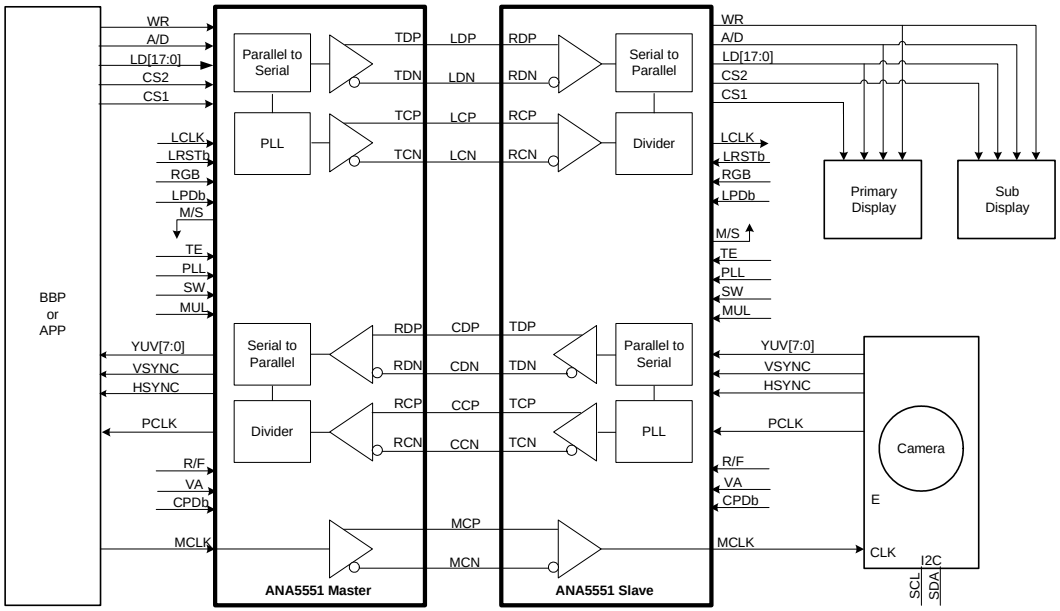


AnaPass *f*-MSL3 for Camera/LCD Interface

- **ANA5551**
  - **RGB Interface (TBR)**

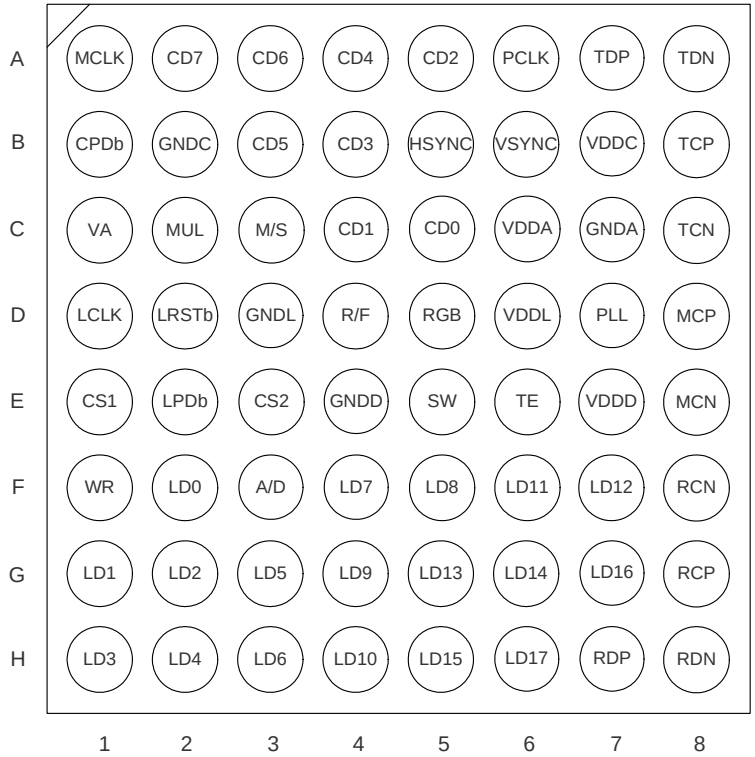


- **CPU Interface**



AnaPass *f*-MSL3 for Camera/LCD Interface

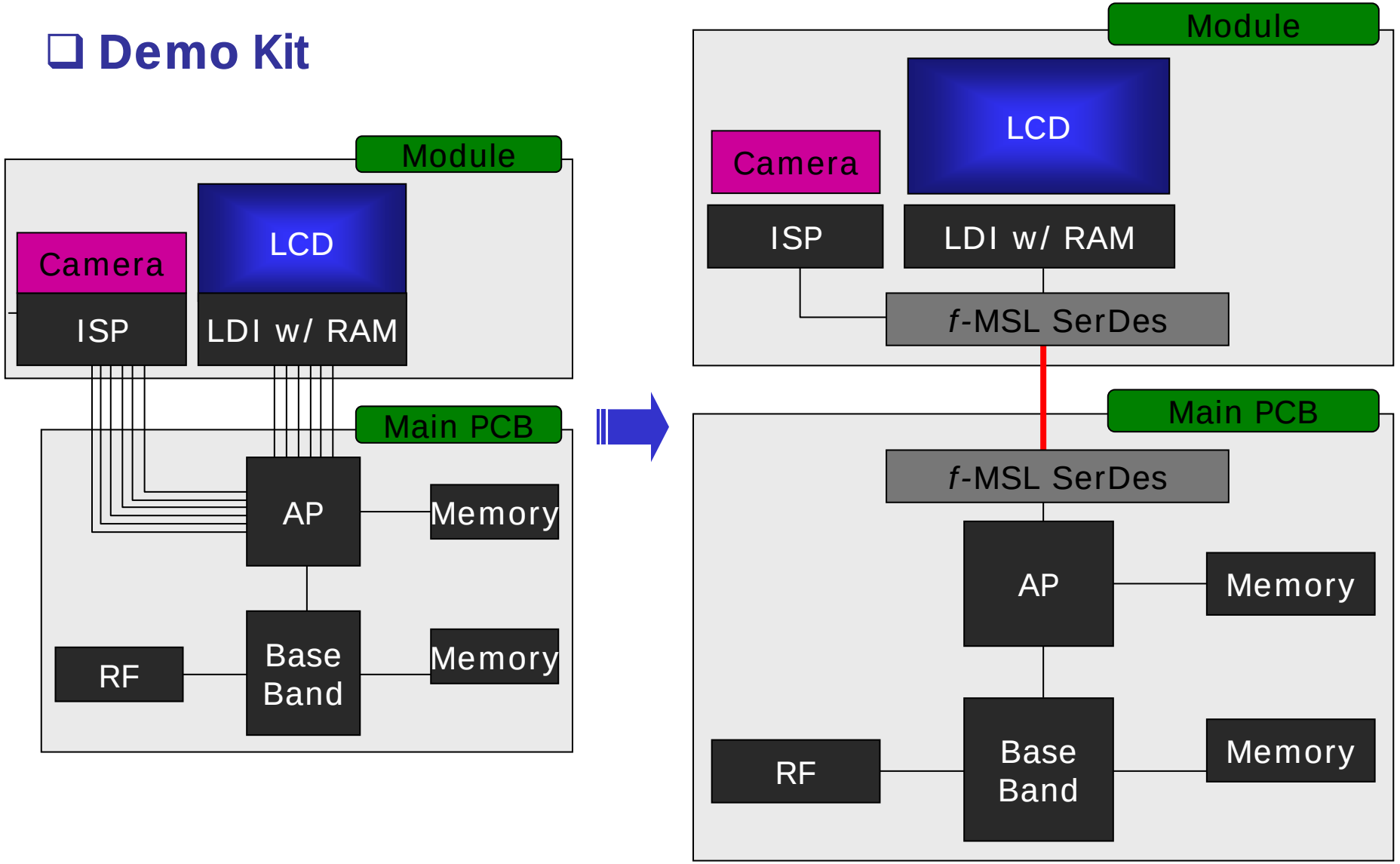
❑ ANA5551



Pin Name	I/O Type	Description
***f*-MSL Interface (10)**		
TDP, TDN	O	Positive/negative data transmitter
TCP, TCN	O	Positive/negative clock transmitter
RDP, RDN	I	Positive/negative data receiver
RCP, RCN	I	Positive/negative clock receiver
MCP, MCN	I/O	Camera positive/negative main clock
LCD Interface (23)		
LD0~LD17	I/O	18 bit LCD data bus
WR	I/O	Write strobe for LCD interface
A/D	I/O	Address/Data selection signal for LCD interface
CS1,CS2	I/O	Chip select 1, 2 for LCD interface
LCLK	I/O	PLL reference clock for CPU mode/LCD PCLK for RGB mode
Camera Interface (12)		
CD0~CD7	I/O	8 bit camera data bus
VSYNC	I/O	VSYNC for camera interface
HSYNC	I/O	HSYNC for camera interface
PCLK	I/O	Pixel clock for camera interface
MCLK	I/O	Main clock for camera interface
Configuration (11)		
M/S	I	Master/Slave selection (L: Master, H: Slave)
LRSTb	I	LCD reset signal input (L: Reset enable)
RGB	I	RGB/CPU mode selection (L: CPU mode, H: RGB mode)
LPDb	I	LCD power down
R/F	I	Clock triggering edge selection (L: Rising, H: Falling)
VA	I	VSYNC active mode selection (L: Low, H: High)
CPDb	I	Camera power down
TE	I	Test mode enable
PLL	I	PLL range configuration (L: High frequency, H: Low frequency)
SW	I	Swing range configuration (L: Small swing, H: Large swing)
MUL	I	Internal clock multiplier configuration (L: 1x, H: 1.5x)
Power/Ground (8)		
VDDA, GNDA	PWR, GND	Power for analog circuitry
VDDD, GNDD	PWR, GND	Power for digital circuitry
VDDL, GNDL	PWR, GND	Power for LCD I/O
VDDC, GNDC	PWR, GND	Power for Camera I/O

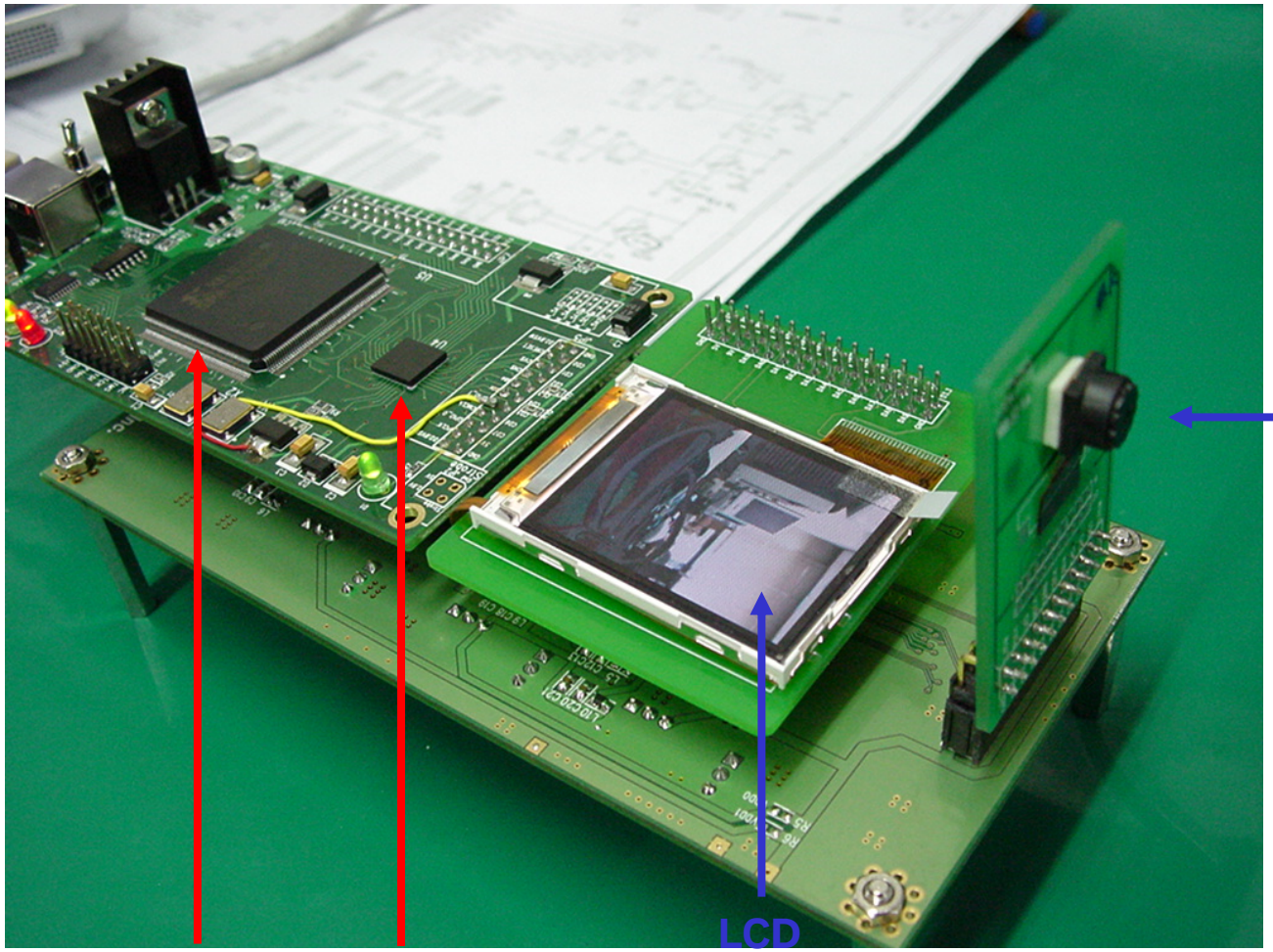
Evaluation & Demonstration

❑ Demo Kit



Evaluation & Demonstration

- *f*-MSL3 Demo Kit (Camera/LCD module interface)



Evaluation & Demonstration

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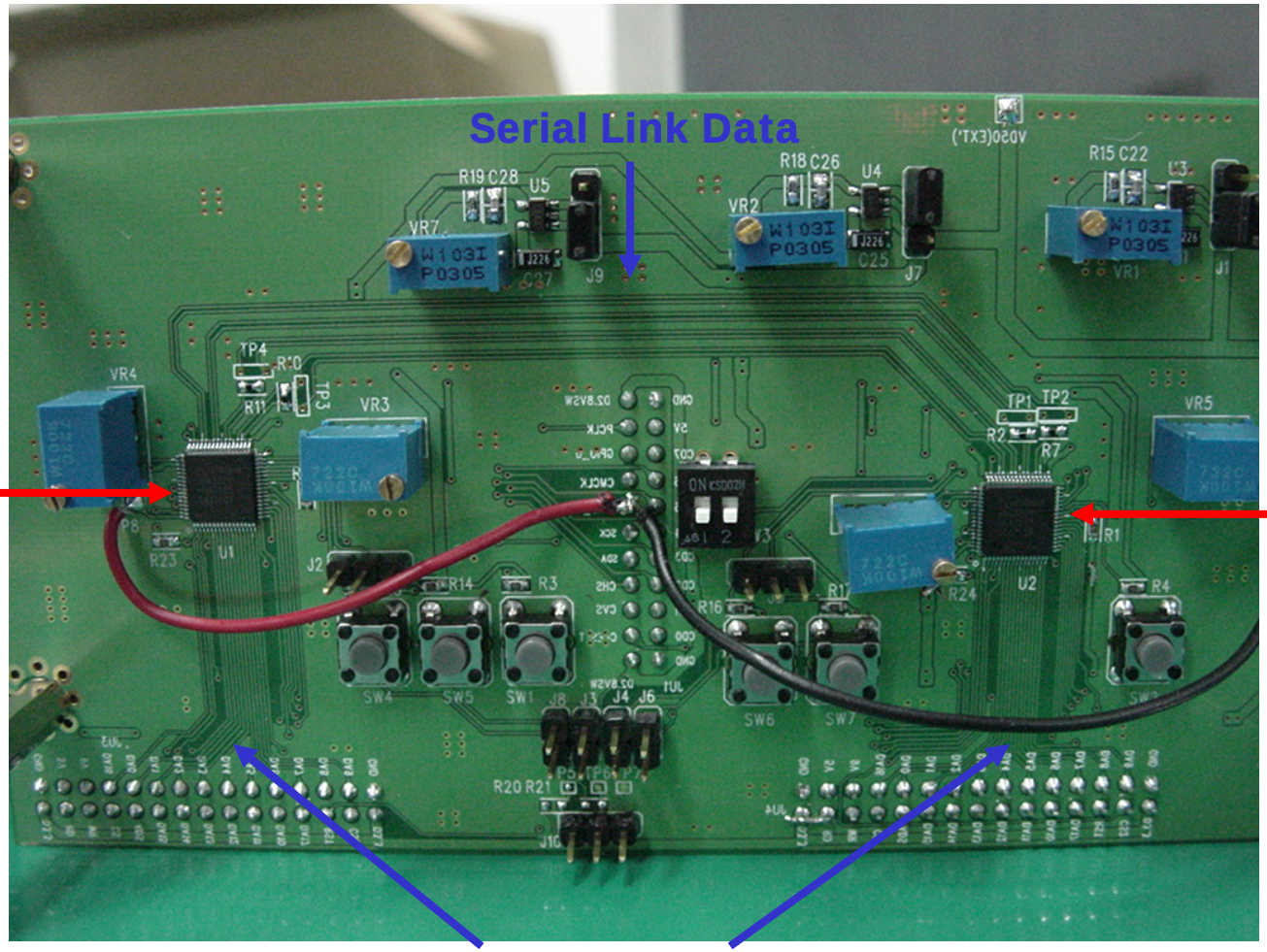

Evaluation & Demonstration

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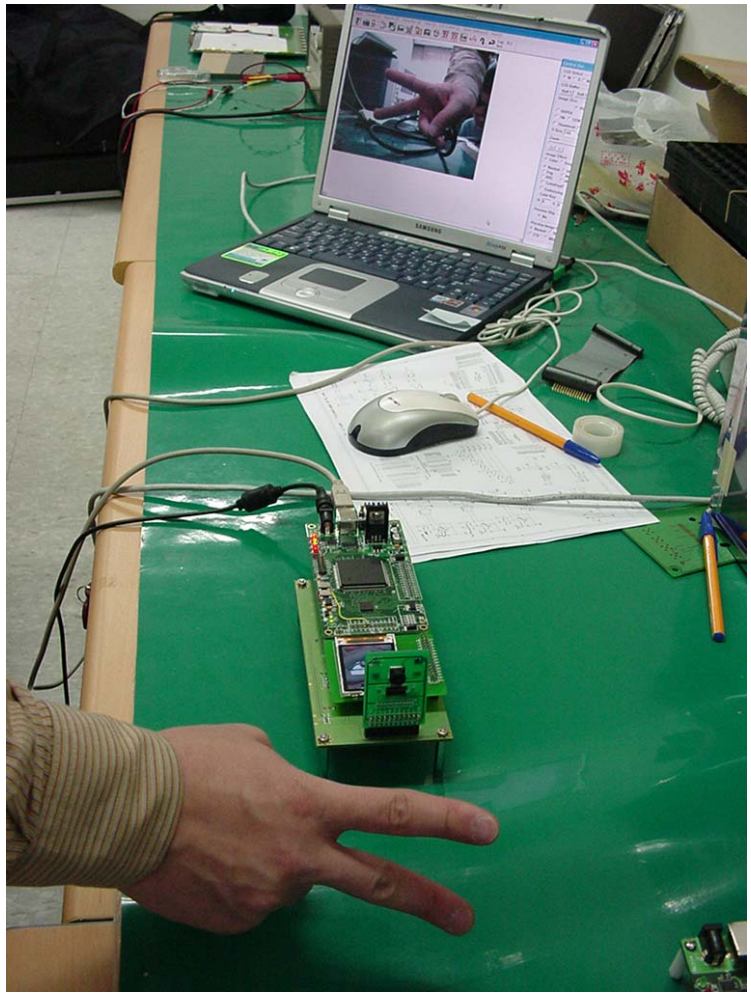

Evaluation & Demonstration

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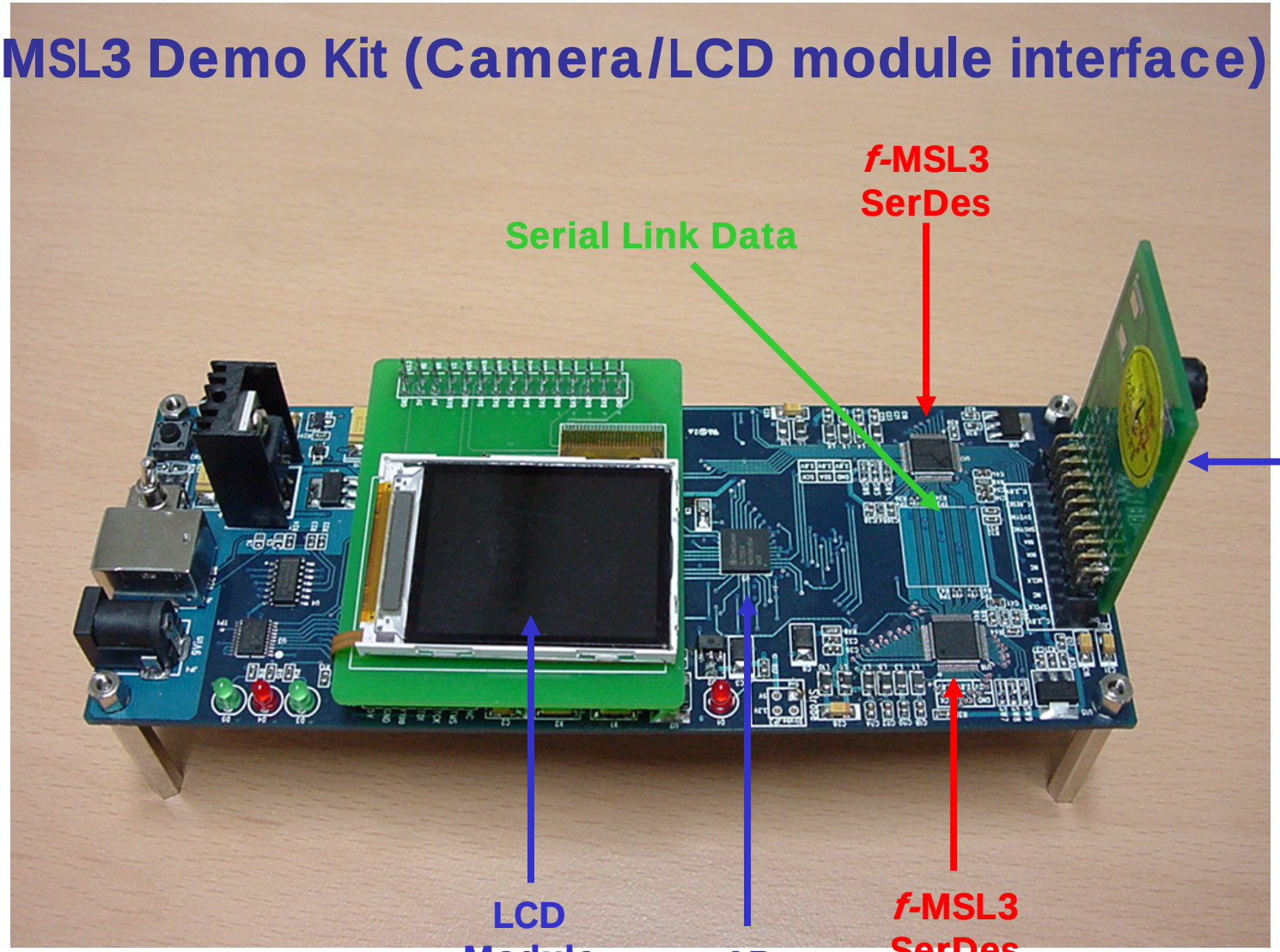

Thank you !

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