APPLICATION NOTE
SC4519

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APPLICATION NOTE

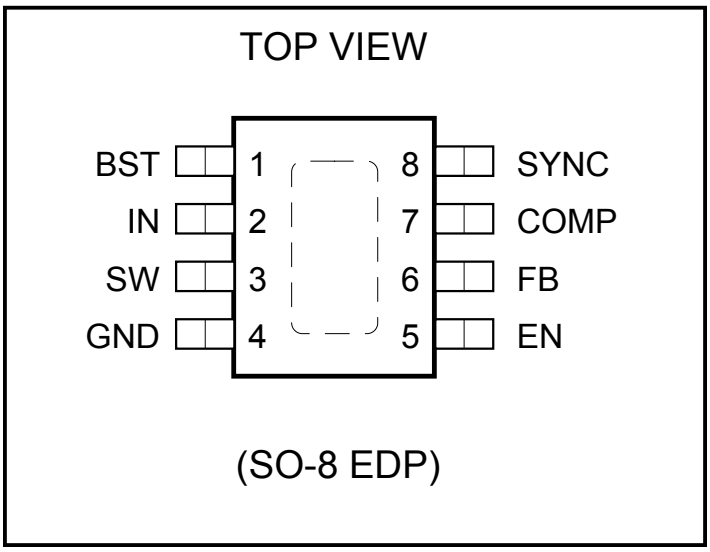
SC4519 Description

The SC4519 is a current mode switching regulator with an integrated switch, operating at 600kHz with separate sync & enable functions. The integrated switch allows for cost effective low power solutions (peak switch current 2 amps). The sync function allows customers to synchronize to a faster clock in order to avoid frequency beating in noise sensitive applications. High frequency of operation allows for very small passive components. Current mode operation allows for fast dynamic response & instantaneous duty cycle adjustment as the input varies (ideal for CPE applications where the input is a wall plug power).

The low shutdown current makes it ideal for portable applications where battery life is important.

The SC4519 is a 600kHz switching regulator synchronizable to a faster frequency from 750kHz to 1.2MHz.

SC4519 Pin Configurations



sc4519 Pin Descriptions

Pin #	Pin Name	Pin Function
1	BST	This pin provides power to the internal NPN switch. The minimum turn on voltage for this switch is 2.7V.
2	IN	Pin IN delivers all power required by control and power circuitry. This pin sees high di/dt during switching actions of the switch. A decoupling capacitor should be attached to this pin as close as possible.
3	SW	Pin SW is the emitter of the internal switch. The external freewheeling diode should be connected as close as possible to this pin.
4	GND	All voltages are measured with respect to this pin. The decoupling capacitor and the freewheeling diode should be connected to GND as short as possible.
5	EN	This is the chip enable input. The regulator is switched on if EN is high, and it is off if EN is low. The regulator is in standby mode when EN is low, and the input supply current is reduced to a few microamperes.
6	FB	Feedback input for adjustable output controllers.
7	COMP	This is the output of the internal error amplifier and input of the peak current comparator. A compensation network is connected to this pin to achieve the specified performance.
8	SYNC	This is synchronous control pin used to synchronize the internal oscillator to an external pulse control signal. When not used, it should be connected to GND.
-	THERMAL PAD	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

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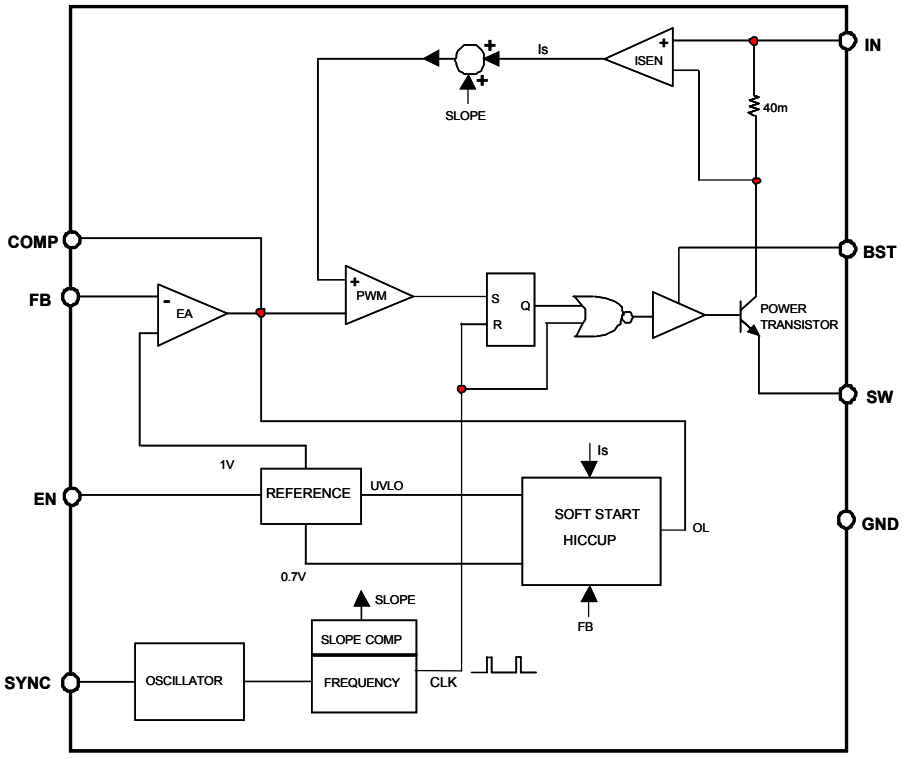
SC4519 Block Diagram



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SC4519 General Overview

The SC4519 is a current mode buck converter regulator. SC4519 has an internal fixed-frequency clock. The SC4519 uses two feedback loops that control the duty cycle of the internal power switch. The error amplifier functions like the one of the voltage mode converter. The output of the error amplifier works as a switch current reference. This technique effectively removes one of the double poles in the voltage mode system. With this, it is much easier to compensate a current mode converter to have better performance. A minimum 2.7V voltage is required to saturate the switch when it is on to reduce its conduction loss.The current sense amplifier in the SC4519 monitors the switch current during each cycle. Overcurrent protection (OCP) is triggered when the current limit exceeds the upper limit of 3A, detected by a voltage on COMP greater than about 2V. When an OCP fault is detected, the switch is turned off and the external COMP capacitor is quickly discharged using an internal npn transistor. Once the COMP voltage has fallen below 250mV, an internal timer prevents any operation for 50µs, after which the part enters a normal startup cycle. In the case of sustained overcurrent or dead-short, the part will continually cycle through the retry sequence as described above, at a rate dependent on the value of Ccomp. During start up, the voltage on COMP rises roughly at the rate of dv/dt=120µA/C_{comp}. C_{comp} is the total capacitance value attached to COMP. Therefore, the retry time for a sustained overcurrent can be approximately calculated as:

$$T_{retry} = C_{comp} \cdot \frac{2V}{120uA} + 50us$$

Figure 1 shows the voltage on COMP during a sustained overcurrent condition.

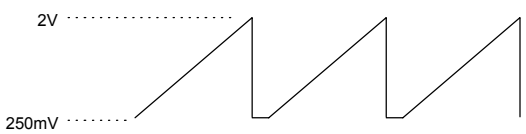

Figure 1. Voltage on COMP for Startup and OCP

Enable

Pulling and holding the EN pin below 0.4V activates the shut down mode of the SC4519 which reduces the input supply current to less than 10µA. During the shut down mode, the switch is turned off. The SC4519 is turned on if the EN pin is pulled high.

Oscillator

Its internal free running oscillator sets the PWM frequency at 600 kHz for the SC4519 without any external components to program the frequency. An external clock with a duty cycle from 20% to 80% connected to the SYNC pin activates synchronous mode. The frequency of the external clock can be from 750kHz to 1.2MHz.

UVLO

When the EN pin is pulled and held above 2V, the voltage on Pin IN determines the operation of the SC4519. As V_{IN} increases during power up, the internal circuit senses V_{IN} and keeps the power transistor off until V_{IN} reaches 2.6V.

Load Current

The peak current I_{PEAK} in the switch is internally limited. For a specific application, the allowed load current I_{OMAX} will change if the input voltage drifts away from the original design as given for current continuous mode:

$$I_{OMAX} = 3 - \frac{V_O \cdot (1 - D)}{2 \cdot L \cdot f_s}$$

Where:
f_s = switching frequency,
V_O = output voltage;
D = duty ratio, V_o/V_I;
V_I = input voltage

Figure 2 shows the theoretical maximum load current for the specific cases. In a real application, however, the allowed maximum load current also depends on the layout and the air cooling condition. Therefore, the maximum load current may need to be degraded according to the thermal situation of the application.

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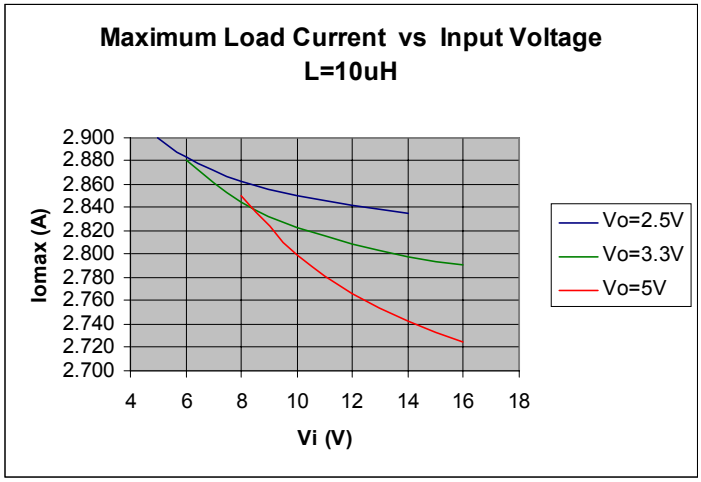

Figure 2. Theoretical maximum load current curves.

Inductor Selection

The factors for selecting the inductor include its cost, efficiency, size and EMI. For a typical SC4519 application, the inductor selection is mainly based on its value, saturation current and DC resistance. Increasing the inductor value will decrease the ripple level of the output voltage while the output transient response will be degraded. Low value inductors offer small size and fast transient responses while they cause large ripple currents, poor efficiencies and more output capacitance to filter out the large ripple currents. The inductor should be able to handle the peak current without saturating and its copper resistance in the winding should be as low as possible to minimize its resistive power loss. A good trade-off among its size, loss and cost is to set the inductor ripple current to be within 15% to 30% of the maximum output current.

The inductor value can be determined according to its operating point under its continuous mode and the switching frequency as follows:

$$L = \frac{V_O \cdot (V_I - V_O)}{V_I \cdot f_s \cdot \Delta I \cdot I_{OMAX}}$$

Where:
f_s = switching frequency,
ΔI = ratio of the peak to peak inductor current to the output load current and
V_O = output voltage.

The peak to peak inductor current is:

$$I_{p-p} = \Delta I \bullet I_{OMAX}$$

After the required inductor value is selected, the proper selection of the core material is based on the peak inductor current and efficiency specifications. The core must be able to handle the peak inductor current I_{PEAK} without saturation and produce low core loss during the high frequency operation.

$$I_{PEAK} = I_{OMAX} + \frac{I_{p-p}}{2}$$

The power loss for the inductor includes its core loss and copper loss. If possible, the winding resistance should be minimized to reduce inductor's copper loss. The core must be able to handle the peak inductor current I_{PEAK} without saturation and produce low core loss during the high frequency operation. The power loss for the inductor includes its core loss and copper loss. If possible, the winding resistance should be minimized to reduce inductor's copper loss. The core loss can be found in the manufacturer's datasheet. The inductor's copper loss can be estimated as follows:

$$P_{COPPER} = I^2_{LRMS} \cdot R_{WINDING}$$

Where:
I_{LRMS} is the RMS current in the inductor. This current can be calculated as follows:

$$I_{LRMS} = I_{OMAX} \cdot \sqrt{1 + \frac{1}{3} \cdot \Delta I^2}$$

Table 1. Inductor parameter comparison

VENDOR	TYPE	INDUCTANCE (µH)	DCR (mΩ)	I_{SAT} (A)
COOPER	DR73-1R0	1	10.2	7.97
	DR73-1R5	1.5	13	6.52
	DR73-2R2	2.2	16.5	5.52
	DR73-3R3	3.3	25.9	4.42
	DR73-4R7	4.7	29.7	3.78
	DR73-6R8	6.8	43.5	3.12
	DR73-8R2	8.2	59.2	2.66
	DR73-100	10	65.6	2.47
	DR74-1R0	1	9.9	10.2
	DR74-1R5	1.5	11.8	8.35
	DR74-2R2	2.2	12.6	7.06
	DR74-3R3	3.3	18.3	5.4
	DR74-4R7	4.7	25.4	4.37
	DR74-6R8	6.8	41.8	3.67
	DR74-8R2	8.2	44.1	3.4
	DR74-100	10	48.9	3.17
TOKO	919-AS-1RON=P3	1	5.9	13.6
	919-AS-1R8N=P3	1.8	7.6	10.4
	919-AS-2R8N=P3	2.8	10.7	8.3
	919-AS-3R7N=P3	3.7	14.2	7
	919-AS-4R7N=P3	4.7	16.2	6.1
	919-AS-6R4N=P3	6.4	22.9	5.2
	919-AS-7R5N=P3	7.5	23	4.8
	919-AS-100N=P3	10	26.5	4.3

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Output Capacitor Selection

Basically there are two major factors to consider in selecting the type and quantity of the output capacitors. The first one is the required ESR (Equivalent Series Resistance) which should be low enough to reduce the output voltage deviation during load changes. The second one is the required capacitance, which should be high enough to hold up the output voltage. Before the SC4519 regulates the inductor current to a new value during a load transient, the output capacitor delivers all the additional current needed by the load. The ESR and ESL of the output capacitor, the loop parasitic inductance between the output capacitor and the load combined with inductor ripple current are all major contributors to the output voltage ripple. Surface mount ceramic capacitors are recommended.

Input Capacitor Selection

The input capacitor selection is based on its ripple current level, required capacitance and voltage rating. This capacitor must be able to provide the ripple current by the switching actions. For the continuous conduction mode, the RMS value of the input capacitor current $I_{CIN(RMS)}$ can be calculated from:

$$I_{CIN(RMS)} = I_{OMAX} \cdot \sqrt{\frac{V_O \cdot (V_I - V_O)}{V^2_I}}$$

This current gives the capacitor's power loss through its $R_{CIN(ESR)}$ as follows:

$$P_{CIN} = I^2_{CIN(RMS)} \bullet R_{CIN(ESR)}$$

The input ripple voltage mainly depends on the input capacitor's ESR and its capacitance for a given load, input voltage and output voltage. Assuming that the input current of the converter is constant, the required input capacitance for a given voltage ripple can be calculated by:

$$C_{IN} = I_{OMAX} \cdot \frac{D \cdot (1-D)}{fs \cdot (\Delta V_I - I_{OMAX} \cdot R_{CIN(ESR)})}$$

Where:
ΔV_I = the given input voltage ripple.

Because the input capacitor is exposed to the large surge current, attention is needed for the input capacitor. If tantalum capacitors are used at the input side of theconverter, one needs to ensure that the RMS and surge ratings are not exceeded. For generic tantalum capacitors, it is suggested to derate their voltage ratings at a ratio of about two to protect these input capacitors.

Table 2. Capacitor parameter comparison

VENDOR	TYPE	CAPACITANCE (µF)	VOLTAGE (V)	PACKAGE
TDK	C3216X7R1C225K	2.2	16	1206
	C3225X7R1E225M	2.2	25	1210
muRata	GRM42-6X7R105K25	1	25	1206
	GRM42-2X7R105K50	1	50	1210
	GRM42-6X7R225K16	2.2	16	1206
	GRM42-2X7R225K25	2.2	25	1210
	GRM42-652X5R475K25	4.7	25	1206
	GRM42-653X5R106K10	10	10	1206
	GRM42-2X5R106K25	10	25	1210
	GRM42-6X5R226K6.3	22	6.3	1206
	GRM42-2X5R476M6.3	47	6.3	1210

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Boost Capacitor Selection

The boost capacitor selection is based on its discharge ripple voltage, worst case conduction time and boost current. The worst case conduction time T_w can be estimated as follows:

$$T_W = \frac{1}{f_s} \cdot D_{max}$$

Where:
f_s = the switching frequency and
Dmax = maximum duty ratio, 0.9 for the SC4519.

The required minimum capacitance for the boost capacitor will be:

$$C_{boost} = \frac{I_B}{V_D} \cdot T_W$$

Where:
I_B = the boost current and
V_D= discharge ripple voltage.

With f_s = 600kHz, V_D = 0.5V and I_B =0.045A, the required minimum capacitance for the boost capacitor is:

$$C_{boost} = \frac{I_B}{V_D} \cdot \frac{1}{f_s} \cdot D_{max} = \frac{0.045}{0.5} \cdot \frac{1}{600k} \cdot 0.9 = 135nF$$

The internal driver of the switch requires a minimum 2.7V to fully turn on that switch to reduce its conduction loss. If the output voltage is less than 2.7V, the boost capacitor can be connected to either the input side or an independent supply with a decoupling capacitor. But the Pin BST should not see a voltage higher than its maximum rating.

Freewheeling Diode Selection

This diode conducts during the switch's off-time. The diode should have enough current capability for full load and short circuit conditions without any thermal concerns. Its maximum repetitive reverse block voltage has to be higher than the input voltage of the SC4519. A low forward conduction drop is also required to increase the overall efficiency. The freewheeling diode should be turned on and off fast with minimum reverse recovery because the SC4519 is designed for high frequency applications. SS33 Schottky rectifier is recommended for certain applications. The average current of the diode, I_{D-AVG} can be calculated by:

$$I_{D\_AVG} = I_{Omax} \cdot (1 - D)$$

There are three major power dissipation sources for the SC4519. The internal switch conduction loss, its switching loss due to the high frequency switching actions and the base drive boost circuit loss. These losses can be estimated as:

$$P_{total} = I_o^2 \cdot R_{on} \cdot D + 10.8 \cdot 10^{-3} \cdot I_o \cdot V_I + \frac{10}{1000} \cdot I_o \cdot D \cdot (V_{boost})$$

Where:
I_O = load current;
R_{ON} = on-equivalent resistance of the switch;
V_{BOOST} = input voltage or output based on the boost circuit connection.

Thermal Considerations

The junction temperature of the SC4519 can be further decided by:

$$T_J = T_A + \theta_{JA} \cdot P_{total}$$

θ_{JA} is the thermal resistance from junction to ambient. Its value is a function of the IC package, the application layout and the air cooling system.

The freewheeling diode also contributes a significant portion of the total converter loss. This loss should be minimized to increase the converter efficiency by using Schottky diodes with low forward drop (V_F).

$$P_{diode} = V_F \cdot I_o \cdot (1 - D)$$

Loop Compensation Design

Assuming the power stage ESR (equivalent series resistance) zero is an order of magnitude higher than the closed loop bandwidth, which is typically one tenth of the switching frequency, the power stage control to output transfer function with the current loop closed (Ridley model) for the SC4519 will be as follows:

$$G_{VD}(s) = \frac{2.5 \cdot R_L}{1 + \frac{s}{\frac{1}{R_L \cdot C}}}$$

Where:
R_L – Load and
C – Output capacitor.
The goal of the compensation design is to shape the loop to have a high DC gain, high bandwidth, enough phase margin, and high attenuation for high frequency noises.

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Figure 3 gives a typical compensation network which offers 2 poles and 1 zero to the power stage:

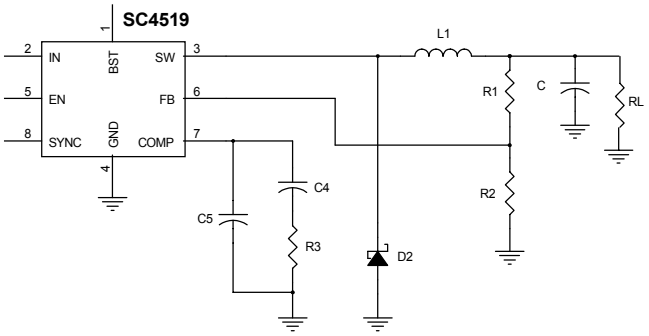

Figure 3. Compensation network provides 2 poles and 1 zero.

The compensation network gives the following characteristics:

$$G_{COMP}(s) = \omega_1 \cdot \frac{1+\frac{s}{\omega_Z}}{s\cdot(1+\frac{s}{\omega_{P2}})} \cdot g_m \cdot \frac{R_2}{R_1+R_2}$$

Where:

$$\omega_1 = \frac{1}{C_4 + C_5}$$

$$\omega_Z = \frac{1}{R_3 \cdot C_4}$$

$$\omega_{P2} = \frac{C_4 + C_5}{R_3 \cdot C_4 \cdot C_5}$$

The loop gain will be given by:

$$T(s) = G_{COMP}(s) \cdot G_{VD}(s) =$$

$$2.125 \cdot 10^{-3} \cdot \frac{R_L}{C_4} \cdot \frac{R_2}{R_1+R_2} \cdot \frac{1}{s} \frac{1+\frac{s}{\omega_Z}}{(1+\frac{s}{\omega_{P1}})\cdot(1+\frac{s}{\omega_{P2}})}$$

where:

$$\omega_{p1} = \frac{1}{R_L \cdot C}$$

One integrator is added at origin to increase the DC gain. ω_Z is used to approximately cancel the power stage pole ω_{P1} so that the loop gain has –20dB/dec rate when it reaches 0dB line. ω_{P2} is placed at half switching frequency to reject high frequency switching noises. Figure 4 gives the asymptotic diagrams of the power stage with current loop closed and its loop gain.

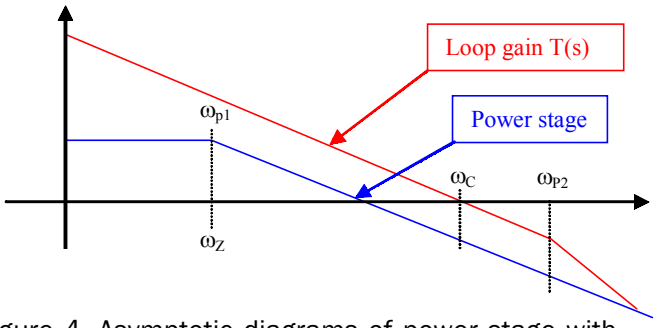

Figure 4. Asymptotic diagrams of power stage with current loop closed and its loop gain.

The design guidelines for the SC4519 applications are as following:

1. Set the loop gain crossover corner frequency ω_c for given switching corner frequency $\omega_c = 2\pi f_c$
2. Place an integrator at the origin to increase DC and low frequency gains.
3. Select ω_z such that it is roughly placed at ω_{P1} to obtain a -20dB/dec rate to go across the 0dB line.
4. Place a high frequency compensator pole ω_{P2} ($\omega_{P2} = \pi f_s$) to get the maximum attenuation of the switching ripple and high frequency noise with the adequate phase lag at ω_c.

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Layout guidelines

In order to achieve optimal electrical and thermal performance for high frequency converters, special attention must be paid to the PCB layouts. The goal of layout optimization is to identify the high di/dt loops and minimize them. The following guidelines should be used to ensure proper operation of the converters.

1. A ground plane is suggested to minimize switching noises and trace losses and maximize heat transferring.
2. Start the PCB layout by placing the power components first. Arrange the power circuit to achieve a clean power flow route. Put all power connections on one side of the PCB with wide copper filled areas if possible.
3. The V_{IN} bypass capacitor should be placed next to
4. The trace connecting the feedback resistors to the output should be short, direct and far away from any noise sources such as switching node and switching components.
5. Minimize the loop including input capacitor, the SC4519 and freewheeling diode D_2. This loop passes high di/dt current. Make sure the trace width is wide enough to reduce copper losses in this loop.
6. Maximize the trace width of the loop connecting the inductor, freewheeling diode D_2 and the output capacitor.
7. Connect the ground of the feedback divider and the compensation components directly to the GND pin of the SC4519 by using a separate ground trace.
8. Connect Pin 4 and the bottom thermal pad to a large copper area to remove the IC heat and increase the power capability of the SC4519. A few feedthrough holes are required to connect this large copper area to a ground plane to further improve the thermal environment of the SC4519. The traces attached to other pins should be as wide as possible for the same purpose.

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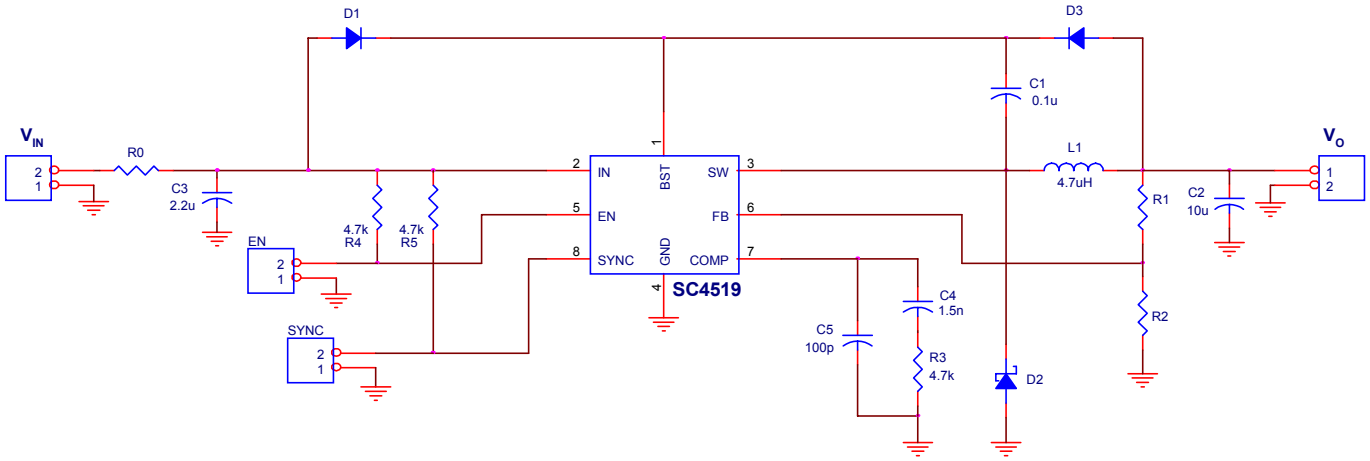
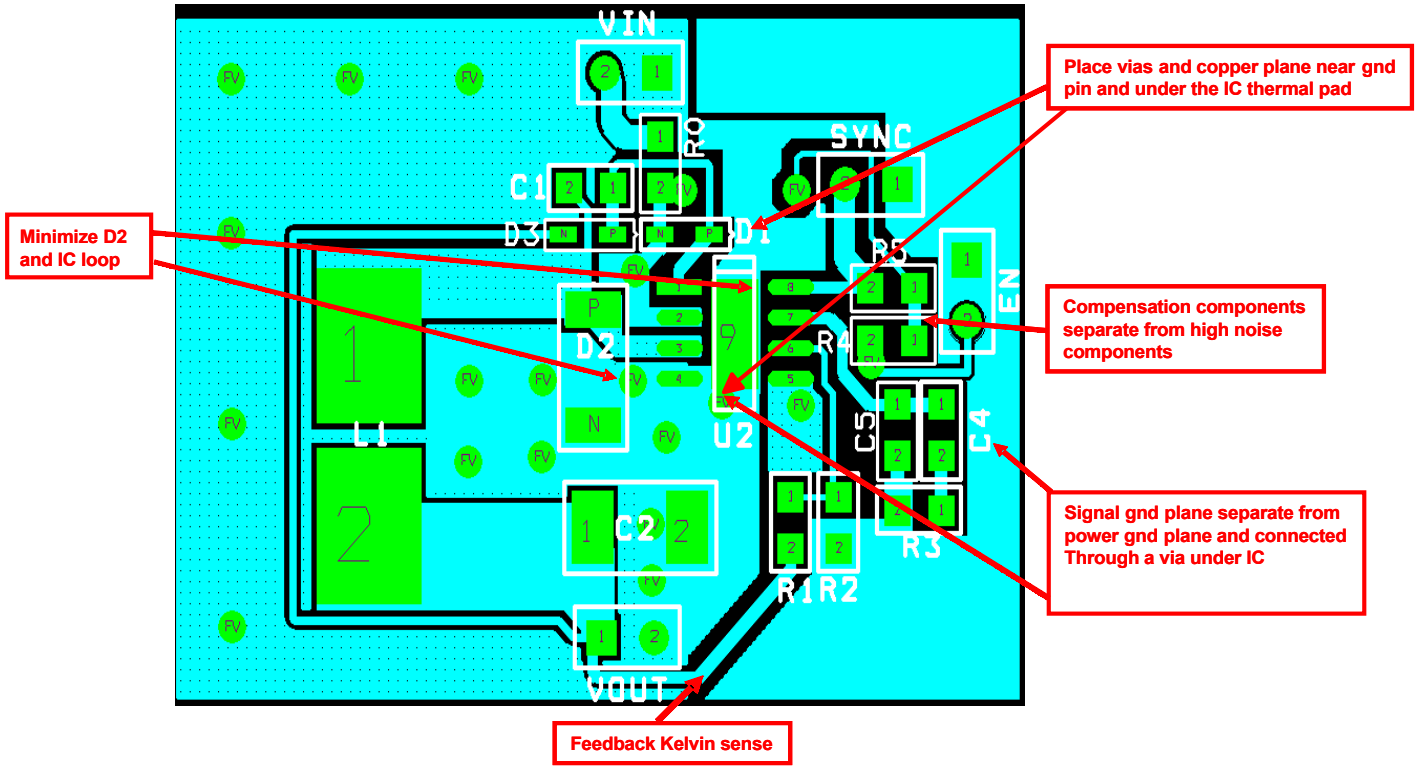
Layout guidelines (cont)



Top view



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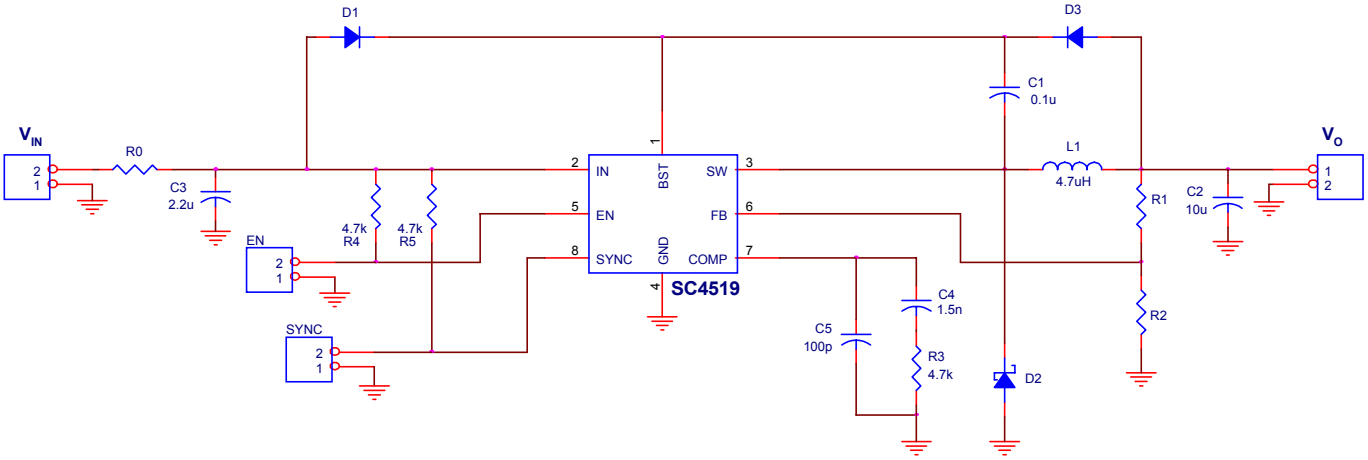
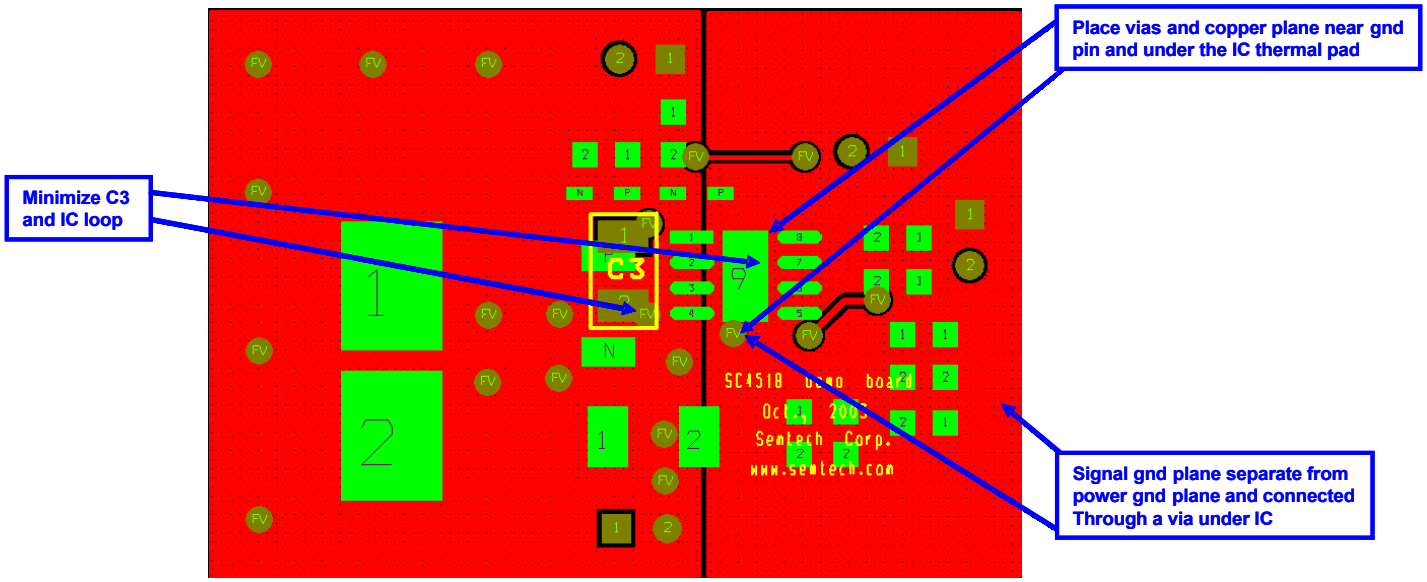
Layout guidelines (cont)



Bottom view



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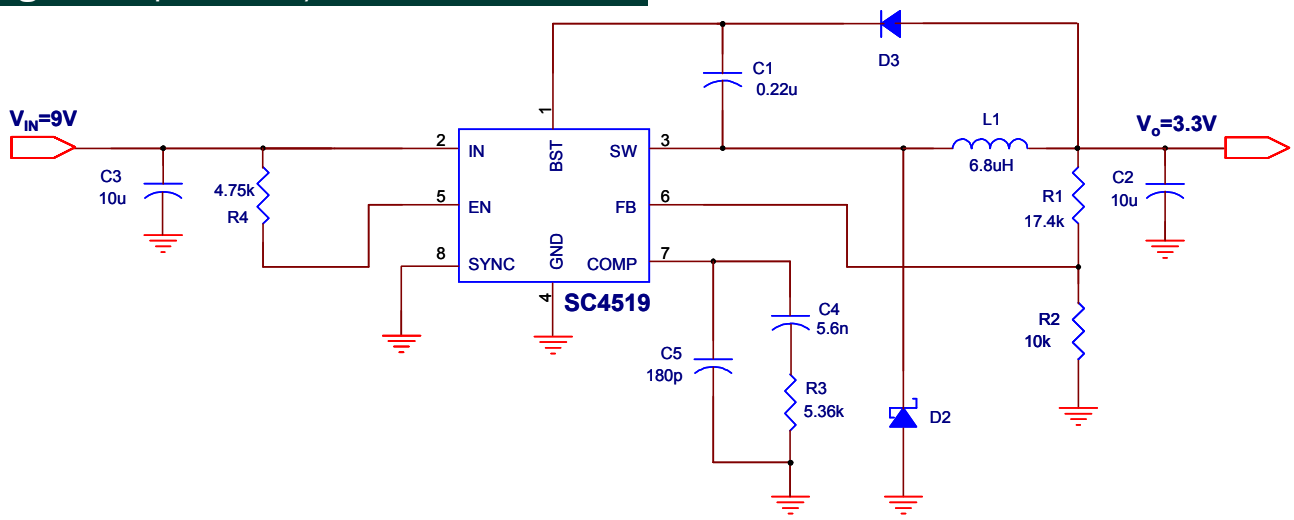
Design Example 1: 9V /3.3V 2.5A



Bill of Materials

Item	Qty	Reference	Value	Part No./Manufacturer
1	1	C1	0.22uF, 25V, 0805, X7R	
2	2	C2, C3	10u, 1210, X5R, 25V	Panasonic
3	1	C4	5.6n, 0805, X7R, 25V	Vishay
4	1	C5	180pF	
5	1	D3	1N4148WS, SOD-323	
6	1	D2	SS33	Fairchild P/N: SS33
7	1	L1	6.8uH	Cooper P/N: DR125-6R8
8	1	R1	17.4k	
9	1	R2	10k	
10	1	R3	5.36k	
11	1	R4	4.75k	
12	1	U1	SC4519	Semtech

Unless specified, all resistors have 1% precision with 0603 package.
Resistors are +/-1% and all capacitors are +/-20%

Design Example 1 (cont)

$V_o = 3.3V$ $I_o = 2.5A$ $f_o = 600kH$ $C = 10uF$

$R_1 = 17.4k$ $R_2 = 10k$ $R_3 = 5.36k$

$C_4 = 5.6n$ $C_5 = 180p$

$$R_L = \frac{V_o}{I_o} = 1.32\Omega$$

The power stage control to output transfer function with the current loop closed (Ridley model) for the SC4519 will be as follows:

$$G_{VD}(s) = \frac{2.5 \cdot R_L}{1 + \frac{s}{\frac{1}{R_L \cdot C}}} = \frac{3.3}{1 + \frac{s}{7.6 \cdot 10^4}}$$

The compensation network gives the following characteristics:

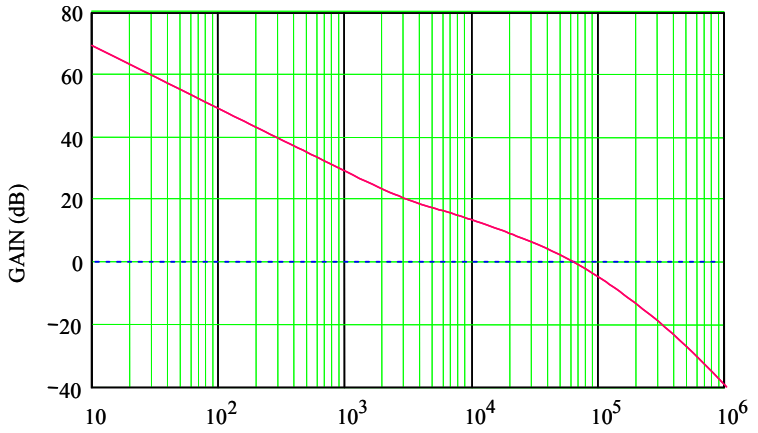
$$G_{COMP}(s) = \omega_1 \cdot \frac{1 + \frac{s}{\omega_Z}}{s \cdot (1 + \frac{s}{\omega_{P2}})} \cdot g_m \cdot \frac{R_2}{R_1 + R_2} =$$

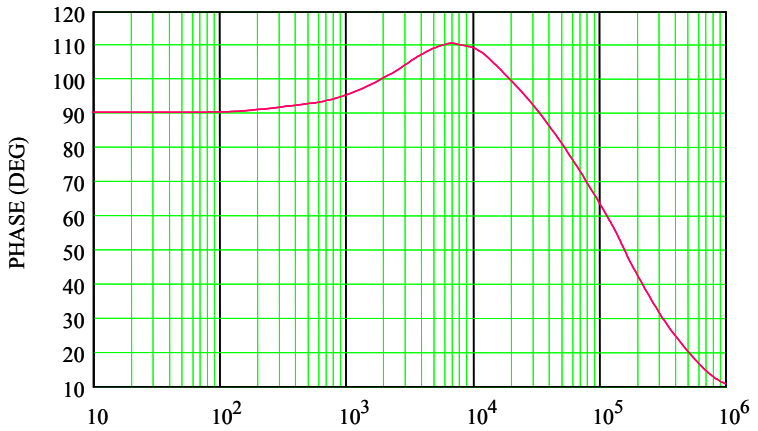
$$5.4 \cdot 10^4 \cdot \frac{1 + \frac{s}{3.3 \cdot 10^4}}{s \cdot (1 + \frac{s}{1.1 \cdot 10^6})}$$

The system loop gain will be given by:

$$T(s) = G_{COMP}(s) \cdot G_{VD}(s) =$$

$$1.8 \cdot 10^5 \cdot \frac{1 + \frac{s}{3.3 \cdot 10^4}}{s \cdot (1 + \frac{s}{1.1 \cdot 10^6}) \cdot (1 + \frac{s}{7.6 \cdot 10^4})}$$





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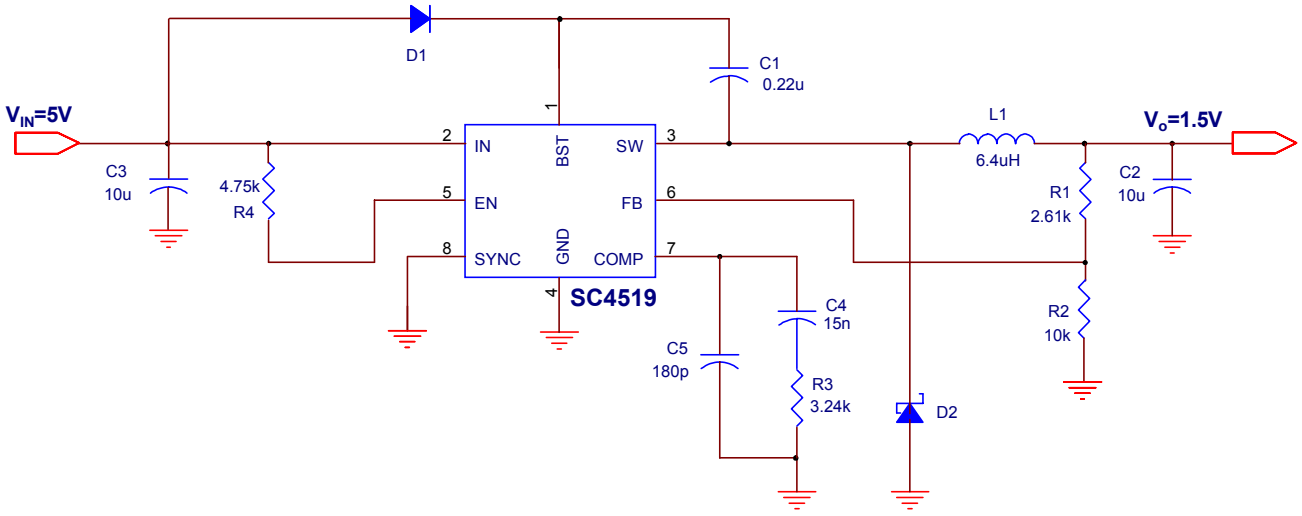
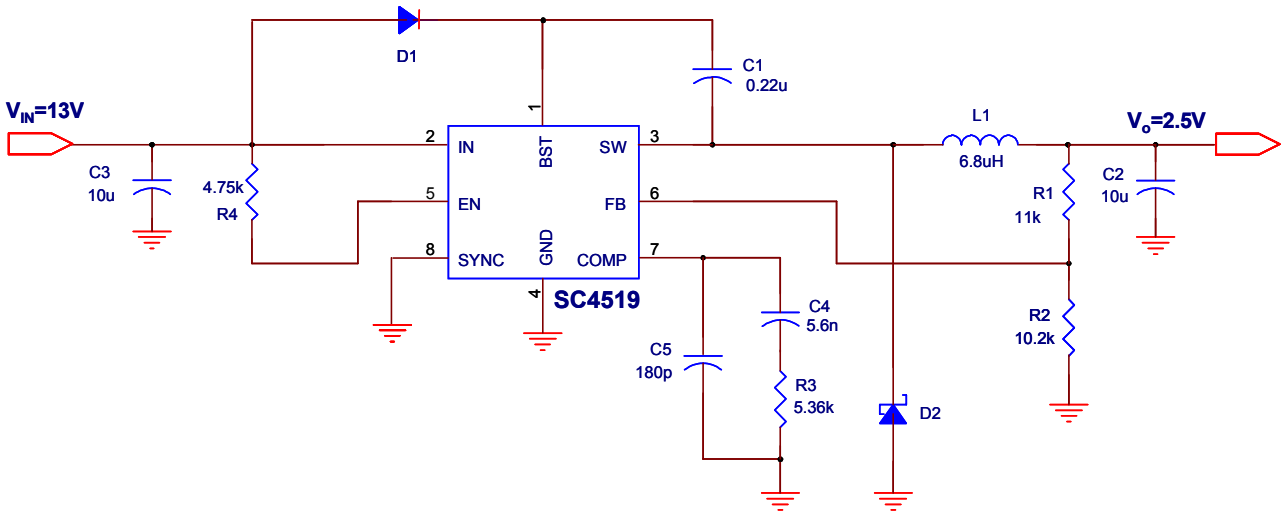
Design Example 2: 5V / 1.5V 2A



Bill of Materials				
Item	**Qty**	**Reference**	**Value**	**Part No./Manufacturer**
1	1	C1	0.22uF, 25V, 0805, X7R	Vishay,
2	2	C2, C3	10u, 1206, 16V, X5R	AVX
3	1	C4	15n, 0805, X7R, 25V	Vishay
4	1	C5	180pF	
5	1	D1	1N4148WS, SOD-323	
6	1	D2	SS33	Fairchild P/N: SS33
7	1	L1	6.4uH	TOKO P/N: 919AS-6R4M
8	1	R1	2.61K	
9	1	R2	10k	
10	1	R3	3.24k	
11	1	R4	4.75k	
12	1	U1	SC4519	Semtech
Unless specified, all resistors have 1% precision with 0603 package. Resistors are +/-1% and all capacitors are +/-20%				

APPLICATION NOTE

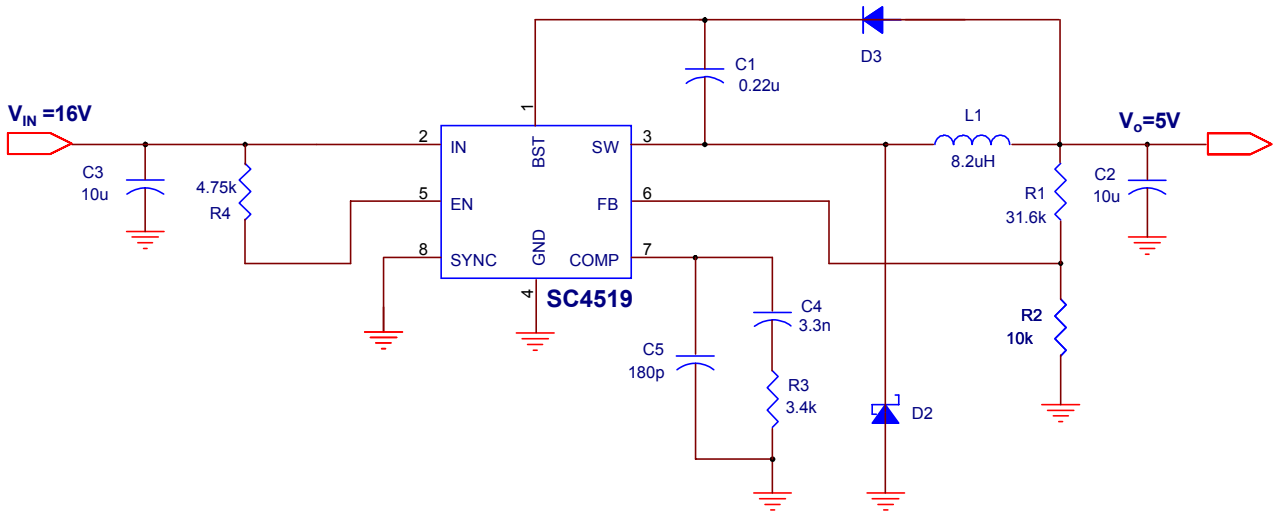
Design Example 3: 13V / 2.5V 2A



Bill of Materials				
Item	**Qty**	**Reference**	**Value**	**Part No./Manufacturer**
1	1	C1	0.22uF, 25V, 0805, X7R	Vishay,
2	2	C2, C3	10u, 1210, X5R, 25V	Panasonic
3	1	C4	5.6n, 0805, X7R, 25V	Vishay
4	1	C5	180pF	
5	1	D1	1N4148WS, SOD-323	
6	1	D2	SS33	Fairchild P/N: SS33
7	1	L1	6.8uH	COOPER P/N:DR125-6R8
8	1	R1	11K	
9	1	R2	10.2k	
10	1	R3	5.36k	
11	1	R4	4.75k	
12	1	U1	SC4519	Semtech
Unless specified, all resistors have 1% precision with 0603 package. Resistors are +/-1% and all capacitors are +/-20%				

APPLICATION NOTE

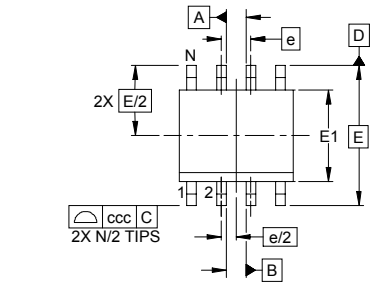
Design Example 4: 16V to 5V 2A

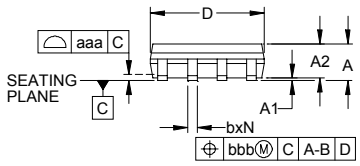


Bill of Materials				
Item	**Qty**	**Reference**	**Value**	**Part No./Manufacturer**
1	1	C1	0.22uF, 25V, 0805, X7R	Vishay
2	2	C2, C3	10u, 1210, X5R, 25V	Panasonic
3	1	C4	3.3n, 0805, X7R, 25V	Vishay
4	1	C5	180pF	
5	1	D1	1N4148WS, SOD-323	
6	1	D2	SS33	Fairchild P/N: SS33
7	1	L1	8.2uH	COOPER P/N:DR125-8R2
8	1	R1	31.6K	
9	1	R2	10k	
10	1	R3	3.4k	
11	1	R4	4.75k	
12	1	U1	SC4519	Semtech
Unless specified, all resistors have 1% precision with 0603 package. Resistors are +/-1% and all capacitors are +/-20%				

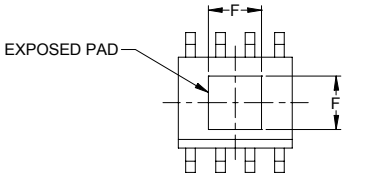
APPLICATION NOTE

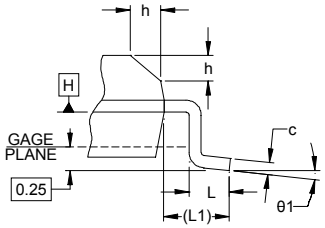
Outline Drawing - SOIC-8L EDP

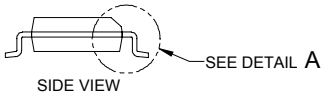




DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
F	.086	.090	.094	2.19	2.29	2.39
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.05)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		



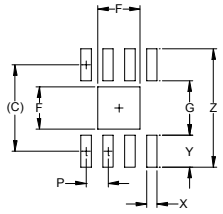




NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - SOIC-8L EDP



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.205)	(5.20)
F	.096	2.44
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

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