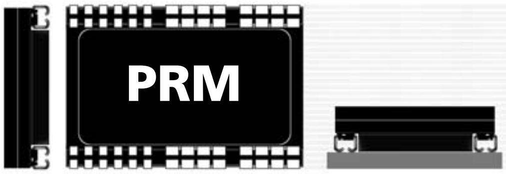
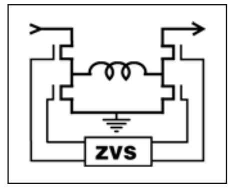


P024F048T12AL

V•I Chip™ – PRM-AL Pre-Regulator Module

- 24 V input V•I Chip PRM
- Vin range 18 – 36 Vdc
- High density – 438 W/in³
- Small footprint – 110 W/in²
- Low weight – 0.5 oz (14 g)
- Adaptive Loop feedback
- ZVS buck-boost regulator
- 1.33 MHz switching frequency
- 95% efficiency
- 125°C operation



©

Vin = 18 – 36 V
V_f = 26 – 55 V
P_f = 120 W
I_f = 2.5 A

Actual size

Product Description

The V•I Chip Pre-Regulator Module (PRM) is a very efficient non-isolated regulator capable of both boosting and bucking a wide range input voltage. It is specifically designed to provide a controlled Factorized Bus distribution voltage for powering downstream V•I Chip Voltage Transformation Modules (VTMs) — fast, efficient, isolated low noise Point-of-Load (POL) converters. In combination, PRMs and VTMs form a complete DC-DC converter subsystem offering all of the unique benefits of Vicor's Factorized Power Architecture (FPA): high density and efficiency; low noise operation; architectural flexibility; extremely fast transient response; and elimination of bulk capacitance at the Point-of-Load (POL).

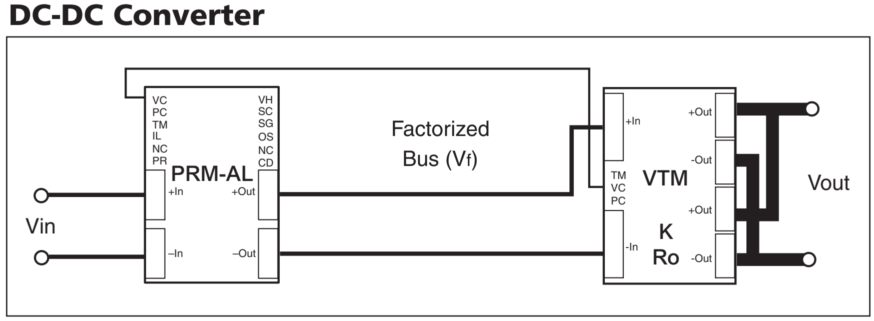
In FPA systems, the POL voltage is the product of the Factorized Bus voltage delivered by a PRM and the "K-factor" (the fixed voltage transformation ratio) of a downstream VTM. The PRM controls the Factorized Bus voltage to provide regulation at the POL. Because VTMs perform true voltage division and current multiplication, the Factorized Bus voltage may be set to a value that is substantially higher than the bus voltages typically found in "intermediate bus" systems, reducing distribution losses and enabling use of narrower distribution bus traces. A PRM-VTM chip set can provide up to 100 A, or 115 W, at a FPA system density of 200 A/in³, or 280 W/in³ — and because the PRM can be located, or "factorized," remotely from the POL, these power densities can effectively be doubled.

The PRM described in this data sheet features a unique "Adaptive Loop" compensation feedback: a single wire alternative to traditional remote sensing and feedback loops that enables precise control of an isolated POL voltage without the need for either a direct connection to the load or for noise sensitive, bandwidth limiting, isolation devices in the feedback path.

Absolute Maximum Ratings

Parameter		Values	Unit
+In to -In		-1.0 to 60.0	Vdc
PC to -In		-0.3 to 6.0	Vdc
PR to -In		-0.3 to 9.0	Vdc
IL to -In		-0.3 to 6.0	Vdc
VC to -In		-0.3 to 18.0	Vdc
+Out to -Out		-0.3 to 59	Vdc
SC to -Out		-0.3 to 3.0	Vdc
VH to -Out		-0.3 to 9.5	Vdc
OS to -Out		-0.3 to 9.0	Vdc
CD to -Out		-0.3 to 9.0	Vdc
SG to -Out		100	mA
Continuous output current		2.5	Adc
Continuous output power		120	W
Operating junction temperature	(M-Grade)	-55 to 125	°C
	(T-Grade)	-40 to 125	°C
Storage temperature	(M-Grade)	-65 to 125	°C
	(T-Grade)	-40 to 125	°C
Case temperature during reflow:		208	°C

DC-DC Converter



The P024F048T12AL is used with any 048 input series VTM to provide a regulated and isolated output.

Part Numbering

P	024	F	048	T	12	AL
Pre-Regulator Module	Input Voltage Designator	Configuration (Fig.21)	Nominal Factorized Bus Voltage	Product Grade Temperatures (°C) Grade / Storage / Operating T: -40 to125 / -40 to125 M: -65 to125 / -55 to125	Output Power Designator (=P_f /10)	AL = Adaptive Loop

Overview of Adaptive Loop Compensation

Adaptive Loop compensation, illustrated in Figure 1, contributes to the bandwidth and speed advantage of Factorized Power. The PRM monitors its output current and automatically adjusts its output voltage to compensate for the voltage drop in the output resistance of the VTM. R_{OS} sets the desired value of VTM output voltage, Vout; R_{CD} is set to a value that compensates for the output resistance of the VTM (which, ideally, is located at the point of load). For selection of R_{OS} and R_{CD}, refer to Table 1 below or Page 9.

The V•I Chip's bi-directional VC port :

1. Provides a wake up signal from the PRM to the VTM that synchronizes the rise of the VTM output voltage to that of the PRM.
2. Provides feedback from the VTM to the PRM to enable the PRM to compensate for the voltage drop in VTM output resistance, R_O.

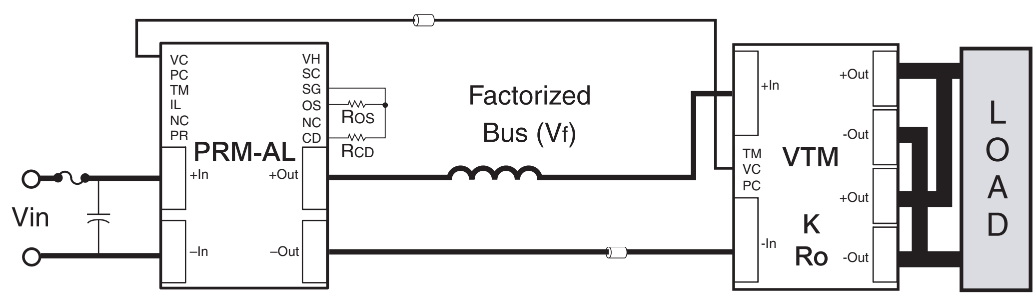


Figure 1 — With Adaptive Loop control the output of the VTM is regulated over the load current range with only a single interconnect between the PRM and VTM and without the need for isolation in the feedback path.

Desired Load Voltage (Vdc)	VTM P/N(1)	Max VTM Output Current (A)(2)	R_{OS} (kΩ)(3)	R_{CD} (Ω)(3)
1.0	V048F015T100	100	3.57	26.1
1.2	V048F015T100	100	2.94	32.4
1.5	V048F015T100	100	2.37	39.2
1.8	V048F020T080	80	2.61	35.7
2.0	V048F020T080	80	2.37	39.2
3.3	V040F033T060	60	2.89	32.6
5.0	V048F060T040	40	2.87	33.2
10	V048F120T025	25	2.86	32.9
12	V048F120T025	25	2.37	39.2
15	V048F160T019	18.8	2.49	37.4
24	V048F240T012	12.5	2.37	39.2
28	V048F320T009	9.4	2.74	35.7
36	V048F480T006	6.3	3.16	30.1
48	V048F480T006	6.3	2.37	39.2

Note:
(1) Verify the product grade temperature before ordering as shown above.
(2) See "PRM output power vs. VTM output power" on Page 10
(3) 1% precision resistors recommended

***Table 1** — Configure your Chip Set using the PRM-AL*

Input Specs (Conditions are at 24 Vin, 48 Vf, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Input voltage range	18	24	36	Vdc	
Input dV/dt			1	V/µs	
Input undervoltage turn-on		15.0	15.7	Vdc	Increases as temp. increases to 16.5 max
Input undervoltage turn-off	13.5	14.1		Vdc	
Input overvoltage turn-on	36.3	37.1		Vdc	
Input overvoltage turn-off		37.8	38.9	Vdc	
Input quiescent current		0.5	1	mA	PC low
Input current		2.6		Adc	
Input reflected ripple current		284		mA p-p	See Figures 4 & 5
No load power dissipation		3.82	7.65	W	
Internal input capacitance		5		µF	Ceramic
Recommended external input capacitance		3,300		µF	See Figure 5 for input filter circuit. Source impedance dependent

Input Waveforms

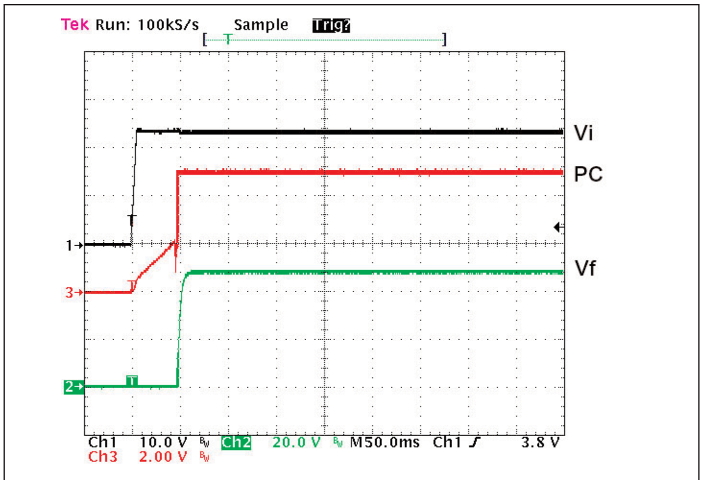


Figure 2 — Vf and PC response from power up

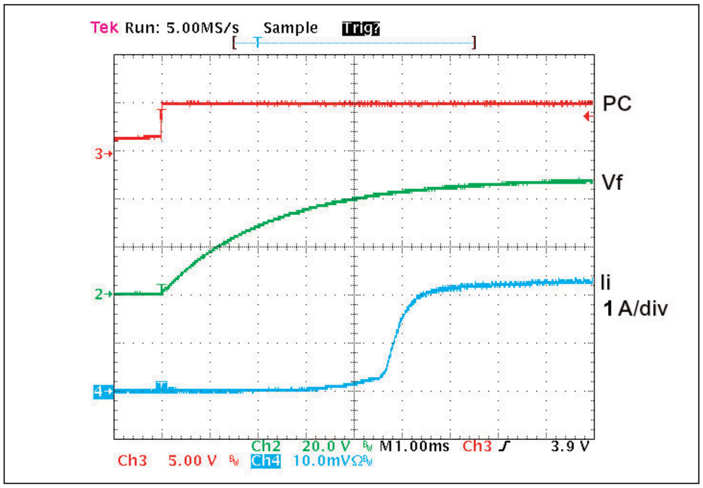


Figure 3 — Vf turn-on waveform with inrush current – PC enabled at full load, 24 Vin, electronic load set constant R

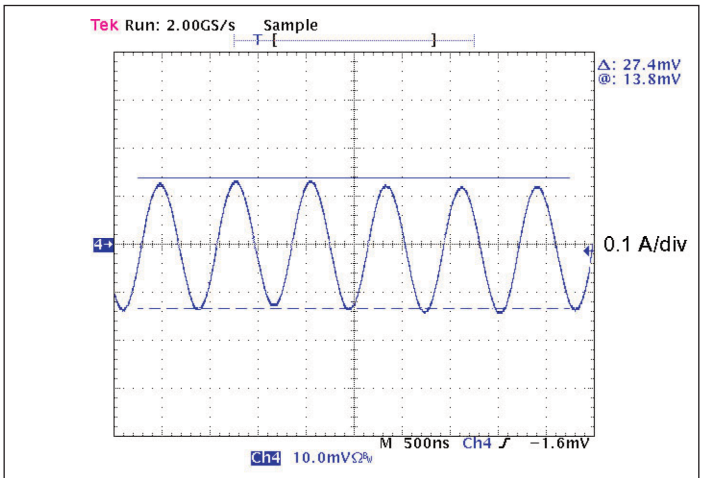


Figure 4 — Input reflected ripple current at full load and 24 Vin

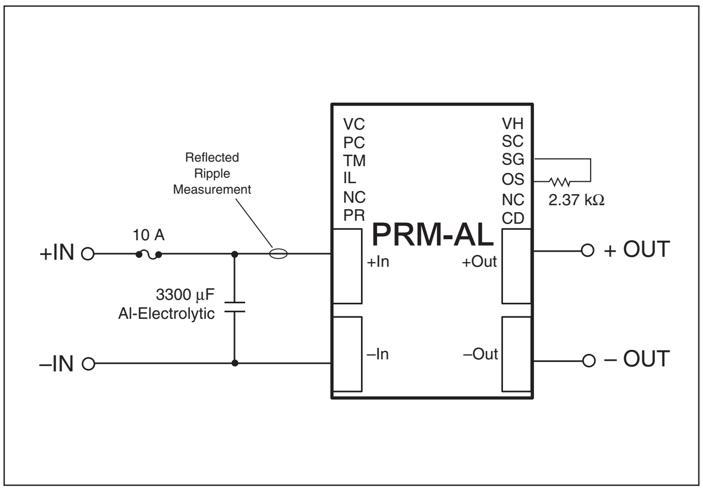


Figure 5 — Input filter capacitor recommendation

Output Specs (Conditions are at 24 Vin, 48 Vf, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Output voltage range	26	48	55	Vdc	Factorized Bus voltage (Vf) set by R_{OS}
Output power	0		120	W	
Output current	0		2.5	Adc	
DC current limit	2.6	3.0	3.3	Adc	I_L pin floating
Average short circuit current			0.5	A	Auto recovery
Set point accuracy		1.5		%	
Line regulation		0.1	0.2	%	Low line to high line
Load regulation		0.1	0.2	%	No CD resistor
Load regulation (at VTM output)		1.0	2.0	%	Adaptive Loop
Current share accuracy		5	10	%	
Efficiency					
Full load		95		%	See Figure 6,7 & 8
Output overvoltage set point	56		59.4	Vdc	
Output ripple voltage					
No external bypass		1.0	2.0	%	Factorized Bus, see figure 13
With 10 µF capacitor		0.5	1.0	%	Factorized Bus, see figure 14
Switching frequency	1.24	1.33	1.45	MHz	Fixed frequency
Output turn-on delay					
From application of power		55	105	ms	See Figure 2
From PC pin high		100		µs	See Figure 3, consult Applications Engineering if powering loads other than VTMs.
Internal output capacitance		5		µF	Ceramic
Factorized Bus capacitance			47	µF	

Efficiency Graphs

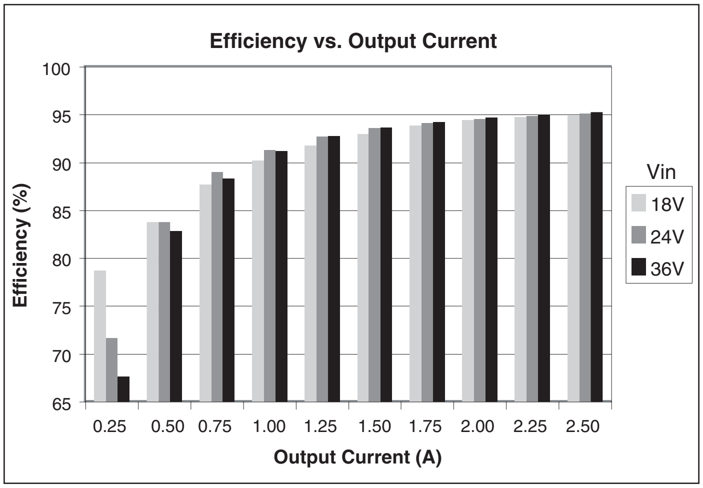


Figure 6 — *Efficiency vs. output current at 48 Vf*

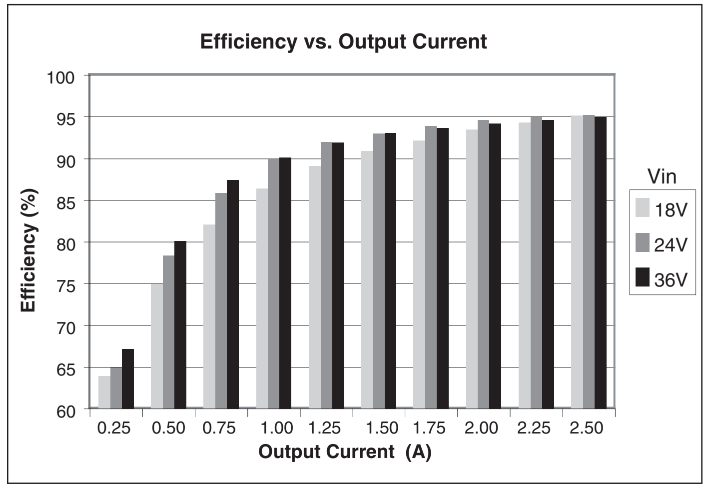


Figure 7 — *Efficiency vs. output current at 36 Vf*

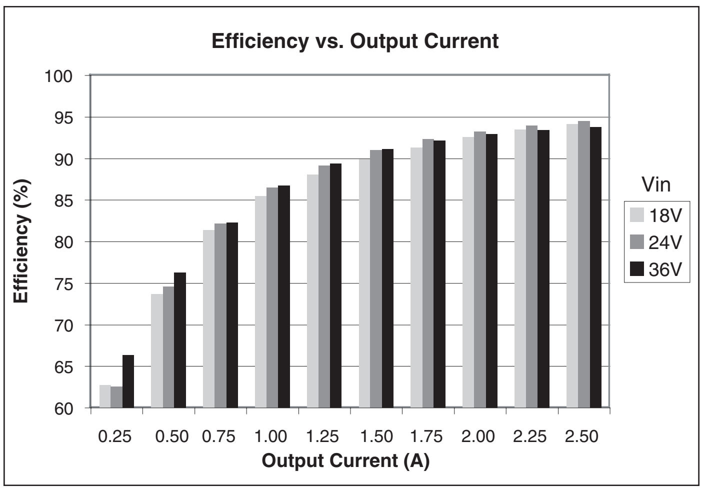


Figure 8 — *Efficiency vs. output current at 26 Vf*

Output Waveforms

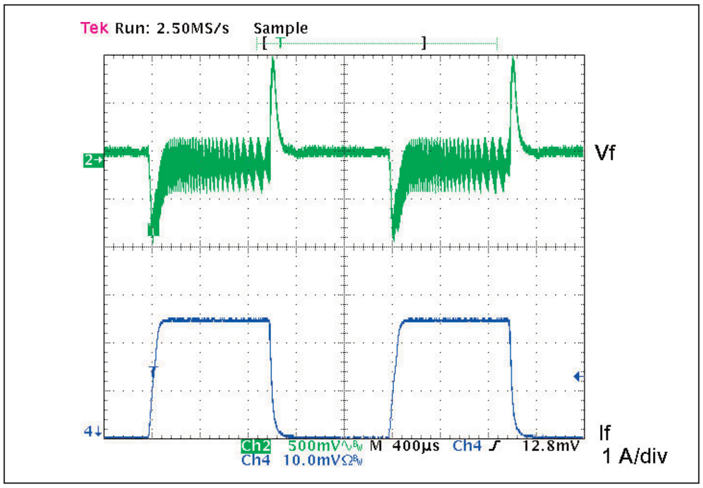


Figure 9 *— Transient response; PRM alone, 24 Vin, 0 – 2.5 – 0 A no load capacitance. Local Loop*

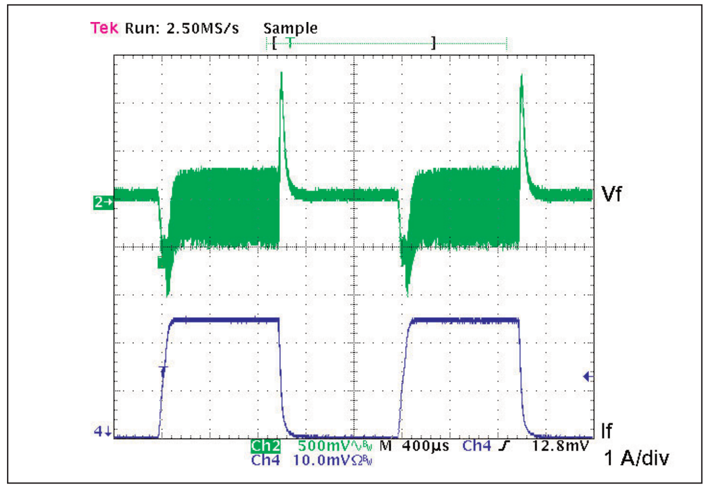


Figure 10 *— Transient response; PRM alone, 18 Vin, 0 – 2.5 – 0 A no load capacitance. Local Loop*

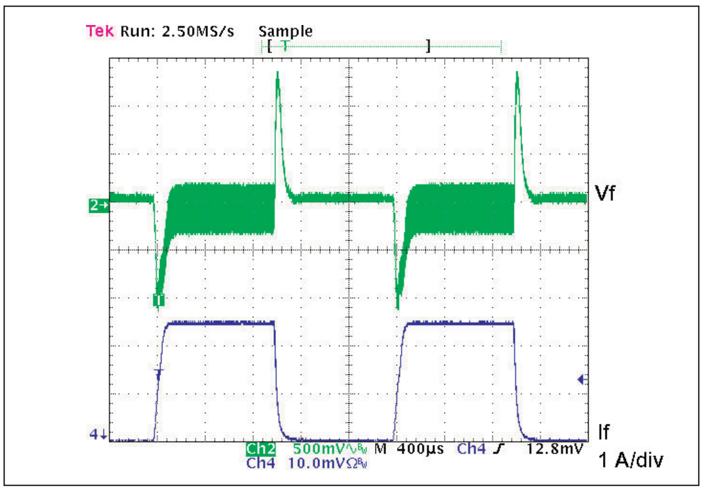


Figure 11 *— Transient response; PRM alone, 36 Vin, 0 – 2.5 – 0 A no load capacitance. Local Loop*

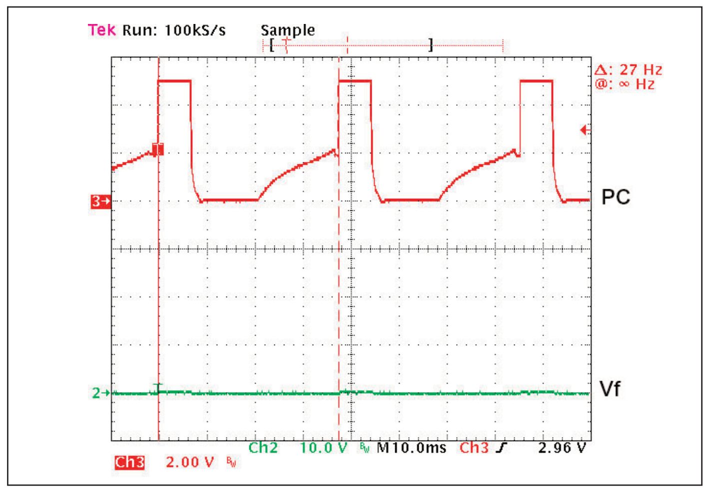


Figure 12 *— PC during fault – frequency will vary as a function of line voltage.*

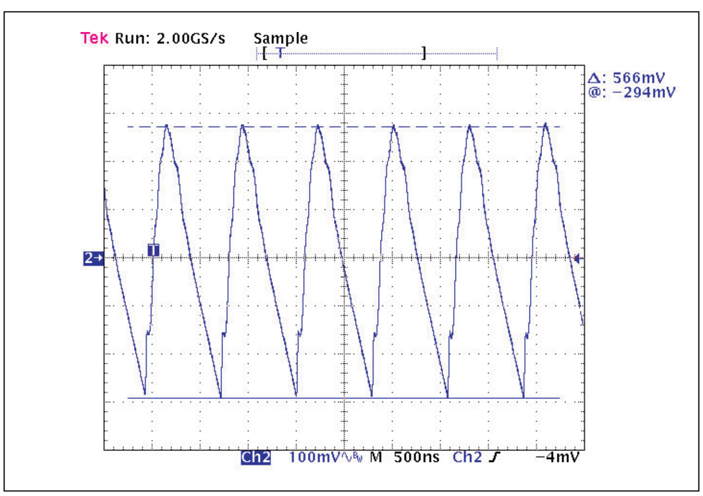


Figure 13 *— Output ripple full load no bypass capacitance.*

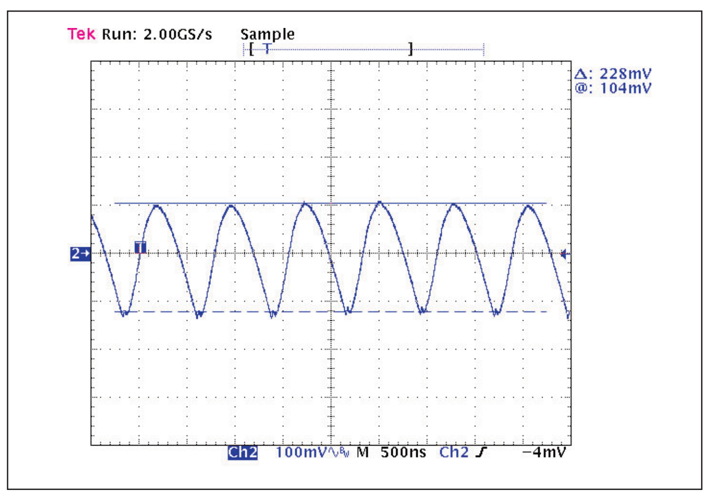


Figure 14 *— Output ripple full load 10 µF bypass capacitance.*

Auxiliary Pins (Conditions are at 24 Vin, 48 Vf, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
VC (VTM Control)					
Peak voltage		14	18	V	Referenced to –Out
PC (Primary Control)					
DC voltage	4.8	5.0	5.2	Vdc	Referenced to –IN
Module disable voltage	2.3	2.4		Vdc	Referenced to –IN
Module enable voltage		2.5	2.6	Vdc	
Disable hysteresis		100		mV	
Current limit		1.75	1.90	mA	Source only after start up; not to be used for aux. supply; 100 kΩ minimum load impedance to assure start up.
Enable delay time		100		µs	
Disable delay time		1		µs	
IL (Current Limit Adjust)					
Voltage	0.95	1	1.05	V	
Accuracy		± 15		%	Based on DC current limit set point
PR (Parallel Port)					
Voltage	1.5		3	V	Referenced to SG
Source current	1			mA	
External capacitance			100	pF	
VH (Auxiliary Voltage)					
Range	8.7	9.0	9.3	Vdc	Maximum source = 5 mA, referenced to SG
Regulation		0.04		%/mA	
SC (Secondary Control)					
Voltage	1.22	1.24	1.25	Vdc	Referenced to SG
Internal capacitance		0.1		µF	
External capacitance			0.7	µF	
OS (Output Set)					
Set point accuracy		± 1.5		%	Includes 1% external resistor
Reference offset		± 4		mV	
CD (Compensation Device)					
External resistance	20			Ω	Omit resistor for regulation at output of PRM

General Specs

Parameter	Min	Typ	Max	Unit	Note
MTBF					
MIL-HDBK-217F		2.2		Mhrs	25°C, GB
Agency approvals (pending)		cTÜVus			UL/CSA 60950, EN60950
		CE Mark			Low voltage directive
Mechanical parameters					See mechanical drawing, Figures 17 and 19
Weight		0.5 / 14		oz / g	
Dimensions					
Length		1.26 / 32		in / mm	
Width		0.85 / 21.5		in / mm	
Height		0.23 / 5.9		in / mm	
Thermal					
Over temperature shutdown	125	130	135	°C	Junction temperature
Thermal capacity		0.61		Ws/°C	
Junction-to-case thermal impedance ($R_{\theta JC}$)		1.1		°C/W	
Junction-to-board thermal impedance ($R_{\theta JB}$)		2.1		°C/W	
Junction-to-ambient (1) ($R_{\theta JA}$)		6.5		°C/W	
Junction-to-ambient (2) ($R_{\theta JA}$)		5.0		°C/W	

Notes:

(1) Surface mounted to a 2" x 2" FR4 board, 4 layers 2 oz Cu, 300 LFM.

(2) With a 0.25"H heatsink surface mounted on FR4 board, 300 LFM.

+IN / -IN DC Voltage Ports

The V•I Chip maximum input voltage should not be exceeded. PRMs have internal over / undervoltage lockout functions that prevent operation outside of the specified input range. PRMs will turn on when the input voltage rises above its undervoltage lockout. If the input voltage exceeds the overvoltage lockout, PRMs will shut down until the overvoltage fault clears. PC will toggle indicating an out of bounds condition.

+OUT / -OUT Factorized Voltage Output Ports

These ports provide the Factorized Bus voltage output. The –OUT port is connected internally to the –IN port through a current sense resistor. The PRM has a maximum power and a maximum current rating and is protected if either rating is exceeded. Do not short –OUT to –IN.

VC – VTM Control

The VTM Control (VC) port supplies an initial V_{CC} voltage to downstream VTMs, enabling the VTMs and synchronizing the rise of the VTM output voltage to that of the PRM. The VC port also provides feedback to the PRM to compensate for voltage drop due to the VTM output resistance. The PRM's VC port should be connected to the VTM VC port. A PRM VC port can drive a maximum of two (2) VTM VC ports.

PC – Primary Control

The PRM voltage output is enabled when the PC pin is open circuit (floating). To disable the PRM output voltage, the PC pin is pulled low. Open collector optocouplers, transistors, or relays can be used to control the PC pin. When using multiple PRMs in a high power array, the PC ports must be tied together to synchronize their turn on. During an abnormal condition the PC pin will pulse (Fig.12) as the PRM initiates a restart cycle. This will continue until the abnormal condition is rectified. The PC should not be used as an auxiliary voltage supply, nor should it be switched at a rate greater than 1 Hz.

TM – Factory Use Only

IL – Current Limit Adjust

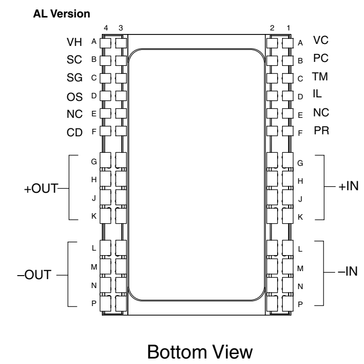
The PRM has a preset, maximum, current limit set point. The IL port may be used to reduce the current limit set point to a lower value. See "Adjusting Current Limits" on page 10.

PR – Parallel Port

The PR port signal, which is proportional to the PRM output power, supports current sharing among PRMs. To enable current sharing, PR ports should be interconnected. Bypass capacitance should be used when interconnecting PR ports and steps should be taken to minimize coupling noise into the interconnecting bus. Please consult Vicor Applications Engineering regarding additional considerations.

VH – Auxiliary Voltage

VH is a gated, non-isolated, nominally 9 Volt, regulated DC voltage (see "Auxiliary Pins" specifications, on Page 7) that is referenced to SG. VH may be used to power external circuitry having a total current consumption of no more than 5 mA.



Signal Name	Designation
+IN	G1-K1,G2-K2
–IN	L1-P1, L2-P2
VC	A1,A2
PC	B1, B2
TM	C1, C2
IL	D1, D2
PR	F1, F2
VH	A3, A4
SC	B3, B4
SG	C3, C4
OS	D3, D4
CD	F3, F4
+OUT	G3-K3, G4-K4
–OUT	L3-P3, L4-P4

***Figure 15** — PRM pin configuration*

SC – Secondary Control

The load voltage may be controlled by connecting a resistor or voltage source to the SC port referenced to SG. The slew rate of the output voltage may be controlled by controlling the rate-of-rise of the voltage at the SC port (e.g., to limit inrush current into a capacitive load).

SG – Signal Ground

This port provides a low inductance Kelvin connection to –IN and should be used as reference for the OS, CD, SC,VH and IL ports.

OS – Output Set

The application-specific value of the Factorized Bus voltage (Vf) is set by connecting a resistor between OS and SG. Resistor value selection is shown in Table 1 on Page 2, and described on Page 9. If no resistor is connected, the PRM output will be approximately one volt. If set resistor is not collocated with the PRM, a local bypass capacitor of ~200 pF may be required.

CD – Compensation Device

Adaptive Loop control is configured by connecting an external resistor between the CD port and SG. Selection of an appropriate resistor value (see Equation 2 on Page 9 and Table 1 on Page 2) configures the PRM to compensate for voltage drops in the equivalent output resistance of the VTM and the PRM-VTM distribution bus. If no resistor is connected to CD, the PRM will be in Local Loop mode and will regulate the +OUT / –OUT voltage to a fixed value.

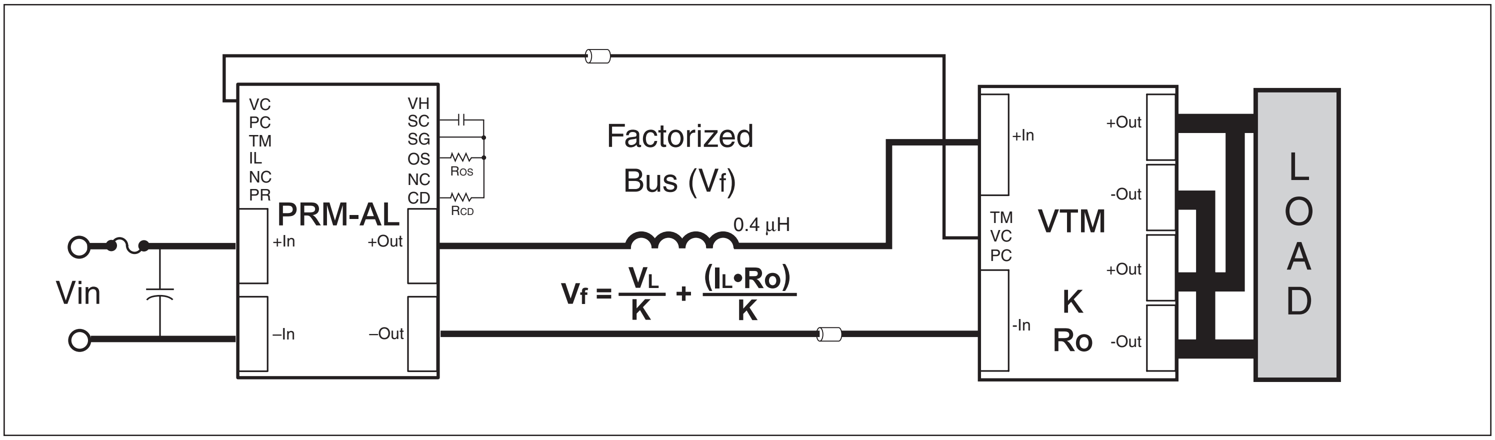


Figure 16 — Adaptive Loop compensation with soft start using the SC port.

Output Voltage Setting with Adaptive Loop

The equations for calculating R_{OS} and R_{CD} to set a VTM output voltage are:

$$R_{OS} = \frac{93100}{\left(\frac{V_L \bullet 0.8395}{K}\right) - 1} \quad (1)$$

$$R_{CD} = \frac{91238}{R_{OS}} + 1 \quad (2)$$

V_L = Desired load voltage

V_{OUT} = VTM output voltage

K = VTM transformation ratio (available from appropriate VTM data sheet)

V_f = PRM output voltage, the Factorized Bus (see Figure 16)

R_O = VTM output resistance (available from appropriate VTM data sheet)

I_L = Load Current (actual current delivered to the load)

Output Voltage Trimming (optional)

After setting the output voltage from the procedure above the output may be margined down (26Vf min) by a resistor from SC-SG using this formula:

$$R_d\Omega = \frac{10000\ V_{fd}}{V_{fs} - V_{fd}}$$

Where V_{fd} is the desired factorized bus and V_{fs} is the set factorized bus.

A low voltage source can be applied to the SC port to margin the load voltage in proportion to the SC reference voltage.

An external capacitor can be added to the SC port as shown in Figure 16 to control the output voltage slew rate for soft start.

Nominal Vout Range (Vdc)	VTM K Factor
0.8 ↔ 1.6	1/32
1.1 ↔ 2.2	1/24
1.6 ↔ 3.3	1/16
2.2 ↔ 4.4	1/12
3.3 ↔ 6.6	1/8
4.3 ↔ 8.8	1/6
6.5 ↔ 13.4	1/4
8.7 ↔ 17.9	1/3
13.0 ↔ 26.9	1/2
17.4 ↔ 36.0	2/3
26.0 ↔ 54.0	1

Table 2 — 048 input series VTM K factor selection guide

OVP – Overvoltage Protection

The output Overvoltage Protection set point of the P048F048T24AL is factory preset for 56 V. If this threshold is exceeded the output shuts down and a restart sequence is initiated. If the condition that causes OVP is still present, the unit will again shut down. This cycle will be repeated until the fault condition is removed. The OVP set point may be set at the factory to meet unique high voltage requirements.

PRM output power versus VTM output power

As shown in Figure 17 the P024F048T12AL is rated to deliver 2.5 A maximum, when it is delivering an output voltage in the range from 26 V to 48 V, and 120 W, maximum, when delivering an output voltage in the range from 48 V to 55 V. When configuring a PRM for use with a specific VTM, refer to the appropriate VTM data sheet. The VTM input power can be calculated by dividing the VTM output power by the VTM efficiency (available from the VTM data sheet). The input power required by the VTM should not exceed the output power rating of the PRM.

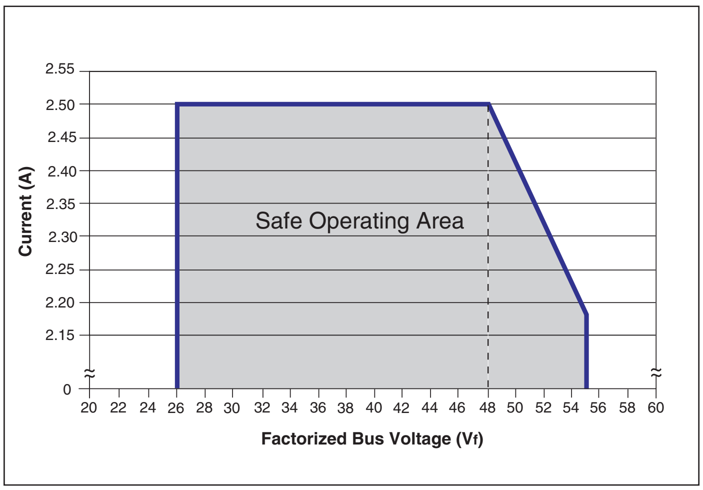


***Figure 17** — P024F048T12AL rating based on Factorized Bus voltage*

The Factorized Bus voltage should not exceed an absolute limit of 55 V, including steady state, ripple and transient conditions. Exceeding this limit may cause the internal OVP set point to be exceeded.

Parallel considerations

The PR port is used to connect two or more PRMs in parallel to form a higher power array. When configuring arrays, PR port interconnection bypass capacitance must be used at ~1nF per PRM. Additionally one PRM should be designated as the master while all other PRMs are set as slaves by shorting their SC pin to SG. The PC pins must be directly connected (no diodes) to assure a uniform start up sequence. The factorized bus should be connected in parallel as well.

Adjusting current limit

The current limit can be lowered by placing an external resistor between the I_L and SG ports (see figure 18 for resistor values). With the I_L port open-circuit, the current limit is preset to be within the range specified in the output specifications table on Page 4.

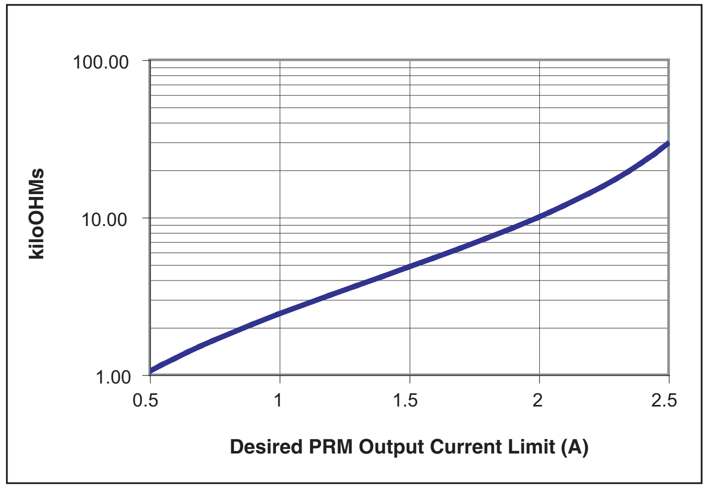


***Figure 18** — External resistor value for adjusting current limit*

Input fuse recommendations

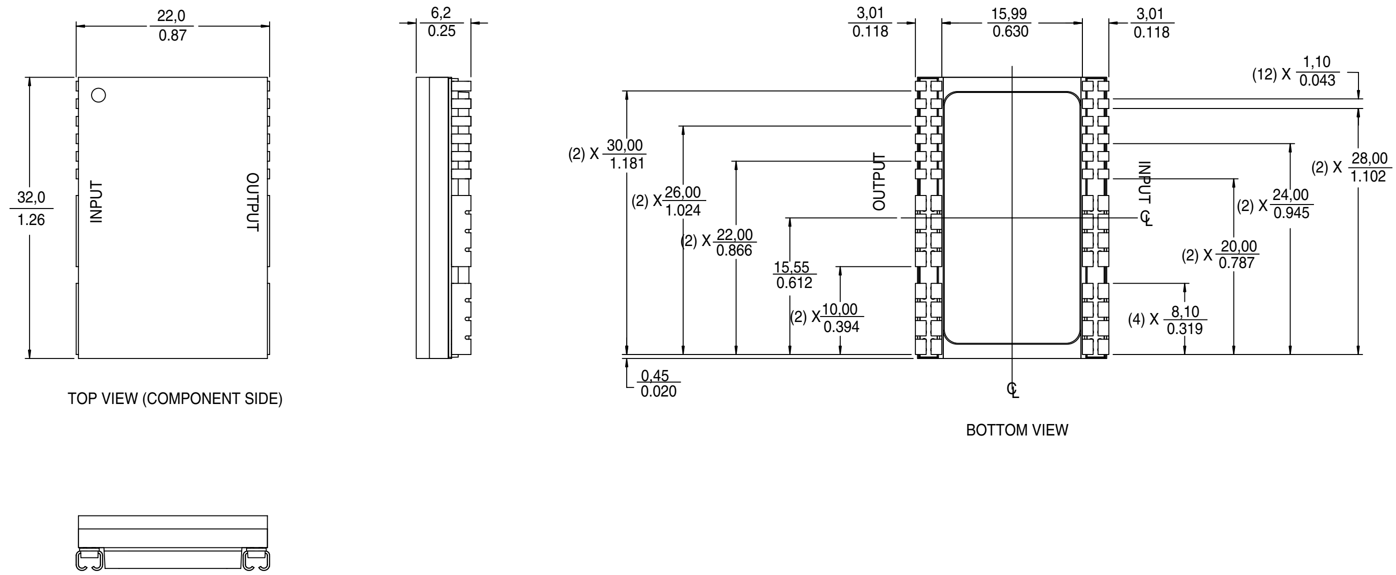
A fuse should be incorporated at the input to the PRM, in series with the +IN port. A fast acting fuse, NANO2 FUSE 451/453 Series 10 A 125 V, or equivalent, may be required to meet certain safety agency Conditions of Acceptability. Always ascertain and observe the safety, regulatory, or other agency specifications that apply to your specific application.

Product safety considerations

If the input of the PRM is connected to SELV or ELV circuits, the output of the PRM can be considered SELV or ELV respectively.

Applications assistance

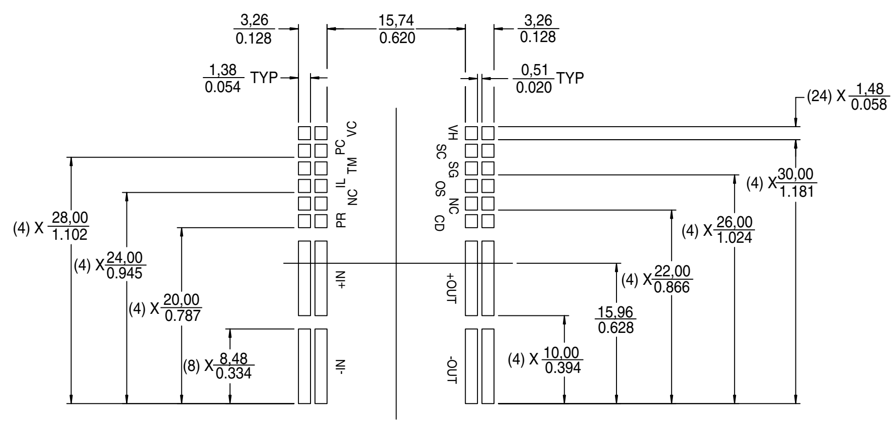
Please contact Vicor Applications Engineering for assistance, 1-800-927-9474, or email at apps@vicr.com.



NOTES:
1- DIMENSIONS ARE mm/inch.
2- UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
.X/[.XX] = +/-0.25/[.01]; .XX/[.XXX] = +/-0.13/[.005]
3- PRODUCT MARKING ON TOP SURFACE

DXF and PDF files are available on vicorpower.com

Figure 19 *—PRM J-Lead mechanical outline; Onboard mounting*



RECOMMENDED LAND PATTERN
(COMPONENT SIDE SHOW)

NOTES:
1- DIMENSIONS ARE mm/inch.
2- UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
.X/[.XX] = +/-0.25/[.01]; .XX/[.XXX] = +/-0.13/[.005]

DXF and PDF files are available on vicorpower.com

Figure 20 *— PRM J-Lead PCB land layout information; Onboard mounting*

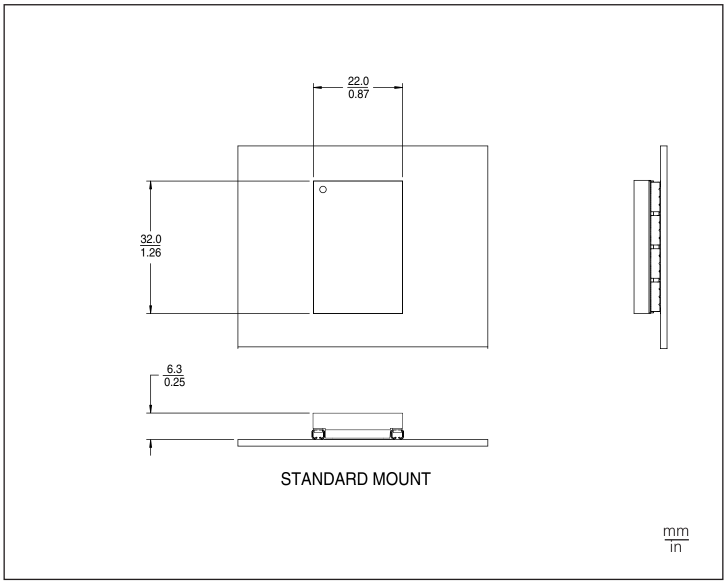


Figure 21 *— Standard mounting – package F*

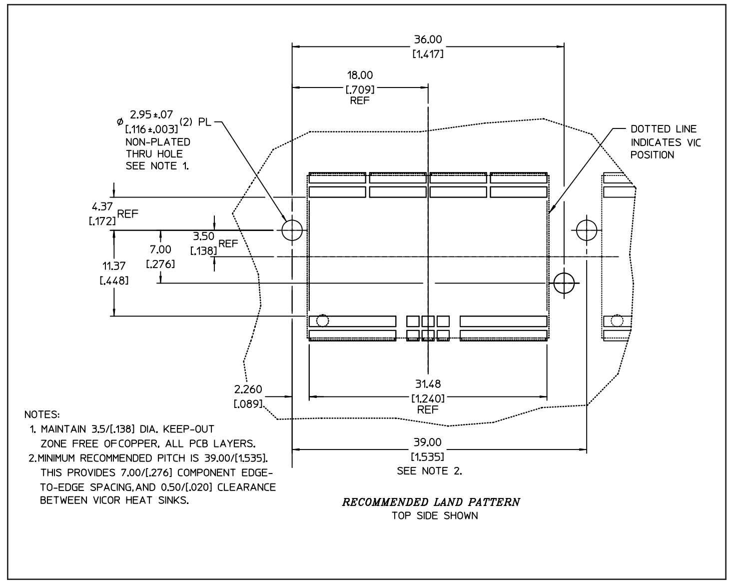


Figure 22 *— Hole location for push pin heatsink relative to VIC*

V•I Chip soldering recommendations

V•I Chip modules are intended for reflow soldering processes. The following information defines the processing conditions required for successful attachment of a V•I Chip to a PCB. Failure to follow the recommendations provided can result in aesthetic or functional failure of the module.

Storage

V•I Chip modules are currently rated at MSL 5. Exposure to ambient conditions for more than 48 hours requires a 24 hour bake at 125ºC to remove moisture from the package.

Solder paste stencil design

Solder paste is recommended for a number of reasons, including overcoming minor solder sphere co-planarity issues as well as simpler integration into overall SMD process.

63/37 SnPb, either no-clean or water-washable, solder paste should be used. Pb-free development is underway.

The recommended stencil thickness is 6 mils. The apertures should be 0.9-0.9:1.

Pick and place

Modules should be placed within ±5 mils.to maintain placement position, the modules should not be subjected to acceleration greater than 500 in/sec² prior to reflow.

Reflow

There are two temperatures critical to the reflow process; the solder joint temperature and the module's case temperature. The solder joint's temperature should reach at least 220ºC, with a time above liquidus (183ºC) of ~30 seconds.

The module's case temperature must not exceed 208 ºC at anytime during reflow.

Because of the ∆T needed between the pin and the case, a forced-air convection oven is preferred for reflow soldering. This reflow method generally transfers heat from the PCB to the solder joint. The module's large mass also reduces its temperature rise. Care should be taken to prevent smaller devices from excessive temperatures. Reflow of modules onto a PCB using Air-Vac-type equipment is not recommended due to the high temperature the module will experience.

Inspection

The J-Lead versions solder joints should conform to IPC 12.2

- Properly wetted fillet must be evident.
- Heel fillet height must exceed lead thickness plus solder thickness.

Removal and rework

V•I Chip modules can be removed from PCBs using special tools such as those made by Air-Vac. These tools heat a very localized region of the board with a hot gas while applying a tensile force to the component (using vacuum). Prior to component heating and removal, the entire board should be heated to 80-100ºC to decrease the component heating time as well as local PCB warping. If there are adjacent moisture-sensitive components, a 125ºC bake should be used prior to component removal to prevent popcorning. V•I Chip modules should not be expected to survive a removal operation.

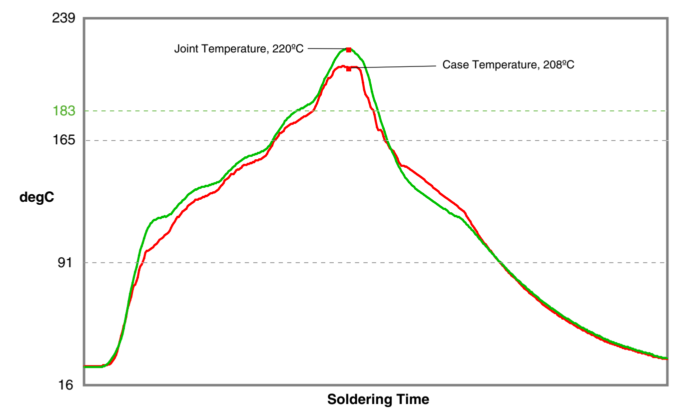


Figure 23 *— Thermal profile diagram*

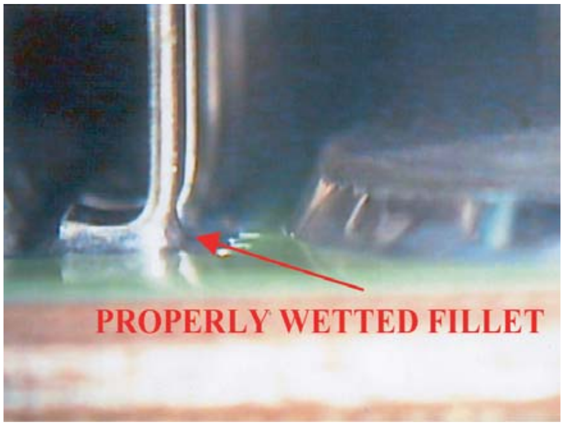


Figure 24 *— Properly reflowed V•I Chip J-Lead*

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