

ACT4060

WIDE INPUT 2A STEP DOWN CONVERTER

FEATURES

- 2A Output Current
- Up to 95% Efficiency
- 4.75V to 20V Input Range
- 8 μ A Shutdown Supply Current
- 360kHz Switching Frequency
- Adjustable Output Voltage from 1.29V to 0.85 \cdot V_{IN}
- Cycle-by-Cycle Current Limit Protection
- Thermal Shutdown Protection
- Frequency Fold Back at Short Circuit
- Stability with Wide Range of Capacitors, Including Low ESR Ceramic Capacitors
- SOP-8 Package

APPLICATIONS

- TFT LCD Monitors
- Portable DVDs
- Car-Powered or Battery-Powered Equipments
- Set-Top Boxes
- Telecom Power Supplies
- DSL and Cable Modems and Routers
- Termination Supplies

GENERAL DESCRIPTION

The ACT4060 is a current-mode step-down DC-DC converter that generates up to 2A output current at 410kHz switching frequency. The device utilizes Active-Semi's proprietary ISOBCD20 process for operation with input voltage up to 20V.

Consuming only 8 μ A in shutdown mode, the ACT4060 is highly efficient with peak efficiency at 95% when in operation. Protection features include cycle-by-cycle current limit, thermal shutdown, and frequency fold back at short circuit.

The ACT4060 is available in SOP-8 package and requires very few external devices for operation.

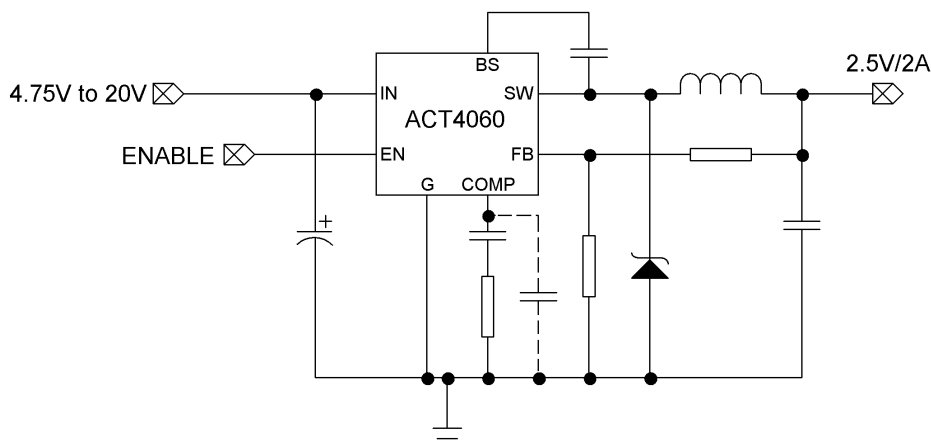
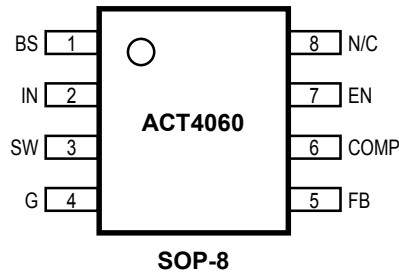


Figure 1. Typical Application Circuit

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS
ACT4060SH	-40°C to 85°C	SOP-8	8

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	BS	Bootstrap. This pin acts as the positive rail for the high-side switch's gate driver. Connect a 10nF between this pin and SW.
2	IN	Input Supply. Bypass this pin to G with a low ESR capacitor. See <i>Input Capacitor</i> in <i>Application Information</i> section.
3	SW	Switch Output. Connect this pin to the switching end of the inductor.
4	G	Ground.
5	FB	Feedback Input. The voltage at this pin is regulated to 1.293V. Connect to the resistor divider between output and ground to set output voltage.
6	COMP	Compensation Pin. See <i>Compensation Technique</i> in <i>Application Information</i> section.
7	EN	Enable Input. When higher than 1.3V, this pin turns the IC on. When lower than 0.7V, this pin turns the IC off. Output voltage is discharged when the IC is off. This pin has a small internal pull up current to a high level voltage when pin is not connected.
8	N/C	Not Connected.

ABSOLUTE MAXIMUM RATINGS

(Note: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

PARAMETER	VALUE	UNIT
IN Supply Voltage	-0.3 to 25	V
SW Voltage	-1 to $V_{IN} + 1$	V
BS Voltage	$V_{SW} - 0.3$ to $V_{SW} + 8$	V
EN, FB, COMP Voltage	-0.3 to 6	V
Continuous SW Current	Internally limited	A
Junction to Ambient Thermal Resistance (θ_{JA})	105	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

ELECTRICAL CHARACTERISTICS

($V_{IN} = 12V$, $T_J = 25^\circ C$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Feedback Voltage	V_{FB}	$4.75V \leq V_{IN} \leq 20V$, $V_{COMP} = 1.5V$	1.267	1.293	1.319	V
High-Side Switch On Resistance	R_{ONH}			0.20		Ω
Low-Side Switch On Resistance	R_{ONL}			4.7		Ω
SW Leakage		$V_{EN} = 0$		0	10	μA
Current Limit	I_{LIM}		2.4	2.85		A
COMP to Current Limit Transconductance	G_{COMP}			1.8		A/V
Error Amplifier Transconductance	G_{EA}	$\Delta I_{COMP} = \pm 10\mu A$		550		$\mu A/V$
Error Amplifier DC Gain	A_{VEA}			4000		V/V
Switching Frequency	f_{SW}		350	410	470	kHz
Short Circuit Switching Frequency		$V_{FB} = 0$		50		kHz
Maximum Duty Cycle	D_{MAX}	$V_{FB} = 1.1V$		90		%
Minimum Duty Cycle		$V_{FB} = 1.4V$			0	%
Enable Threshold Voltage		Hysteresis = 0.1V	0.7	1	1.3	V
Enable Pull Up Current		Pin pulled up to 4.5V typically when left unconnected		1		μA
Supply Current in Shutdown		$V_{EN} = 0$		8	20	μA
IC Supply Current in Operation		$V_{EN} = 3V$, $V_{FB} = 1.4V$		0.7		mA
Thermal Shutdown Temperature		Hysteresis = 10°C		160		°C

APPLICATION INFORMATION

OUTPUT VOLTAGE SETTING

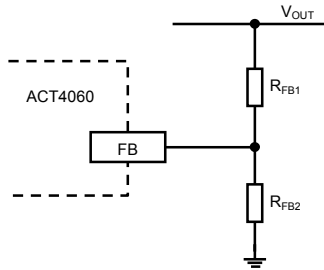


Figure 3. Output Voltage Setting

Figure 3 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Typically, use $R_{FB2} \approx 10\text{k}\Omega$ and determine R_{FB1} from the output voltage:

$$R_{FB1} = R_{FB2} \left(\frac{V_{OUT}}{1.293V} - 1 \right) \quad (1)$$

INDUCTOR SELECTION

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value: higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{OUTMAX} K_{RIPPLE}} \quad (2)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, I_{OUTMAX} is the maximum output current, and K_{RIPPLE} is the ripple factor. Typically, choose $K_{RIPPLE} = 30\%$ to correspond to the peak-to-peak ripple current being 30% of the maximum output current.

With this inductor value (Table 1), the peak inductor current is $I_{OUT} \cdot (1 + K_{RIPPLE} / 2)$. Make sure that this peak inductor current is less than the 3A current limit. Finally, select the inductor core size so that it does not saturate at 3A.

Table 1. Typical Inductor Values

V_{OUT}	1.5V	1.8V	2.5V	3.3V	5V	12V
L	6.8 μH	6.8 μH	10 μH	15 μH	22 μH	47 μH

INPUT CAPACITOR

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10 μF . The best choice is the ceramic type; however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1 μF ceramic capacitor is placed right next to the IC.

OUTPUT CAPACITOR

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{V_{IN}}{28 \cdot f_{SW}^2 L C_{OUT}} \quad (3)$$

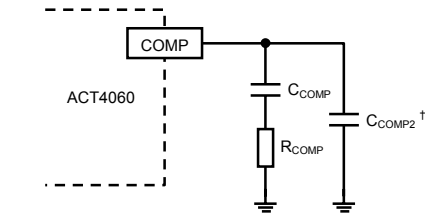
where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR resistance of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic type, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output type, typically choose a capacitance of about 22 μF . For tantalum or electrolytic type, choose a capacitor with less than 50m Ω ESR.

RECTIFIER DIODE

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and the reverse voltage rating higher than the maximum input voltage.

STABILITY COMPENSATION



† C_{COMP2} is needed only for high ESR output capacitor

Figure 4. Stability Compensation

The feedback system of the IC is stabilized by the components at COMP pin, as shown in Figure 4. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{1.3V}{I_{OUT}} A_{VEA} G_{COMP} \quad (4)$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}} \quad (5)$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}} \quad (6)$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP}} \quad (7)$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}} \quad (8)$$

Follow the following steps to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via R_{COMP}:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \cdot 1.3V} = 1.7 \times 10^8 V_{OUT} C_{OUT} \quad (\Omega) \quad (9)$$

but limit R_{COMP} to 15kΩ maximum.

STEP 2. Set the zero f_{Z1} at 1/4 of the cross over frequency. If R_{COMP} is less than 15kΩ, the equation for C_{COMP} is:

$$C_{COMP} = \frac{1.8 \times 10^{-5}}{R_{COMP}} \quad (F) \quad (10)$$

If R_{COMP} is limited to 15kΩ, then the actual cross over frequency is 3.4 / (V_{OUT}C_{OUT}). Therefore:

$$C_{COMP} = 1.2 \times 10^{-5} V_{OUT} C_{OUT} \quad (F) \quad (11)$$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:

$$R_{ESRCOUT} \geq \text{Min} \left(\frac{1.1 \times 10^{-6}}{C_{OUT}}, 0.012 \cdot V_{OUT} \right) \quad (\Omega) \quad (12)$$

And the proper value for C_{COMP2} is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}} \quad (13)$$

Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects.

Table 2 shows some calculated results based on the compensation method above.

Table 2. Typical Compensation for Different Output Voltages and Output Capacitors

V _{OUT}	C _{OUT}	R _{COMP}	C _{COMP}	C _{COMP2}
2.5V	22μF Ceramic	8.2kΩ	2.2nF	None
3.3V	22μF Ceramic	12kΩ	1.5nF	None
5V	22μF Ceramic	15kΩ	1.5nF	None
12V	22μF Ceramic	15kΩ	3.3nF	None
2.5V	47μF SP Cap	15kΩ	1.5nF	None
3.3V	47μF SP Cap	15kΩ	1.8nF	None
5V	47μF SP Cap	15kΩ	2.7nF	None
12V	47μF SP Cap	15kΩ	6.8nF	None
2.5V	470μF/6.3V/30mΩ	15kΩ	15nF	1nF
3.3V	470μF/6.3V/30mΩ	15kΩ	22nF	1nF
5V	470μF/10V/30mΩ	15kΩ	27nF	None
12V	220μF/25V/30mΩ	15kΩ	33nF	None

Figure 5 shows a sample ACT4060 application circuit generating 2.5V/2A output.

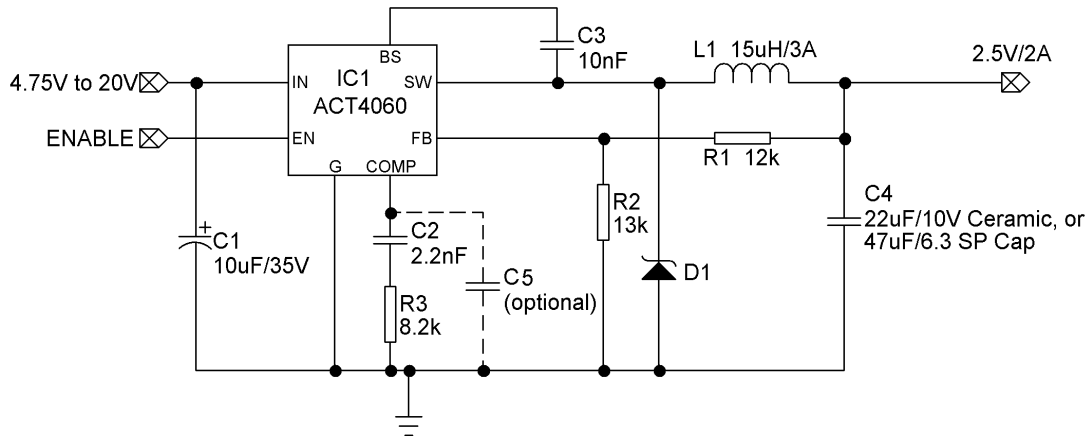
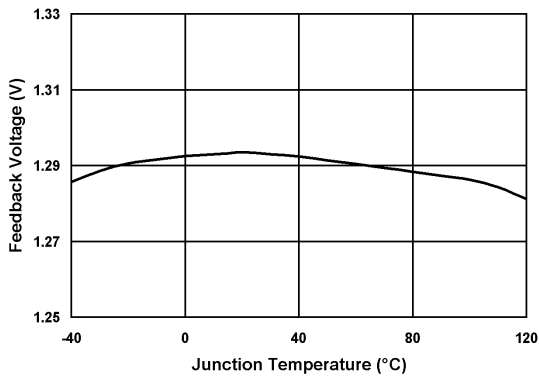


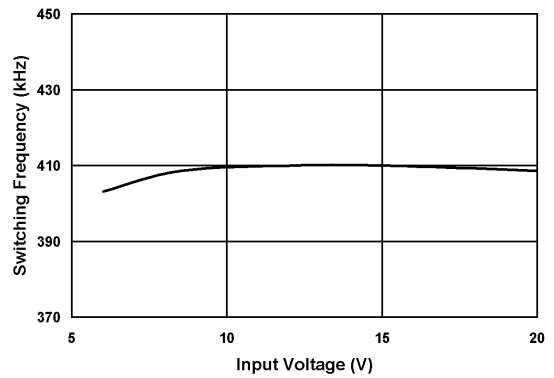
Figure 5. ACT4060 2.5V/2A Output Application

TYPICAL PERFORMANCE CHARACTERISTICS

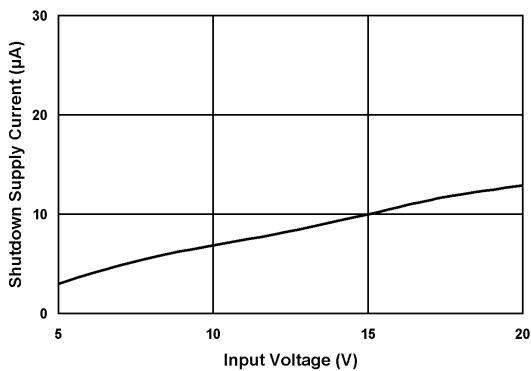
Feedback Voltage vs. Junction Temperature



Switching Frequency vs. Input Voltage

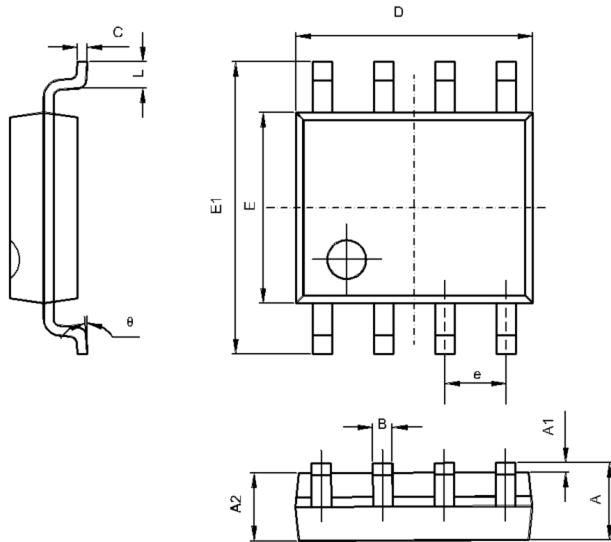


Shutdown Supply Current vs. Input Voltage



PACKAGE OUTLINE

SOP-8 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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44081 Old Warm Springs Blvd, Fremont, California 94538, USA