FS3332<Preliminary>

2 cell Lithium-ion/Polymer Battery Protection IC

General Description

The FS3332 Series are protection ICs for 2-serial-cell lithium-ion/lithium-polymer rechargeable batteries and include high-accuracy voltage detectors and delay circuits.

These ICs are suitable for protecting 2-cell rechargeable lithium-ion/lithium-polymer battery packs from overcharge, overdischarge, and over-current.

Features

- **Low supply current**
  Normal Operation : 7.5 μA typ. 14.2 μA max.
  Power-down mode : 0.1 μA max.
- **Overcharge detection voltage**
  〔VOCU〕 3.90V~4.60V, Accuracy of ±25mV
- **Overcharge release voltage**
  〔VOCR〕 3.60V~4.60V, Accuracy of ±50mV
- **Over-discharge detection voltage**
  〔VODL〕 1.70V~2.60V, Accuracy of ±80mV
- **Over-discharge release voltage**
  〔VODR〕 1.70V~3.80V, Accuracy of ±100mV
- **Over current detection voltage**
  〔VOI1〕 0.07V~0.30V, Accuracy of ±20mV
- **Short circuit detection voltage**
  〔VOI2〕 Fixed at 1.2V
- **Delay times are set by an external capacitor. Each delay time for Overcharge detection, Over-discharge detection, Over-current detection are "Proportion of hundred of ten to one"**
- **Two over-current detection levels (protection for short-circuit)**
- **Internal auxiliary over voltage detection circuit (Fail safe for over voltage)**
- **Internal charge circuit for 0 V battery (Unavailable is option)**
- **High-withstanding-voltage devices Absolute maximum rating: 18 V**
- **Wide operating temperature range -40 to +85°C**
- **Wide supply voltage range 2.0 ~ 16V**
- **8-pin TSSOP package**

Ordering Information

FS3332 **x**
└── Serial code *

*: Refer to the product name list on next page.

Applications

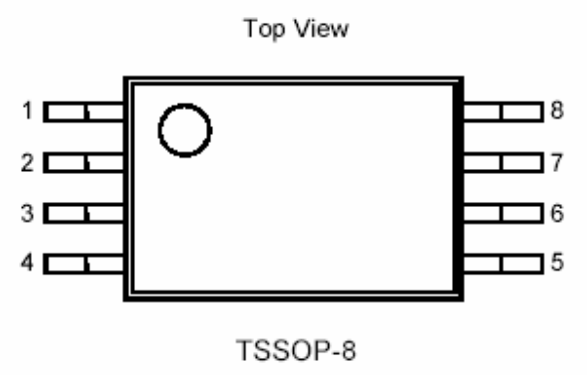
- **Protection IC for 2-Cell Lithium-Ion / Lithium-Polymer Battery Pack**
- **Portable DVD, DSC, PDA, etc.**

Product Name List

Model	Overcharge detection voltage [VOCU] (V)	Overcharge release voltage [VOCR] (V)	Over-discharge detection voltage [VODL] (V)	Over-discharge release voltage [VODR] (V)	Over-current detection voltage [VOI1] (mV)	0 V Battery Charging Function
FS3332A	4.250±0.025	4.050±0.050	2.40±0.080	3.00±0.100	150±20	Yes
FS3332B	4.350±0.025	4.150±0.050	2.30±0.080	3.00±0.100	300±20	Yes
FS3332L	4.300±0.025	4.050±0.050	2.00±0.080	3.00±0.100	200±20	Yes

Overcharge and over-discharge and over-current detection voltages can be changed at the customer's request.

Pin Configuration



Pin No.	Symbol	Description
1	SENS	Detection pin for voltage between SENS and VC (Detection for overcharge and over-discharge)
2	DO	FET gate connection pin for discharge control
3	CO	FET gate connection pin for charge control
4	VM	Input pin for current sense (Over-current detection pin)
5	VSS	Negative power input pin
6	ICT	Capacitor connection pin for detection delay
7	VC	Connection for negative voltage of battery 1 and positive voltage of battery 2
8	VDD	Positive power input pin

Functional Block Diagram

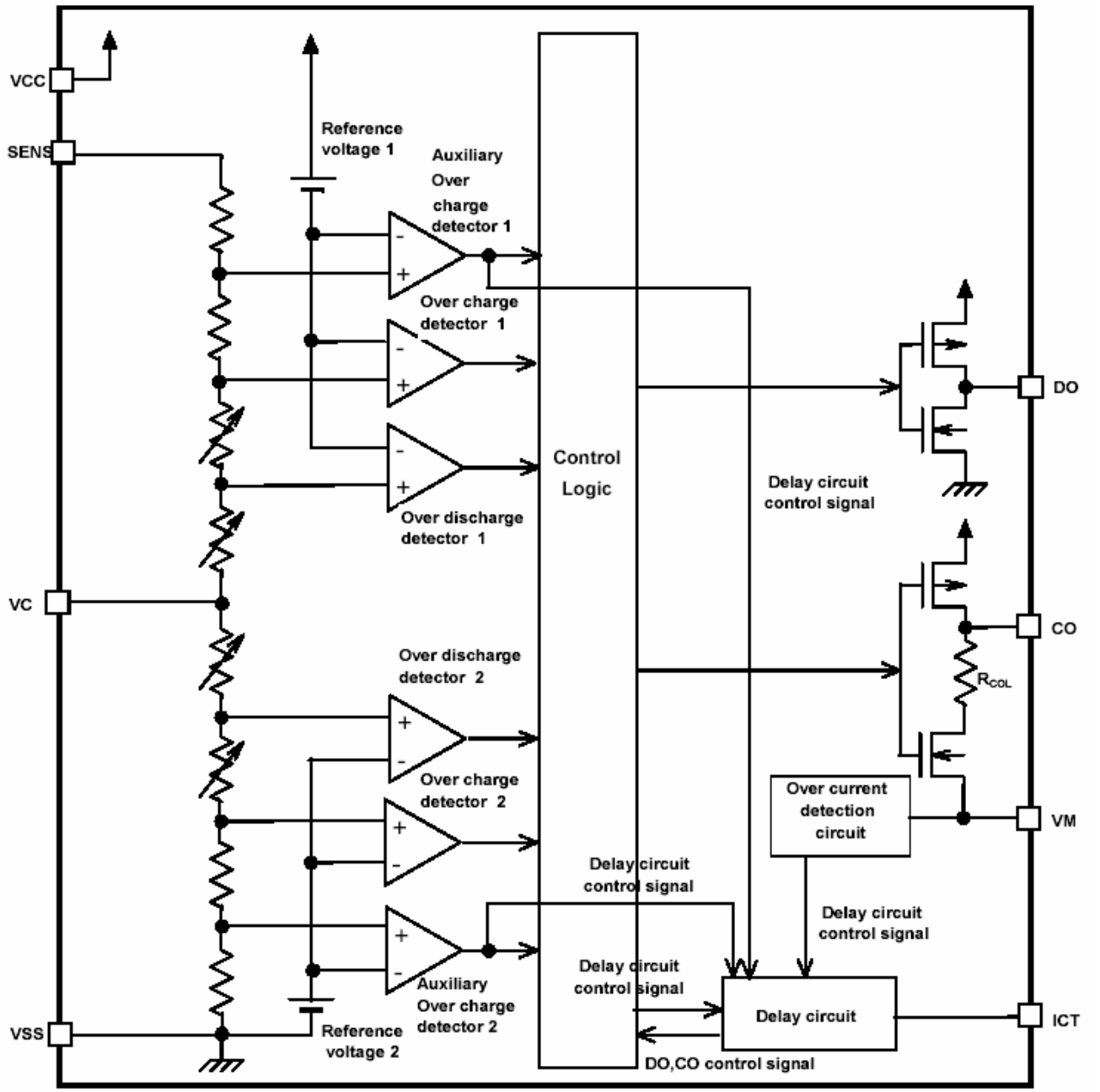
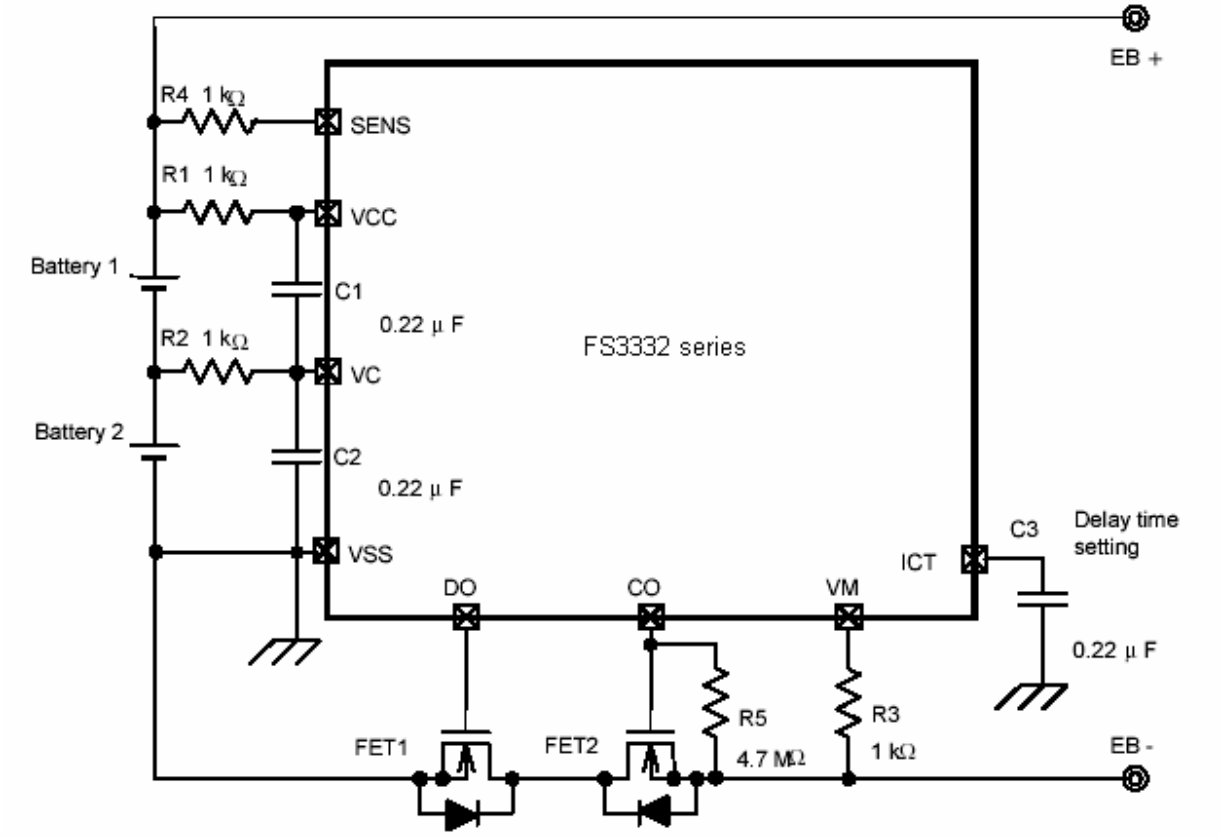


Figure 1

Typical Application Circuit



Absolute Maximum Ratings

(VSS=0V, Ta=25°C unless otherwise specified)

Item	Symbol	Rating	Unit
Input voltage between VDD and VSS *	V_{DD}	V_{SS}-0.3 to V_{SS} +18	V
SENS input pin voltage	V_{SENS}	V_{SS} -0.3 to V_{DD} +0.3	V
ICT input pin voltage	V_{ICT}	V_{SS} -0.3 to V_{DD} +0.3	V
CO output pin voltage	V_{CO}	V_{VM} -0.3 to V_{DD} +0.3	V
DO output pin voltage	V_{DO}	V_{SS} -0.3 to V_{DD} +0.3	V
VM input pin voltage	V_{VM}	V_{DD} -18 to V_{DD} +0.3	V
VC input pin voltage	V_{VC}	V_{SS} -0.3 to V_{DD} +0.3	V
Operating Temperature Range	T_{OP}	-40 to +85	°C
Storage Temperature Range	T_{ST}	-40 to +125	°C

Note: FS3342 contains a circuit that will protect it from static discharge; but please take special care that no excessive static electricity or voltage which exceeds the limit of the protection circuit will be applied to it.

* Pulse (μsec) noise exceeding the above input voltage (V_{SS} +12V) may cause damage to the IC.

Electrical Characteristics

(VSS=0V, Ta=25°C unless otherwise specified)

PARAMETER	CONDITIONS	SYMBOL	Min	Typ	Max	UNIT
CURRENT CONSUMPTION						
Supply Current	VDD=7V(2*3.5V)	IDD		7.5	12.7	μA
Power-Down Current	VDD=4.0V(2*2V)	IPD			0.1	μA
OPERATING VOLTAGE						
Operating input voltage	VDD-VSS	VDS1	2.0		16	V
DETECTION VOLTAGE						
Overcharge detection voltage		VOCU	VOCU -0.025	VOCU	VOCU +0.025	V
Auxiliary overcharge detection Voltage 1,2		$VCU_{AUX1,2}$	VOCU* 1.21	VOCU* 1.25	VOCU* 1.29	
Overcharge release voltage		VOCR	VOCR -0.050	VOCR	VOCR +0.050	V
Over-discharge detection voltage		VODL	VODL -0.080	VODL	VODL +0.080	V
Over-discharge release voltage		VODR	VODR -0.100	VODR	VODR +0.100	V
Over current detection voltage 1		VOI1	VOI1 -0.020	VOI1	VOI1 +0.020	V
Over current detection voltage 2		VOI2	-1.57	-1.20	-0.83	V
DELAY TIME(C3=0.22μF)						
Overcharge detection delay time		TOC	0.73	1.00	1.35	s
Over-discharge detection delay time		TOD	68	100	138	ms
Over current detection delay time		TOI1	6.7	10	13.9	ms
OTHER						
CO pin output “H” voltage		Voh1	V_{DD}-0.15	V_{DD}-0.019	V_{DD}	V
DO pin output “H” voltage		Voh2	V_{DD}-0.05	V_{DD}-0.003	V_{DD}	V
DO pin output “L” voltage		Vol2	V_{SS}	V_{SS}+0.003	V_{SS}+0.05	V
Resistance between VSS and CO		R_{COL}	0.29	0.6	1.44	MΩ
Resistance between VDD and VM		R_{VMD}	105	240	575	kΩ
Resistance between VSS and CO		R_{VSM}	511	597	977	kΩ
0 V battery charge starting voltage		V_{0CHA}	0.38	0.75	1.12	V

Description of Operation

1. Normal Condition

This IC monitors the voltage of the battery connected between the VDD and VSS pins and the voltage difference between the VM and VSS pins to control charging and discharging. When the voltages of two batteries are in the range from over-discharge detection voltage ($V_{DL1,2}$) to overcharge detection voltage ($V_{CU1,2}$), and the VM pin voltage is in the range from the charger detection voltage (V_{CHA}) to over-current detection voltage 1 (V_{IOV1}), the IC turns both the charging and discharging control FETs on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely. The VM and VSS pins are shorted by the R_{VSM} resistor in this condition.

Caution: When the battery is connected for the first time, discharging may not be enabled. In this case, short the VM and VSS pins or connect the charger to restore the normal status.

2. Overcharge Condition

When one of the battery voltages becomes higher than overcharge detection voltage ($V_{CU1,2}$) during charging in the normal status and detection continues for the overcharge detection delay time ($t_{CU1,2}$) or longer, the charging control FET turns off to stop charging. When one of the battery voltages becomes higher than auxiliary overcharge detection voltage ($V_{CUAUX1,2}$), the charging control FET turns off to stop charging, too. Both conditions are called the overcharge status. The VM and VSS pins are shorted by the R_{VSM} resistor in this condition.

The overcharge status is released in the following two cases (a and b).

a) The battery voltage which exceeded overcharge detection voltage ($V_{CU1,2}$) falls below the overcharge release voltage ($V_{CR1,2}$), the charging control FET turns on and returns to the normal status.

b) The battery voltage which exceeded overcharge detection voltage ($V_{CU1,2}$) is equal to or higher than the overcharge release voltage ($V_{CR1,2}$), the charger is removed, a load is connected and discharging starts, the charging control FET turns on and returns to the normal status. Just after the load is connected and discharging starts, the discharging current flows through the parasitic diode in the charging control FET. At this moment the VM pin potential becomes V_f, the voltage for the parasitic diode, higher than the V_{SS} level. When the battery voltage goes under overcharge detection voltage ($V_{CU1,2}$) and provided that the VM pin voltage is higher than over-current detection voltage 1, the IC releases the overcharge status and returns to the normal status.

3. Over-discharge Condition

When one of the battery voltages falls below over-discharge detection voltage ($V_{DL1,2}$) during discharging in the normal status and detection continues for the over-discharge detection delay time ($t_{DL1,2}$) or longer, the discharging control FET turns off to stop discharging. This condition is called the over-discharge status. When the discharging control FET is turned off, the VM pin voltage is pulled up by the resistor between the VM and VDD pins in the IC (R_{VMD}). When the voltage difference between the VM and VDD pins then is over-current detection voltage 2 or lower, the current consumption is reduced to the power-down current consumption (I_{PDN}). This condition is called the power-down status. The power-down status is released when a charger is connected and the voltage difference between the VM and VDD pins is over-current detection voltage 2 or higher. Moreover, when all the battery voltages become over-discharge detection voltage ($V_{DL1,2}$) or higher, the discharging FET turns on and returns to the normal status.

4. Over Current Condition

When a battery in the normal status is in the status where the voltage of the VM pin is equal to or higher than the over-current detection voltage because the discharge current is higher than the specified value and the status lasts for the over-current detection delay time, the discharge control FET is turned off and discharging is stopped. This status is called the over-current status. In the over-current status, the VM and VSS pins are shorted by the resistor between VM and VSS (R_{VSM}) in the IC. The charging FET is also turned off. The voltage of the VM pin is at the V_{DD} potential as long as the load is connected. When the load is disconnected, the VM pin returns to the V_{SS} potential. This IC detects the status when the impedance between the EB+ pin and EB- pin (see typical application circuit) increases and is equal to the impedance that enables automatic restoration and the voltage at the VM pin returns to over-current detection voltage 1 (V_{IOV1}) or lower and the over-current status is restored to the normal status.

Caution: The impedance that enables automatic restoration varies depending on the battery voltage and the set value of over-current detection voltage 1.

5. Delay Circuits

The overcharge detection delay time ($t_{CU1,2}$), the over-discharge detection delay time ($t_{DL1,2}$), and the over-current detection delay time 1 (t_{OI1}) are set via an external capacitor (C3). One capacitor determines each delay time, and the delay times are correlated by following ratio:

Overcharge delay time : Over-discharge delay time : Over-current delay time = 100 : 10 : 1

The delay times are calculated as follows:

Overcharge detection delay time t_{CU} [s] = delay factor 1 x C3 [µF]

Delay factor 1 = (2.500 min, 4.545 typ, 9.364 max)

Over-discharge detection delay time t_{DL} [s] = delay factor 2 x C3 [µF]

Delay factor 2 = (0.3045 min, 0.4545 typ, 0.6409 max)

Over-current detection delay time 1 t_{IOV1} [s] = delay factor 3 x C3 [µF]

Delay factor 3 = (0.02864 min, 0.04545 typ, 0.06682 max)

Note : The over-current detection delay time 2 is fixed by internal circuit.

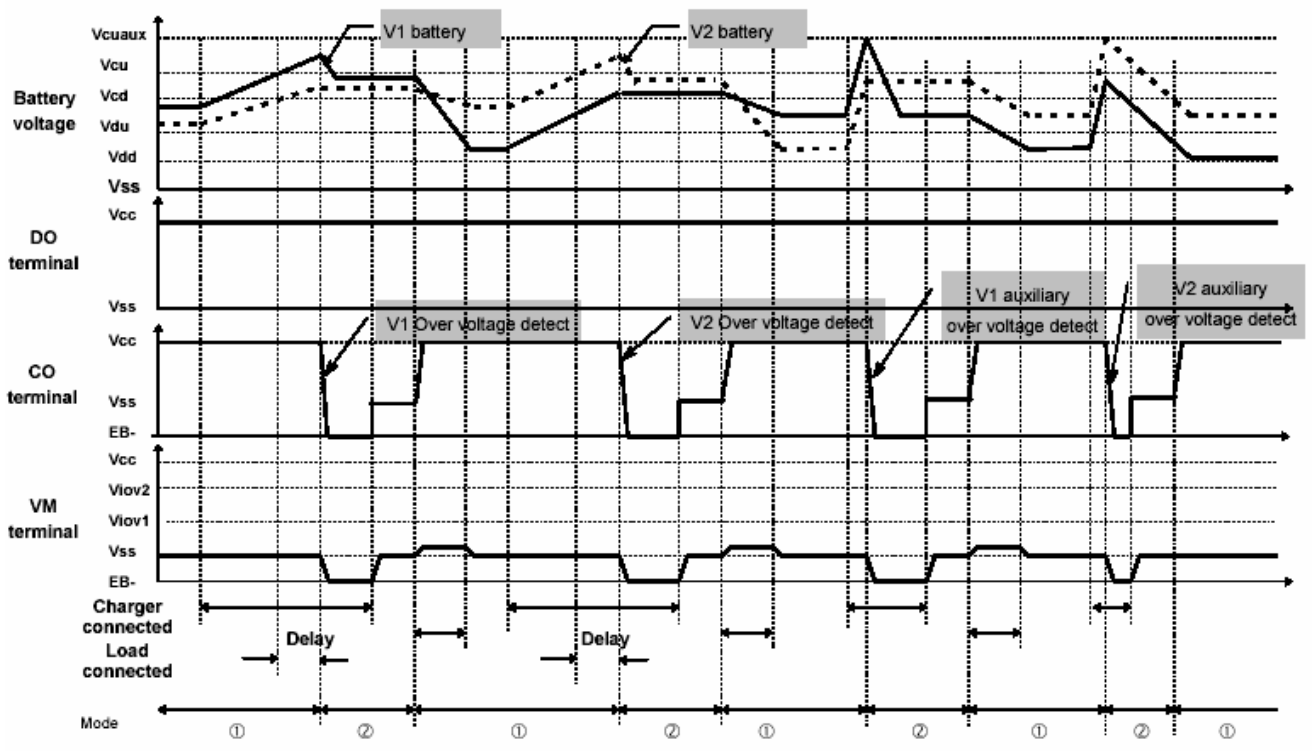
6. 0 V Battery Charging Function

This function is used to recharge both of two serially-connected batteries after they self-discharge to 0 V. When the 0 V charging start voltage (V_{0CHA}) or higher is applied to between VM and VDD by connecting the charger, the charging FET gate is fixed to VDD potential.

When the voltage between the gate sources of the charging FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging FET turns on to start charging. At this time, the discharging FET turns off and the charging current flows through the internal parasitic diode in the discharging FET. If all the battery voltages become equal to or higher than the over-discharge release voltage ($V_{DL1,2}$), the normal condition returns.

Timing Diagram

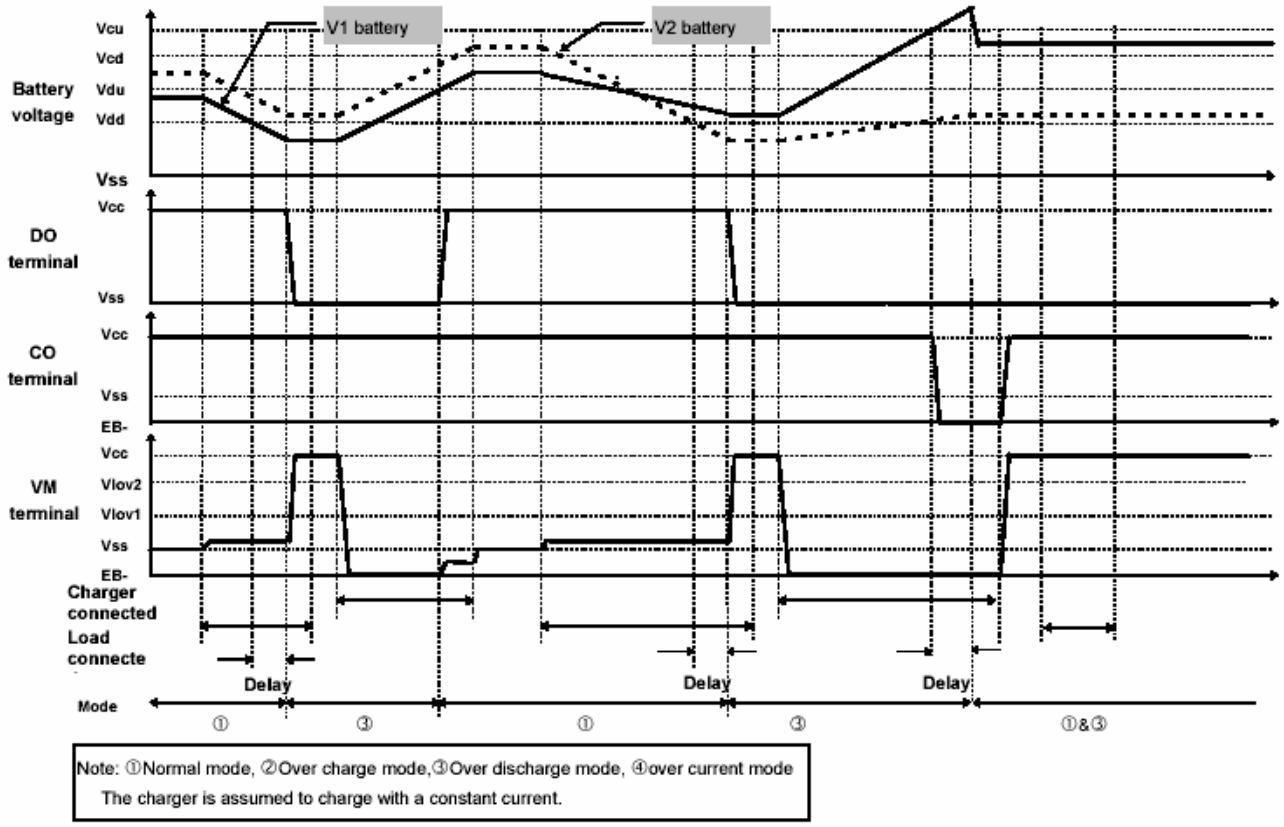
1. Overcharge detectiontion



Note: ①Normal mode, ②Over charge mode,③Over discharge mode, ④over current mode
The charger is assumed to charge with a constant current.

Figure 3

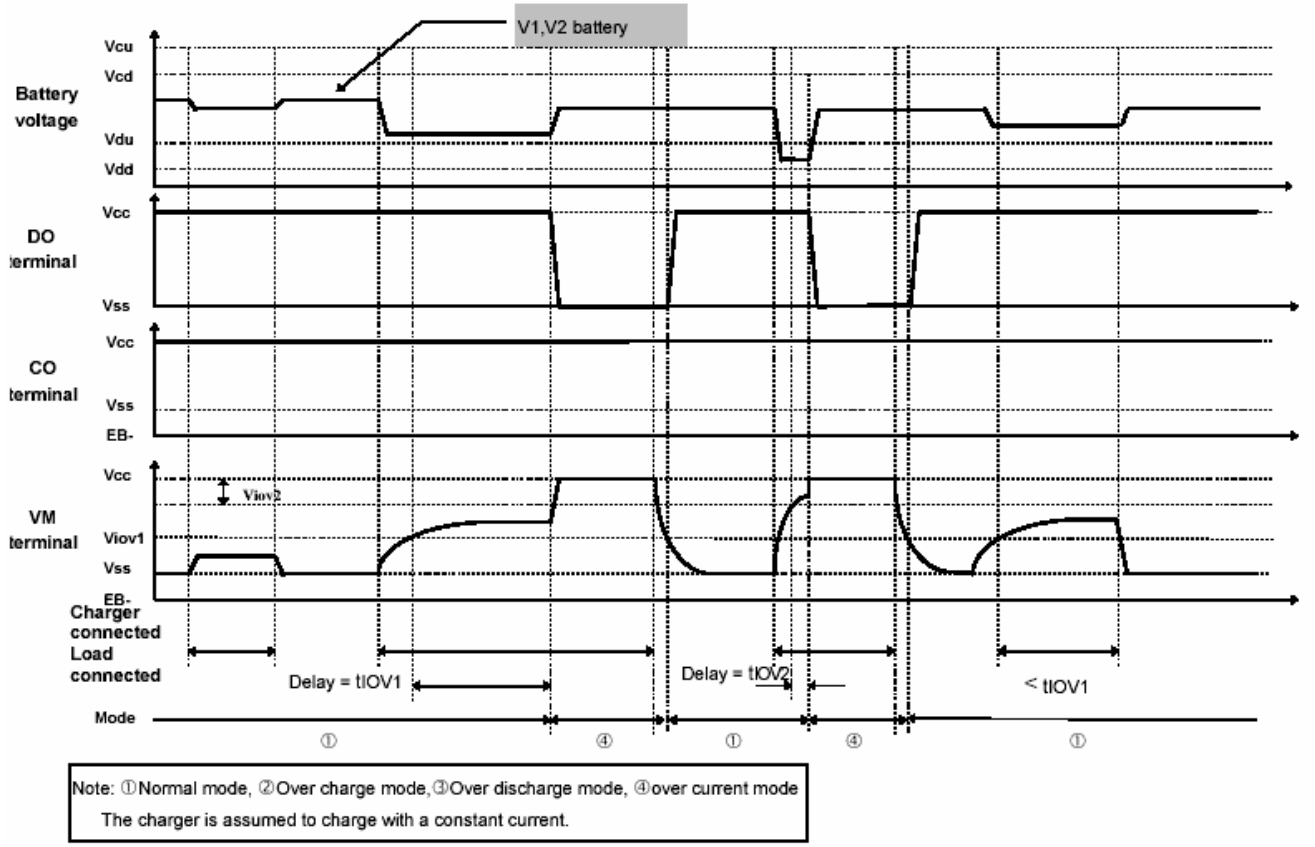
2. Over-discharge detection



Note: ①Normal mode, ②Over charge mode,③Over discharge mode, ④over current mode
The charger is assumed to charge with a constant current.

Figure 4

3. Over-current detection



Note: ①Normal mode, ②Over charge mode,③Over discharge mode, ④over current mode
The charger is assumed to charge with a constant current.

Figure 5

Typical Characteristics

(To be measured.)

Package Outline

8-pin TSSOP