Controlling the Parasitic Parameters to Improve EMI Filter Performance

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***Abstract* — This paper firstly reviewed the parasitic parameters in EMI filters and then introduced many methods to reduce and control these parasitic parameters. Three important methods of controlling parasitic couplings are analyzed in detail. Experiments show the filter performance is significantly improved using these three methods. A novel method is then proposed to reduce the parasitic parameters of capacitors. The experiment shows the proposed method can effectively reduce the ESL and ESR of capacitors and thus improve the EMI filter performance significantly.**

***Index Terms*— EMI filter, parasitic coupling, inductive coupling, capacitive coupling, transfer gain, ESL and ESR cancellation.**

I. INTRODUCTION

In an EMI filter, two groups of parasitic parameters determine the filter performance. The first group is the parasitic parameters of components, such as the ESL, ESR of capacitors. The effects of this group are well known. The second group is the mutual parasitic parameters caused by the couplings between components. The effects of parasitic couplings on the EMI filter performance are described in the work [1]. The work [1] identified several important couplings affecting EMI filter performance. This paper firstly discusses the methods to control these parasitic couplings and then discusses a method to cancel ESL and ESR of capacitors. The objective of this paper is to explore the methods of controlling parasitic parameters and thus to improve the EMI filter performance.

Six different coupling effects are firstly reviewed in this paper: the inductive couplings between the inductor and capacitors, a filter inductor and trace loops, two capacitor parasitic inductances, a filter inductor and ground plane, and two trace loops. The last one is the capacitive coupling between in and out traces. The effects of most of these couplings on EMI filter performance are discussed in detail in work [1]. For a typical Π filter, the schematic, prototype and the parasitic couplings for the differential mode (DM) filter are shown in Fig.1.

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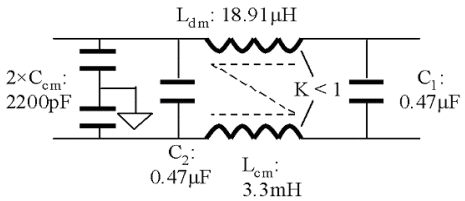

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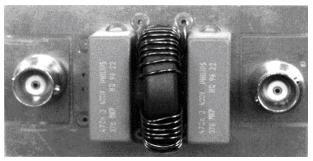

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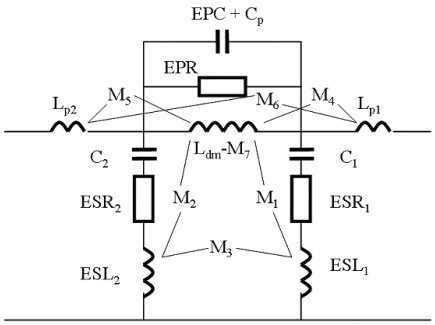


(c)

L_{p1}, L_{p2}: trace-loop inductance
ESL, ESR, C: capacitor model parameters
L_{dm}, EPC, EPR: DM inductor model parameters
M_1, M_2: mutual inductance between L_{dm} and capacitor branches
M_3: mutual inductance between two capacitor branches
M_4, M_5: mutual inductance between L_{dm} and trace loops
M_6: mutual inductance between in and out trace loops
M_7: equivalent mutual inductance between ground plane and L_{dm}
C_p: mutual capacitance between in and out traces.

Fig.1. EMI filter and the parasitic couplings of its DM part.
(a) Circuit of the filter.
(b) Prototype of the filter .
(c) DM filter model.

In Fig.1, because the DM inductor is the leakage of CM inductor, the DM inductor can easily couple with other components. M1 and M2 are the mutual inductive couplings

between DM inductor and the capacitors. M4 and M5 are the mutual inductive couplings between the DM inductor and in, out trace loops. The inductive coupling M3 between two capacitors plays very important role in filter performance because of the larger current difference between these two capacitors [1]. It becomes more significant especially under following conditions: (1) the inductive couplings between the inductor and the capacitor, between the inductor and the trace loops are well controlled; thus their effects are neglectable. (2) when two capacitors are close to each other. The ground plane on the printed circuit board (PCB) generates the eddy current, which reduces the DM inductance and is characterized as M7. The capacitive coupling between the in and out traces is characterized by Cp, which is equivalent to enlarge the paralleled capacitance with the DM inductor. This capacitive coupling includes the direct capacitive coupling between in and out traces and the capacitive couplings through the ground plane. Another inductive coupling M6 is between the in and out trace loops. All of these couplings affect the performance of EMI filters, which makes the performance of the filter components deviate from what a designer expected.

This paper discusses the methods to control the parasitic couplings in the EMI filter. For those unknown to engineers, experimental results are given. By applying these methods, the EMI filter performance is greatly improved especially in the high frequency range.

II. CONTROL THE COUPLINGS IN THE EMI FILTERS

From the analysis in the previous section, M1, M2 and M3 directly affect the performance of capacitors. M4 and M5 affect the capacitors through branch current. Therefore, capacitors are the critical components to improve the EMI filter performance. Preventing capacitors from being affected by the couplings is a sensible method. The ground plane is another important factor influencing the performance of EMI filters because it facilitates the capacitive couplings and reduces the inductance of inductor. Therefore, a suitable ground plane layout is necessary to reduce its effects.

In order to reduce M1 and M2, measures include:

1) Using the proposed winding arrangement as described in work [1], which is shown in Fig.2.

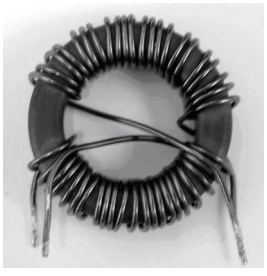


Fig.2. Two windings are rotated by 90° to reduce the inductive couplings caused by the inductor.

In Fig.2, because two windings are symmetrical to the capacitor, the mutual inductance between the inductor and the capacitors is greatly reduced. This approach was proposed in work [1] and will be quantified in this paper.

2) Keeping the capacitors and the inductor far away enough to reduce the inductive coupling between them. The disadvantage of this method is that it results in a larger filter size.

3) Shielding two capacitors to reduce the couplings with capacitors. Two shields should be kept far away enough to reduce the possible capacitive couplings between them. The shield and the inductor should also be kept far away enough also to reduce its effects on the inductance of the inductor.

In order to reduce M3, measures include:

1) Keeping two capacitors far away enough to reduce the inductive coupling between them. The disadvantage is a larger filter size.

2) Two capacitors can be shielded.

3) The pin of the capacitor should be kept as short as possible to reduce loops generating inductive couplings.

For M4, M5 and M6, two measures can be used to reduce them:

1) The proposed winding arrangement can be used for the inductor to reduce the inductive coupling with trace loops.

2) The areas of in and out trace loops should be kept small to reduce the M4, M5 and M6.

M_7 and C_p result from the ground plane and the effects of the ground plane should be reduced. Some steps can be taken to reduce these effects:

1) Do not use ground plane under the inductor to reduce M_7.

2) Keeping the enough clear distance between ground plane and traces, in and out traces to reduce the direct capacitive couplings and those through the ground plane.

For a two-stage filter, the inductive coupling between two inductors determines the low frequency performance of the EMI filters, because this mutual inductance, which is equivalent to be series with the middle capacitor, is much larger than the ESL of the capacitor [1]. The methods include:

1) Two inductors can be placed in perpendicular fashion to reduce the inductive coupling between them.

2) Purposely selecting the appropriate winding directions to get either positive or negative mutual inductance.

Many measures are recommended above. Some of them are well known, while some are seldom recognized. For example, using the proposed winding arrangement, shielding two capacitors and special ground layout are seldom used in the EMI filter design.

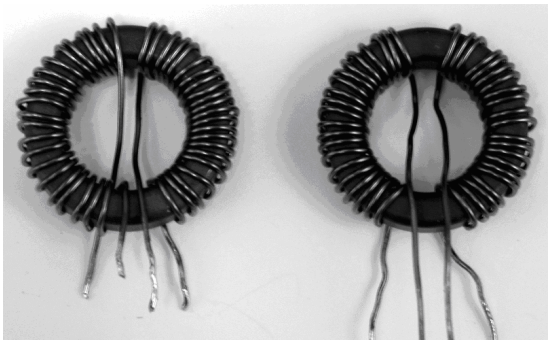
Another method to control the parasitic parameters is changing PCB layout, which will be discussed in this paper.

III. EXPERIMENTAL RESULTS

Many methods used to control the parasitic couplings in an EMI filter are recommended in the previous section. The experiments are mainly carried out to investigate three methods: using the proposed winding arrangement, shielding two capacitors and changing PCB layout.

A. Proposed winding arrangement

The proposed winding structure is shown in Fig.2 of previous section. Two windings are symmetrical to the trace loops and the capacitors so it can reduce the mutual inductances M1, M2 and M4, M5. On the other hand, two conventional winding structures are shown in Fig.3. Their winding directions are different. The windings are located on the two sides of the core, which is unsymmetrical to the trace loops and capacitors; so the mutual inductances are much larger than those of proposed winding arrangement.



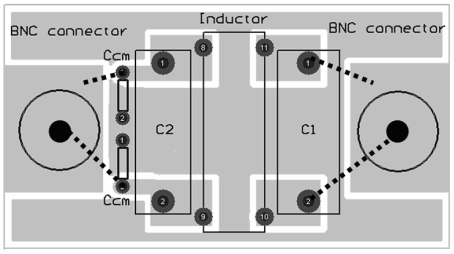
Winding direction1 Winding direction2

Fig.3. Two conventional winding arrangements (Two windings are on the two sides of the core).

Three inductors with same inductances are then mounted to the PCB of an EMI filter to compare the performance.

The PCB layout of the investigated EMI filter is shown in Fig.4; and the measured transfer gains are shown in Fig.5.

The mutual inductances between the inductor and the capacitors, between the inductor and the trace loops are extracted and they are shown in Table I.



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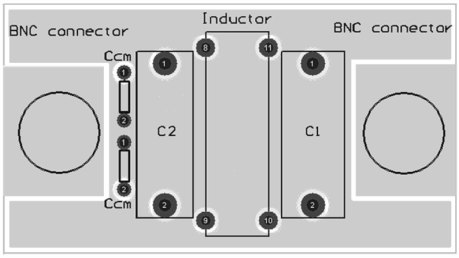


(b)

Fig.4. PCB layout of the investigated filter. (a) Top side. (b) Bottom side.

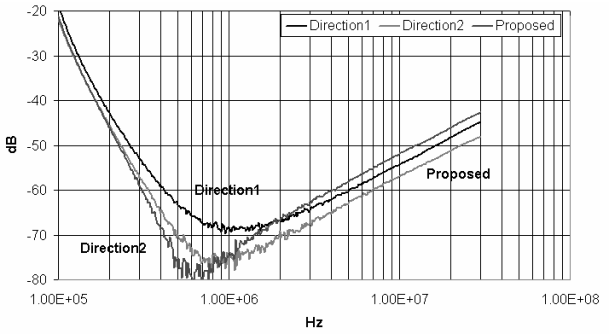


Fig.5. Comparison of measured transfer gains

Table I. Extracted mutual inductances

	Between the inductor and in/out trace loops	Between the inductor and capacitor branches
Winding direction1 (negative coupling)	18.7 nH	89.3 nH
Winding direction2 (positive coupling)	10.3 nH	83.3 nH
Proposed arrangement	1.8 nH	7.5 nH

In Table I, the mutual inductances are greatly reduced by employing the proposed winding structure. Because the ESL of capacitor is 14nH, the conventional winding arrangements have much larger mutual inductances than ESL. They affect the capacitor performance significantly. After using the proposed winding structure, the mutual inductance is smaller than ESL. In Fig.5, the proposed winding arrangement gives better performance in the whole frequency range.

B. Changing PCB Layout to Improve EMI Filter Performance

For the PCB layout in Fig.4, M1 and M2 always have same polarity. So do M4 and M5. Therefore two capacitor branches have similar performance. In Fig.6, the traces at one side of the filter are changed. Two points labeled A and two points labeled B are connected together respectively. Because the current goes through the different way from the original layout, the EM field distribution is also changed. As a result, not only the polarities but also the values of M2, M3, M5 and M6 are different from those of the original layout. The filter performance is therefore different from the original one.

Fig.7 shows the measured transfer gains, which are compared with the original ones.

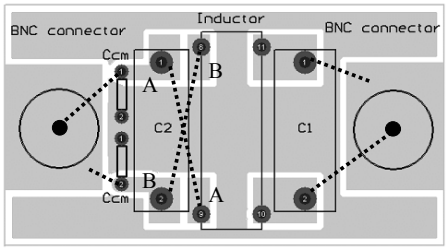
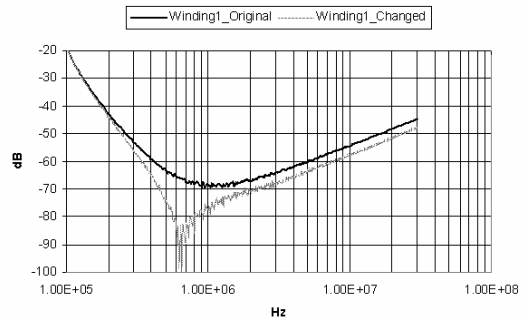


Fig.6. Changing the couplings through the PCB layout.



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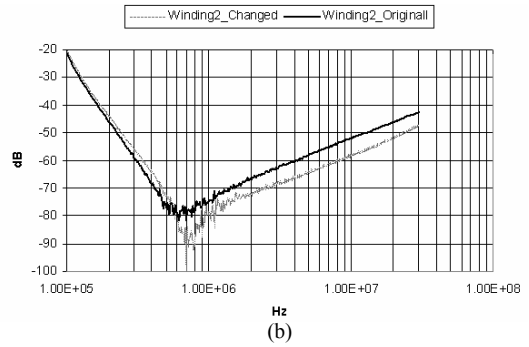

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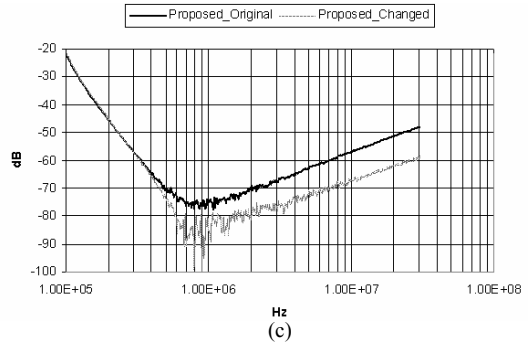

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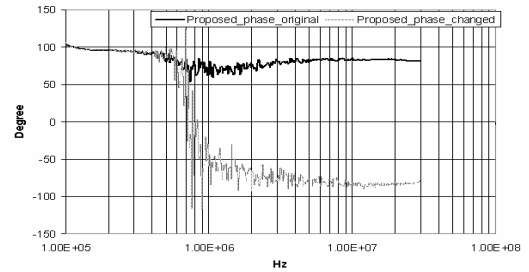


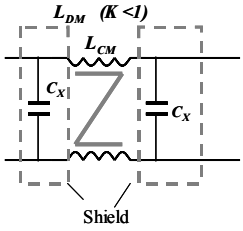
(d)

Fig.7. Comparison of the transfer gains.
(a) The case of winding direction1. (b) The case of winding direction2.
(c) The case of proposed winding arrangement and (d) the phases.

In Fig.7, after the PCB layout was changed, all three cases are improved. The case of winding direction 1 is almost same as the case of winding direction 2 because after the PCB layout changed they are almost same: one capacitor branch is positive coupling [1] and another side is negative coupling [1]. For the proposed winding arrangement, the performance is improved as much as 11dB. It is obvious that using both proposed winding structure and proposed trace layout is the best choice. The EMI filter has a 15 dB improvement compared with the original case of winding direction 1 (the typical industrial application). There is a 180° phase difference between the original and the changed PCB for each case above 1MHz (Only the proposed arrangement is shown in (d)), which is attributed to the opposite coupling polarities between two capacitors. The method is very attractive, because no new components are added and much better performance is achieved. Fig.7 also shows that the performance of the changed case below 1MHz is similar to the original positive coupling [1] case, which benefits the performance in low frequency range.

C. Shielding the capacitors and with careful ground plane layout

The mutual inductances between two capacitors affect the capacitors too much because the large current difference of two capacitor branches [1]. The ground plane should be carefully designed to reduce the effect on inductor and the capacitive coupling between in and out traces. For this case, the investigated EMI filters are shown in Fig.8.



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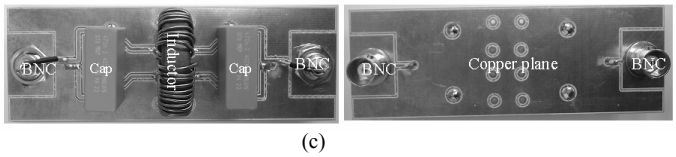

(c)

Fig.8. Comparison of two EMI filters.
(a) The schematic of the EMI filter.
(b) The filter with shielded capacitors and careful ground plane layout.
(c) The conventional design.

In Fig.8, two EMI filters are compared. For the filter shown in (b), capacitors are shielded so the couplings between the inductor and capacitors and between two capacitors are greatly reduced. No copper plane is placed under the inductor so copper plane has no effects on the inductance of the inductor. The copper plane is separated into two parts without connection so the capacitive coupling through the ground plane is reduced. The in and out loop areas are small so the couplings with these two loops are reduced. The shields are inserted and soldered on the copper plane through the slots on the PCB. Two BNC connectors are attached on the two sides for the measurement. For the inductor, the loop areas beside the inductor are kept small to prevent the coupling between these two loops. By employing these measures, not only the inductive couplings in the filter but also the capacitive couplings through the ground plane are reduced. In Fig.8, the filter shown in (c) is a practical case with a conventional ground plane and PCB layout. The measured transfer-gain curves are compared in Fig.9.

In Fig.9, the enhanced EMI filter of (b) greatly improves the performance from 400kHz to 22MHz. From 1MHz to 15MHz, the transfer gain is very good even below the background noise of the network analyzer.

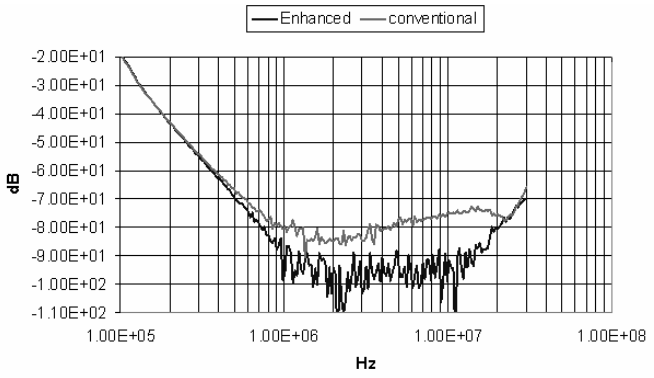

Fig.9. Comparison of the EMI filter performance.

Above 22MHz, the enhanced EMI filter is almost same as the original one because of the capacitive coupling between two shields.

IV. Reduce the Paraisitc Parameters of Capacitors

When the mutual couplings are well controlled, the self-parasitic parameters would play an important role on EMI filter performance. In fact, the self-parasitic parameters of the components can also be well controlled and reduced. The following example is to reduce the ESL and ESR of the capacitors and thus to improve the capacitor and filter performance significantly.

The basic idea is using a network to cancel ESL and ESR, which is shown in Fig.10.

In Fig.10, for a two-port network connected as the left diagram, the network can be equivalent to the right one. If Z3 branches are capacitors and Z1 is equal to ESL or ESL + ESR, then the network can be equivalent to new networks shown in Fig.11.

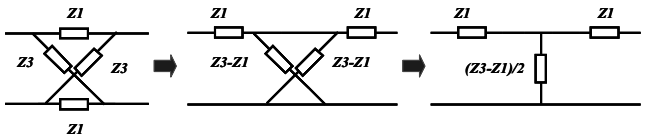

Fig. 10. Network theory used to reduce ESL and ESR.

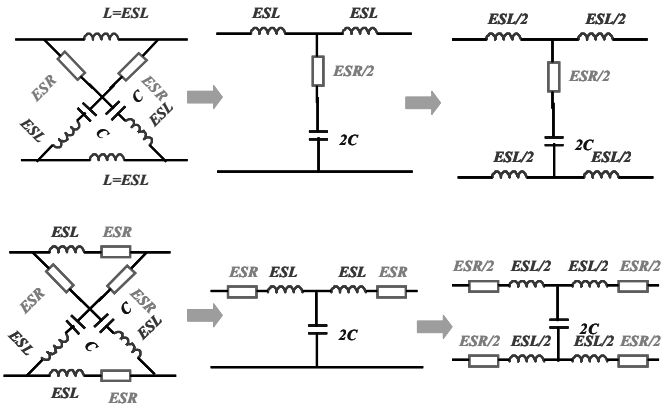

Fig. 11. Idea of ESL and ESR cancellation.

In Fig.11, the inductance ESL and ESR are pushed to the two sides of the network, which benefits the performance of capacitor because ESL, ESR and the capacitor form a T type filter. This approach reduces not only the parasitic parameters of capacitors, but also constructs a T type filter.

This idea is implemented to a prototype shown in Figs.12, 13.

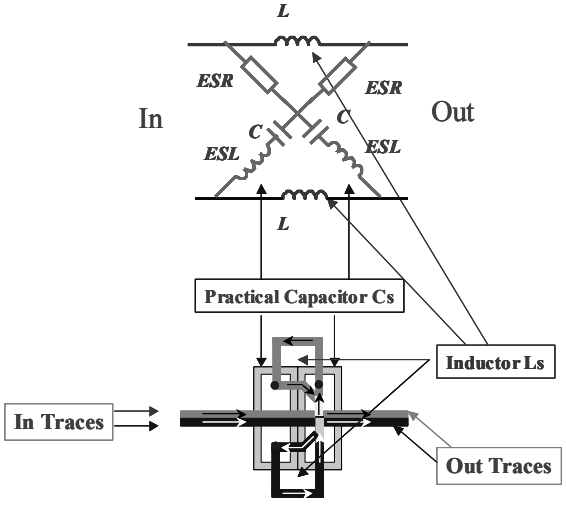

Fig. 12. PCB layout used to implement the idea.

In Fig.12, the cancellation windings are constructed by the PCB traces. By regulating the areas of the PCB traces, the desired inductance can be achieved. Here, ESL includes all the parasitic inductances on the capacitor branch. Two PCBs are built in Fig.13 for comparison. The left PCB is two paralleled capacitors. The right one is the PCB with proposed idea. The capacitor is polystyrene capacitor (0.47μF).

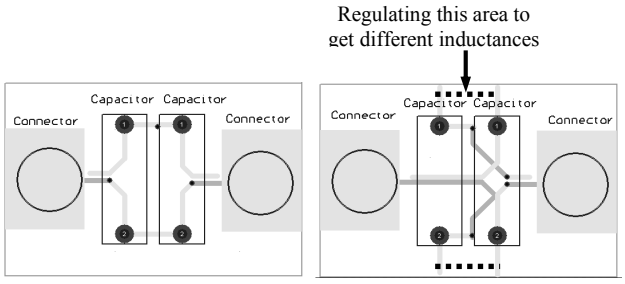

Fig. 13. PCB layouts used for comparison.
(a) Two paralleled capacitors.
(b) Two capacitors with parasitic parameters reduction.

The experimental results are shown in Fig.14. A group transfer gains are measured with different cancellation winding inductances. In Fig.14, the top one is the transfer gain of two paralleled capacitors. The self-resonant frequency of the capacitor is around 2MHz. Other curves are the transfer gains of proposed structure. As the inductance of the cancellation windings increases from L1 to L2, the resonant frequency increases. The valley values of the transfer-gain decrease due to the AC resistance of cancellation windings. Part of ESR and ESL are in fact cancelled due to the inductance and AC resistance of the cancellation windings. As the inductance of the cancellation windings increases from L3 to L4, the resonant frequency keeps increasing. But the equivalent minus resistance makes the valley values larger than L1 and L2 cases. The ESL is almost cancelled for the curve L4 because the transfer gain is a straight line before 8MHz.

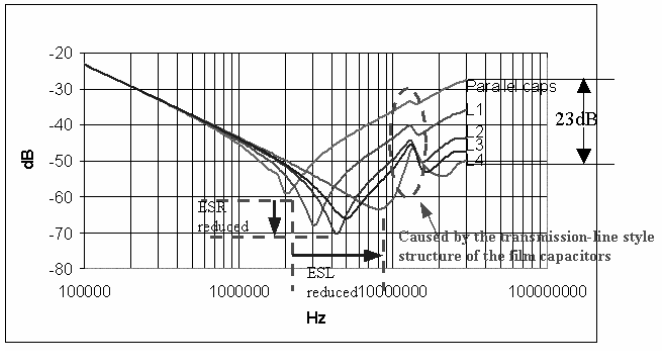

Fig. 14. Comparison of the measured transfer gains of capacitors.

The bump between 10MHz and 20MHz is caused by the transmission-line style structure of the film capacitors [3]. This bump causes the transfer gain goes up. Compared with the two capacitors without parasitic cancellations, at 30MHz, 23dB improvement achieved. Further increasing the cancellation winding inductance or resistance would cause equivalent minus inductance and resistance and would not offer better performance. So L2 is the optimal value. If the resistance of the cancellation winding is kept constant, the ESR and ESL could be well reduced. The proposed idea is applied in a Γ filter in Fig.15 and the measured transfer gains are compared in Fig.16. The filter performance is significantly improved in a very wide high frequency range (2MHz-30MHz).

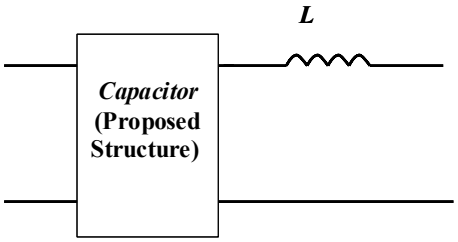

Fig. 15. Schematic of the investigated Γ filter.

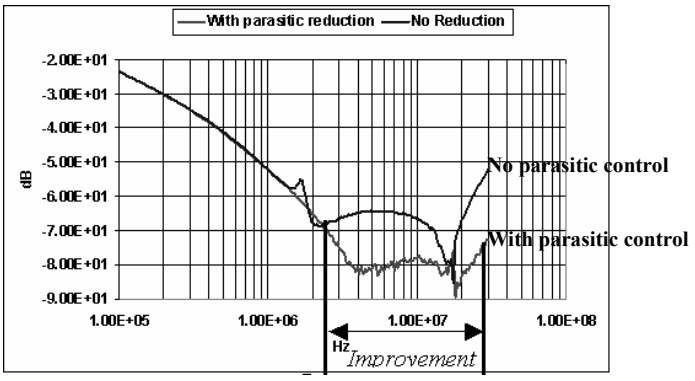

Fig. 16. Comparison of the measured transfer gains of filters.

In Fig.16, for the filter without the parasitic control, the self-resonance shows up around 2MHz and the transfer gain becomes flat after it. The dip near 20MHz is caused by the self-resonance of the inductor. For the filter with the parasitic cancellation, no self-resonance shows up and the transfer gain goes down till reach the noise floor of the network analyzer. The self-resonance of the inductor still shows up near 20MHz. At 30MHz, 20dB improvement is achieved.

In order to effectively improve the EMI filter performance using this idea, the parasitic couplings should be well controlled. The couplings between the capacitors and other components can degrade the capacitor performance.

V. CONCLUSION

In this paper, based on the knowledge of parasitic parameters of EMI filters, many methods are proposed to control the parasitic couplings and self-parasitic parameters. For parasitic couplings, three important methods are verified by experiments. For the self-parasitic parameters, one method is given and verified by the experiment. The experiments show that the proposed methods can effectively control the parasitic parameters in the EMI filter and thus significantly improve the EMI filer performance in high frequency range.

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