SYSTEM GENERAL 崇貿科技

文件名稱	SG6961 Application Note V1.0	制訂部門	系統研發部
文件編號	IAO37.0009	版　本	B0
生效日期	2005/12/05	總頁數	

文件修訂履歷

版本	日期	修訂人	修訂頁次	修訂內容概述
B0 V1.0	2005/12/05	蘇英傑	-	新建立; ECN:IA941202-2

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Design and Apply to Power Factor Correction Circuit Using SG6961 **AN6961**

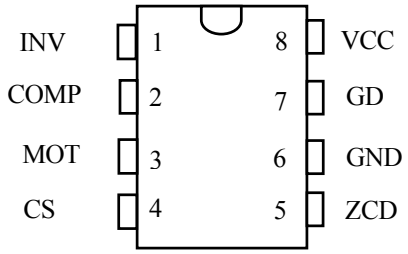
ABSTRACT

This application note describes a power factor correction circuit using the SG6961. Both the features of this controller as well as the operation of the power factor correction circuit are presented in detail. Based on the proposed design guideline, a design example with detailed parameters is given to demonstrate the great performance of the controller.

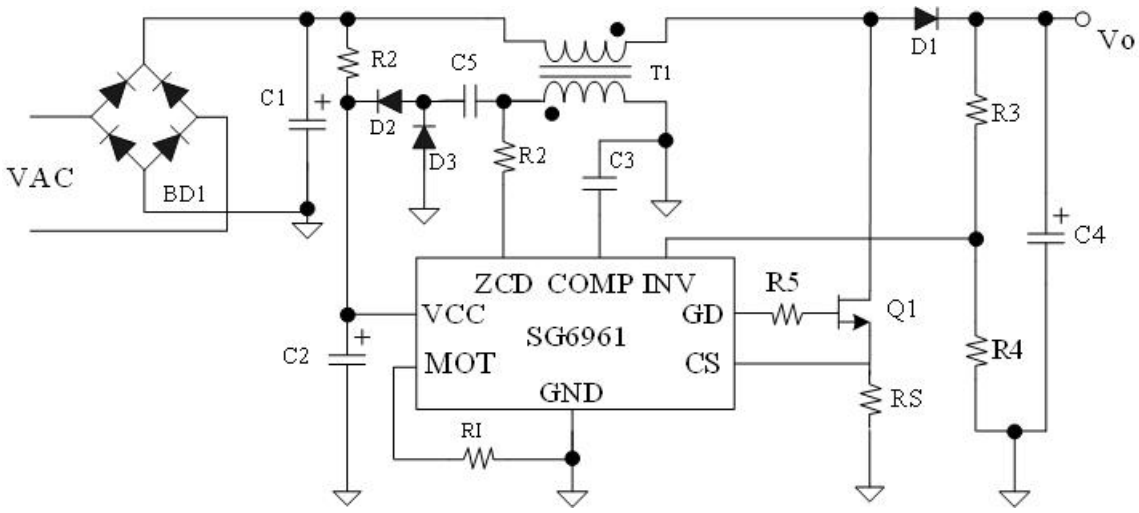
FEATURES

- Boundary Mode PFC Controller
- Low Input Current THD
- Controlled On-Time PWM
- Zero-Current Detection
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking instead of RC Filtering
- Low Start-Up Current (10uA TYP.)
- Low Operating Current (5mA TYP.)
- Feedback Open loop Protection
- Programmable Maximum On-Time (MOT)
- Output Over-Voltage Clamping Protection
- Clamped Gate Output Voltage 16.5V

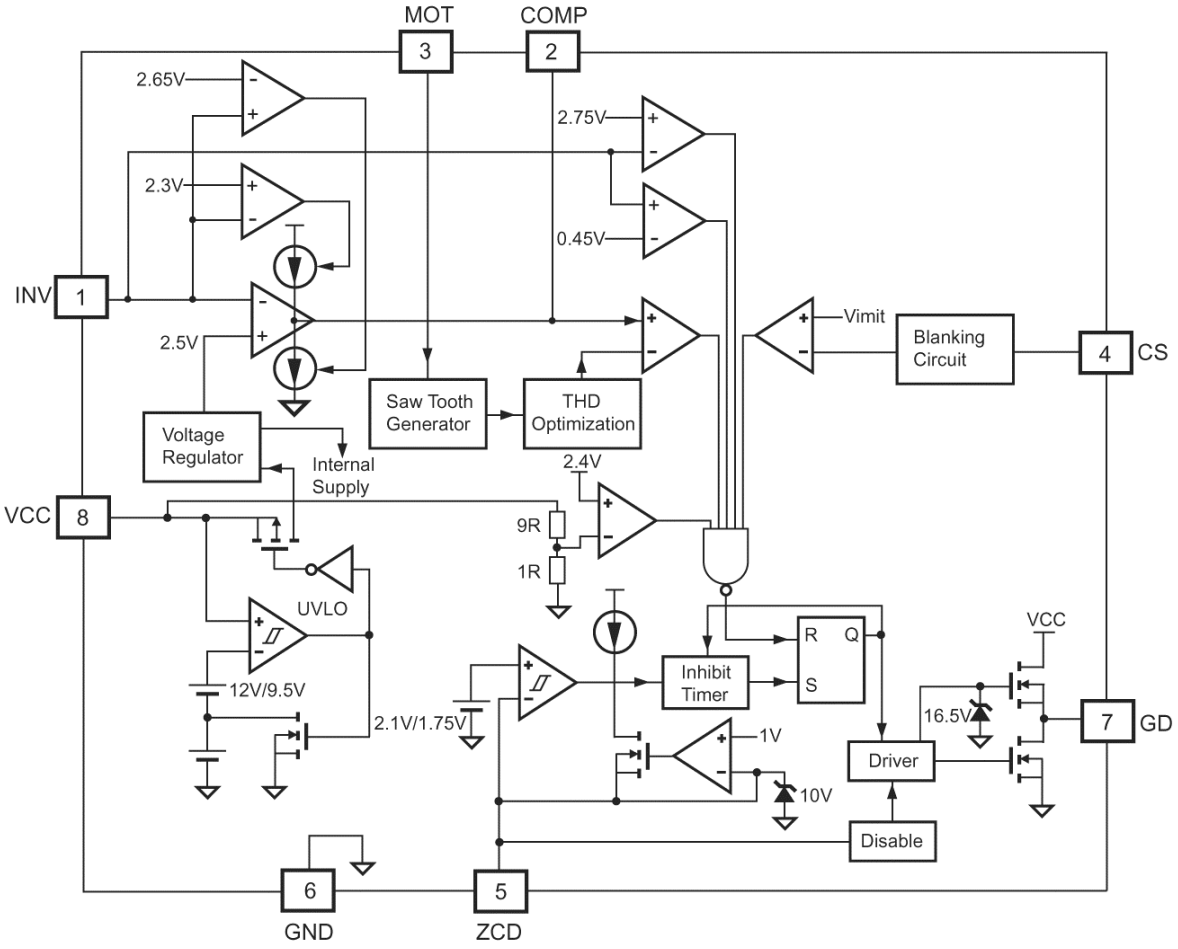
PIN CONFIGURATION



TYPICAL APPLICATION



BLOCK DIAGRAM



INTRODUCTION

The SG6961 PFC controller is an 8-pin boundary current mode(BCM) IC intended for controlling PFC pre-regulators. The SG6961 has many new features. It provides a controlled on-time to regulate the output DC voltage and achieve natural power factor correction. The maximum on-time of the switch is programmable to ensure safe operation during AC brownouts. An innovative multi-vector error amplifier is built in to provide rapid transient response and precise output voltage clamping. Once the output feedback loop is opened, the output driver(GD)will be disabled to provide a great protection of the system. The start up current is lower than 20uA and the operating current has been shrunk to 5mA. The supply voltage can be operated up to 20 volts, maximizing application flexibility. The SG6961 also enables cycle-by-cycle current limiting protection for the external power MOSFET.

1. BASIC OPERATION OF THE BOOST CONVERTER

The typical Boost Converter and its operational waveforms are shown in Figure 1.1, 1.2, and 1.3, respectively.

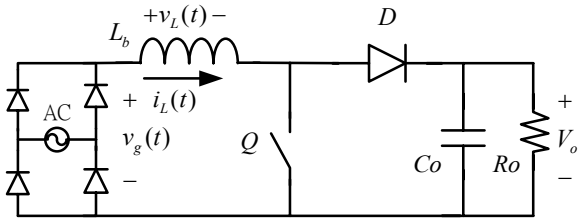
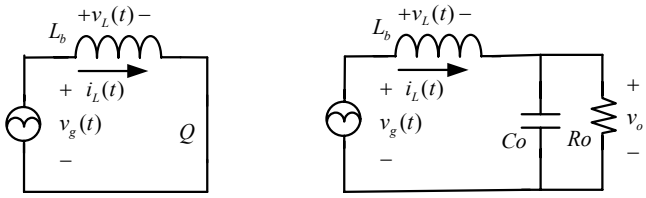


Figure 1.1 Boost Converter



(a) Switch Q is ON (b) Switch Q is OFF

Figure 1.2 Switching Sequences of the Boost Converter

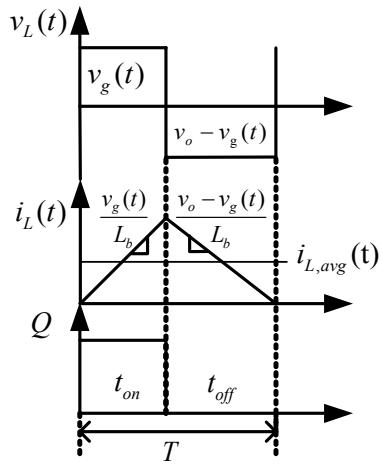


Figure 1.3 One-cycle waveform of the Boost Converter

Operation Principle

Switch Q is ON ：When Q turns on, the rectifier diode D is reverse-biased and output capacitor Co supplies load current. The rectified AC line input voltage $V_g(t)$ is applied to the inductor L_b so that inductor current i_L ramps up linearly and that can be expressed as:

$$i_L(t_{on}) = \frac{V_g(t)}{L_b} \qquad (1.1)$$

Switch Q is OFF：When Q turns off, the voltage $V_o - V_g(t)$ is applied to inductor L_b, and the polarity on the inductor L_b is reversed. The diode D is forward-biased in this stage. The energy stored in the inductor L_b is delivered to supply load current and output capacitor C_o. The inductor current i_L can be expressed as:

$$i_L(t_{off}) = \frac{V_o - V_g(t)}{L_b} \qquad (1.2)$$

Controlled ON-Time：The on-time of the power MOSFET Q is determined by the output of the error amplifier which monitors the preregulators output voltage. With a low-bandwidth error amplifier, the feedback signal is almost constant during a half AC cycle, resulting a fixed on time of the power MOSFET at a specific AC voltage and some certain output power level. Therefore, the peak inductor current $i_{L,pk}$ will automatically follow the input voltage $V_g(t)$, achieving a natural power factor correction mechanism. Fig 1.4 shows the typical inductor current waveform during a half AC cycle.

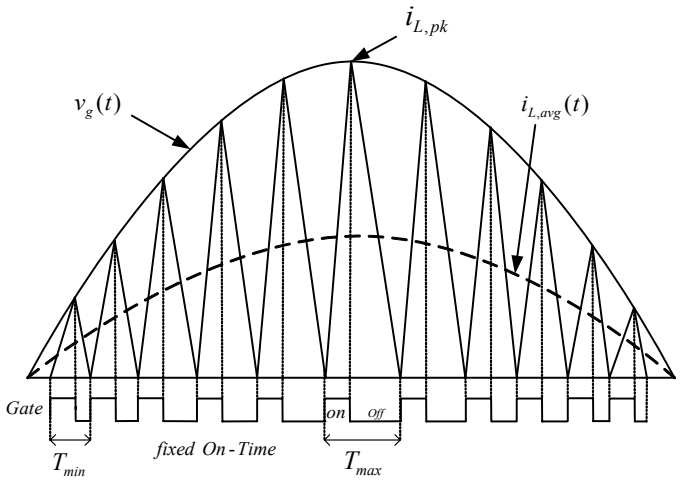


Figure 1.4 Controlled ON-Time Inductor Current Waveform

Referring to Fig. 1.3, considering one switching period the average inductor current $i_{L,avg}(t)$ can be calculated by the average area of triangle waveform of inductor current:

$$i_{L,avg}(t) = \left[V_g(t) + \frac{V_g(t)^2}{V_o - V_g(t)} \right] \cdot \frac{\left[\frac{t_{on}}{T_s} \right]^2 \cdot T_s}{2 \cdot L_b} \qquad (1.3)$$

2. BLOCK OPERATION DESCRIPTION

2.1 Multi-Vector Error Amplifier

The SG6961 has a trans-conductance type amplifier that could provide better dynamic performance. Referring to Fig 2.1, the error amplifier output V_{EA} is compared with a saw-tooth waveform to generate a fixed on-time. In order to achieve a low input current THD, the variation of the on-time within one input AC cycle should be very small. Therefore, the bandwidth of the feedback loop should be set below 20 Hertz to maintain a constant on-time for a line half-cycle. Connecting a capacitance C_{EA} such as 1uF between COMP and GND is suggested.

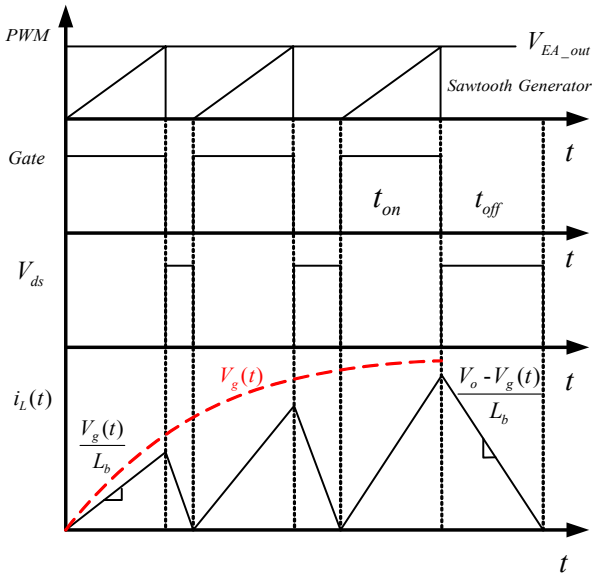


Figure 2.1 Operation Waveforms of fixed on time technique

For fast transient response and precise clamping of the output voltage overshoot and undershoot, the SG6961 has a built in multi-vector error amplifier. Fig 2.2 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds +6% and -8% of the reference voltage, the multi-vector error amplifier will adjust its output impedance to increase the loop response.

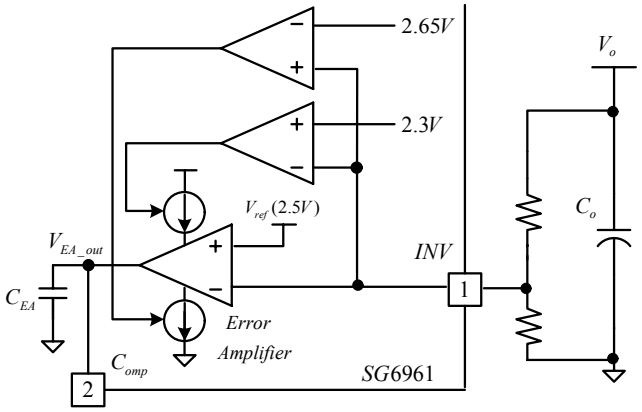


Figure 2.2 Block Diagram of the Multi-Vector Error Amplifier

2.2 THD Optimization

As discusses previously, the SG6961 uses the controlled on-time technique to achieve power factor correction mechanism. However, in order to get better THD at light load condition, especially at high input voltage, a THD optimization circuit is inserted into the SG6961. With this internal THD optimization circuit, the on-time of the power MOSFET will be modulated to further improve the THD performance. The calculated on time variation within one line voltage period with the fixed on-time technique and after the THD optimization is added are shown in Fig. 2.3. Also, the calculated input current waveform is shown in Fig. 2.4.

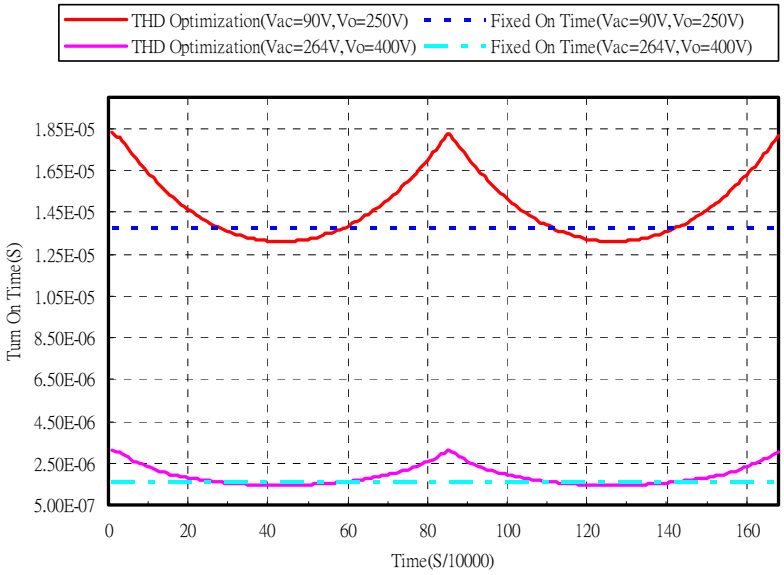


Fig 2.3 MOS turn on time calculational curve (Before and after the THD optimization circuit is added)

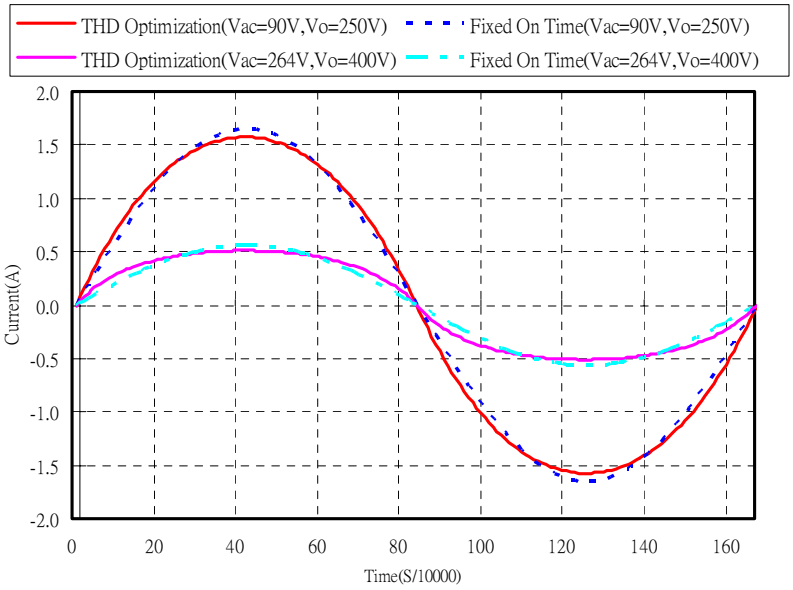
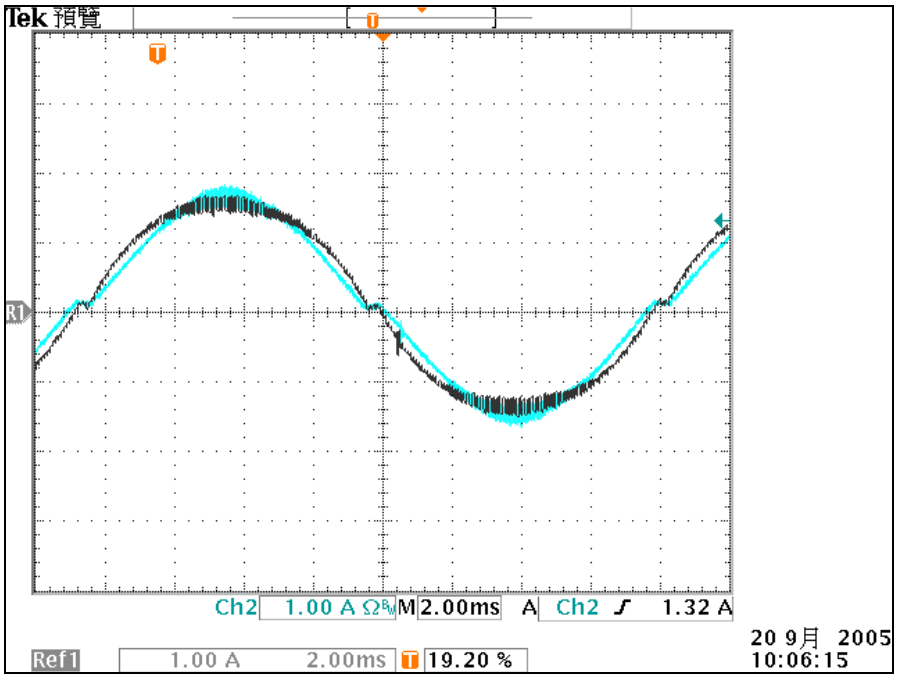


Fig 2.4 Calculated waveforms of the input current (Before and after the THD optimization circuit is added)

Fig 2.5 shows the measured input current on the example circuit board (the detail design guideline is described in chapter 3.6).



Ch2: Before THD Optimization (1A/div) ; Ref1: After THD Optimization (1A/div)

Fig 2.5 Measured waveforms of the input current (Before and after the THD optimization circuit is added)

Fig 2.6 shows the measured THD performance on the example circuit board (the detail design guideline is described in chapter 3.6).

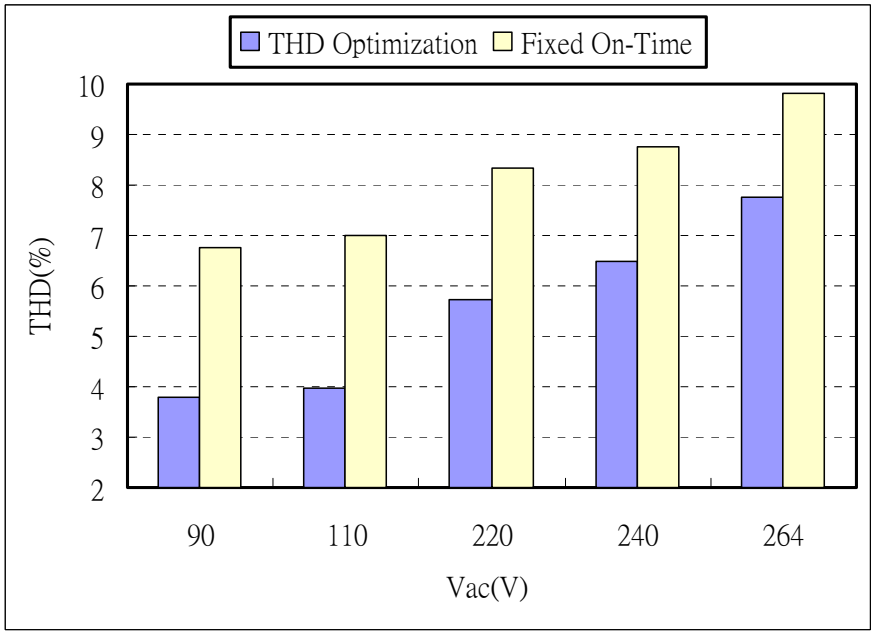


Fig 2.6 Measured THD result at Full load condition (Fixed on-time technique versus THD optimization)

2.3 Over/under-Voltage Protection

Over/under-voltage protection is built in to provide better protection, and it is by detecting and examining the voltage on INV pin. When the voltage V_{INV} exceeds 2.75V due to abnormal conditions, the internal OVP protection circuit is triggered to disable the PWM output. Over-voltage conditions are usually caused by a feedback open-looped. A de-bounce time around 35uS is added to prevent false triggering. Once the voltage V_{INV} is smaller than 0.45V due to short circuit conditions, PWM output will also be turned off.

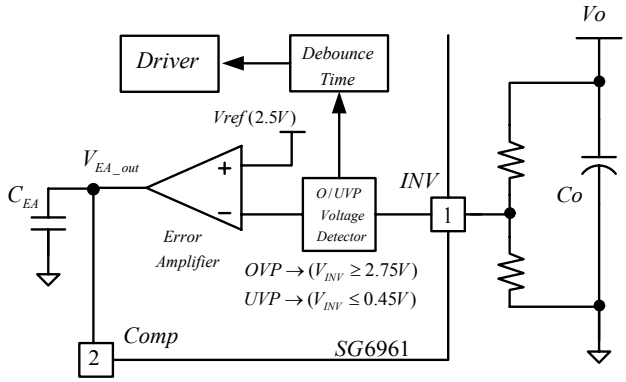


Figure 2.7 Block Diagram of the Over/ Under- Voltage Protection

2.4 Zero Current Detection

Fig 2.8 shows the block diagram of the zero current detection. The zero inductor current detection is performed by sensing the information on an auxiliary winding of the PFC inductor. Referring to Fig 2.9, when Q turns off, the stored energy of the inductor starts to release to the output. The voltage on the ZCD will start to decrease when the energy in the inductor dries out. Once the ZCD voltage is lower than the threshold voltage (1.75V TYP.), the PWM output will be high again and initiates a new switching cycle. The output rectifier will always be turned off with zero current, so the converter will work in boundary mode conditions and the power MOSFET will be switched on with low voltage to minimize the switching losses.

Once the ZCD voltage is smaller than the disable threshold voltage (around 0.25V) for a duration of about 800uS, the PWM output will be disabled.

To prevent high switching frequency during light load conditions an inhibit timer function is built in to limit the maximum switching frequency.

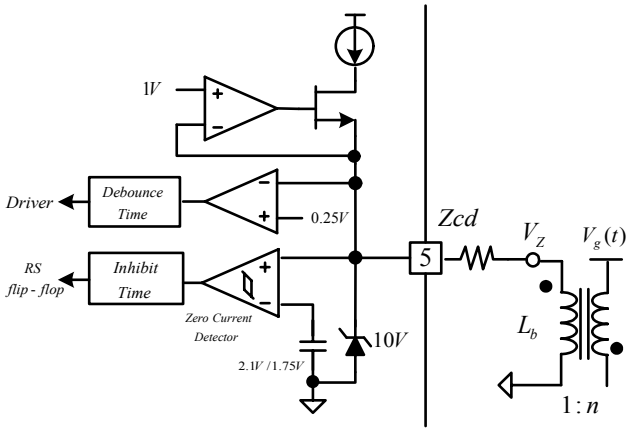


Figure 2.8 Block Diagram of the Zero Current Detection

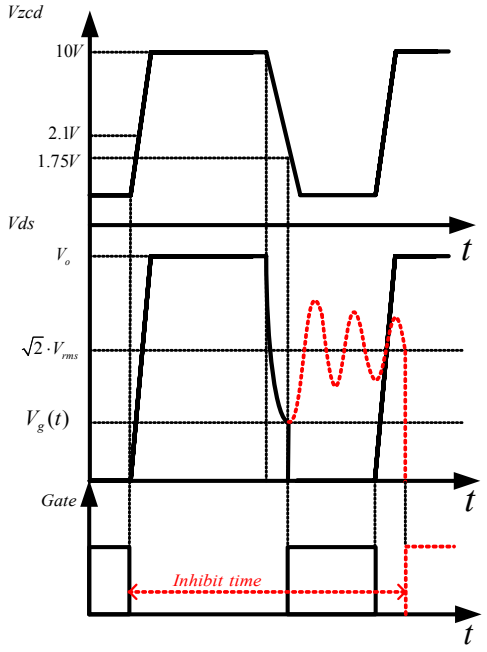


Figure 2.9

2.5 Maximum On-Time Operation

The on-time of the power MOSFET is varied with the output power and the AC input voltage. While the AC input voltage decreases, the on-time will increase accordingly. The maximum on-time limit $t_{on,\max}$, can be programmed by the resistor connected between MOT and GND pin.

$$t_{on,\max} = R_{mot}\,(k\Omega)\cdot\frac{25}{24}(u\sec) \qquad (2.1)$$

The range of the maximum on-time is designed to be within 10~50usec, and 25usec is recommended.

2.6 Vcc Over-Voltage Protection

A Vcc over-voltage protection has been built in to avoid damage when the voltage VDD exceeds the internal threshold due to an open loop failure. Once the protection is triggered, the PWM output will be turned off.

2.7 Peak Current Limiting

The switch current is sensed across a resistor and then supplied to an input terminal of a comparator. A voltage higher than 0.82V threshold voltage on CS pin will immediately terminate the current switching cycle, thus activating cycle-by-cycle current limiting.

2.8 Leading-Edge Blanking

A turn-on spike will inevitably occur at the CS pin when the power MOSFET is switched on. At the beginning of each switching pulse, the current-limit comparator is disabled for around 350nsec to avoid premature termination. The gate drive output cannot be switched off during the blanking period.

2.9 Under-Voltage Lockout (UVLO)

The turn-on and turn-off threshold voltages are fixed internally at 12V and 9.5V, respectively, for the SG6961. This hysteresis behavior will guarantee a one shot start-up, as long as a proper start-up resistor and hold-up capacitor are used.

2.10 Output Driver

With a low ON-resistance and a high current driving capability, the output driver can easily drive an external capacitive load larger than 3000pF. Cross conduction currents are avoided to minimize heat dissipation, allowing the efficiency and reliability to be improved. This output driver is internally clamped by a 17V Zener diode.

2.11 Lab Note

Before rework or solder/desolder on the power supply, it is suggested to **discharge the primary capacitors by external bleeding resistor**. Otherwise the PWM IC may be destroyed by external high voltage during solder/desolder.

3. DESIGN GUIDELINE

3.1 PFC Inductor Design

As shown in Fig 3.1, considering one AC line voltage cycle, the minimum switching frequency $f_{s.\min}$ will occur at the peak of the AC line voltage. To avoid audible noise, the minimum switching frequency $f_{s.\min}$ must be above audible frequency. The appropriate inductance can be calculated by equation (3.1). The minimum switching frequency $f_{s.\min}$ may happen in AC maximum or minimum input voltage, depending on the output voltage. Therefore, you need to calculate both the maximum and the minimum input voltages, and then choose the lower inductance value.

$$L_b = \frac{\eta \cdot V_{pk}^{\ 2} \cdot (V_o - V_{pk})}{4 \cdot P_o \cdot V_o \cdot f_{s.\min}} \qquad (3.1)$$

where L_b is the PFC inductor, η is conversion efficiency, V_{pk} is the peak of the AC line voltage, P_o is rated output power, V_o is PFC output voltage, $f_{s.\min}$ is the minimum switching frequency

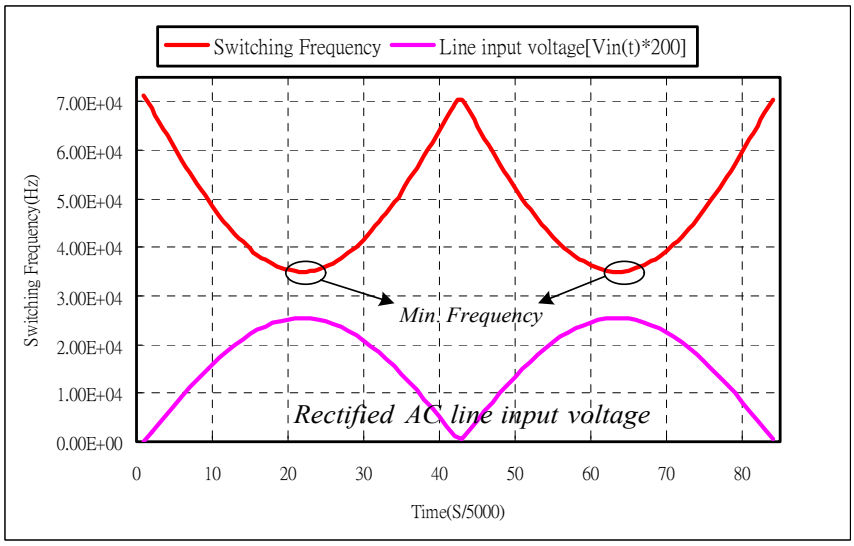


Fig 3.1

The peak inductor current $i_{L,pk}$ can be expressed as follows:

$$i_{L,pk} = \frac{4 \cdot P_o}{\sqrt{2} \cdot V_{rms.\min} \cdot \eta} \qquad (3.2)$$

where $V_{rms.\min}$ is the minimum input line rms voltage.

With the internal THD optimization circuit, the real peak inductor current will be smaller than calculated. Usually, the real peak current is around 95% of calculated value.

3.2 Determine Current-Sense Resistor

The MOSFET on-time and the input current will increase with the decreasing AC input voltage or increasing load. As mentioned in chapter 2.5, the SG6961 can establish the maximum on-time limit (25usec is recommended) of power MOSFET. Once the voltage on Current-Sense pin reaches the internal limit Vcs, 0.82V typically, the SG6961 will stop the PWM output immediately. Thus, the maximum output power can be designed by the current-sense resistor and maximum on-time limit. In general operation, the maximum on-time will occur at minimum AC input voltage and maximum loading conditions.

When the output power increases from full load to maximum load, the on-time will be restricted to the maximum on-time limit first, then encounter with current limit. In the design example which will be introduced in chapter 3.6, the voltage on the Current-Sense pin is set to 0.57V at full load and minimum input voltage conditions. At this condition, the maximum power is about 156% of full load at minimum input voltage condition. The current-sense resistor can be calculated from equation 3.3. The calculated curve of the MOSFET turn on time at different loading conditions are shown in Fig 3.2. The calculated waveforms of the PFC inductor current at two kinds of current limit are shown in Fig 3.3.

$$R_s = \frac{0.57V}{i_{L,pk} \cdot 95\%} \qquad (3.3)$$

The SG6961 current-sense limit Vcs is 0.82V typically.

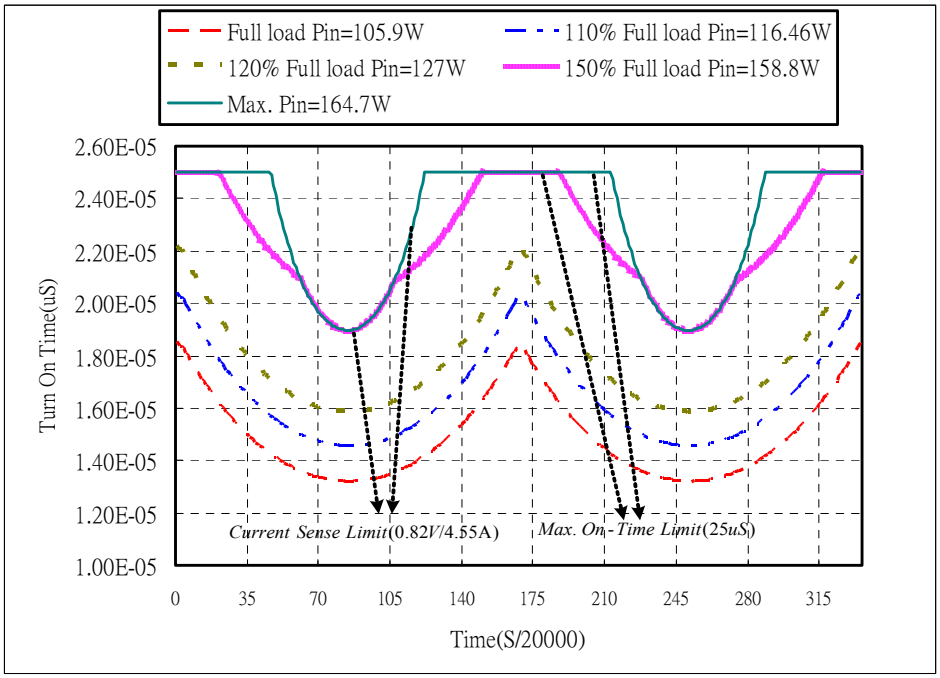


Fig 3.2 Calculated curve of the MOSFET turn on time at different loading conditions

Another example is set the Current-Sense pin to 0.7V at full load and minimum input voltage conditions, then the maximum power will be around 133% of full load at minimum input voltage condition. At full load and minimum input voltage condition, to establish the voltage of current-sense voltage between from 0.55V to 0.7V is suggested.

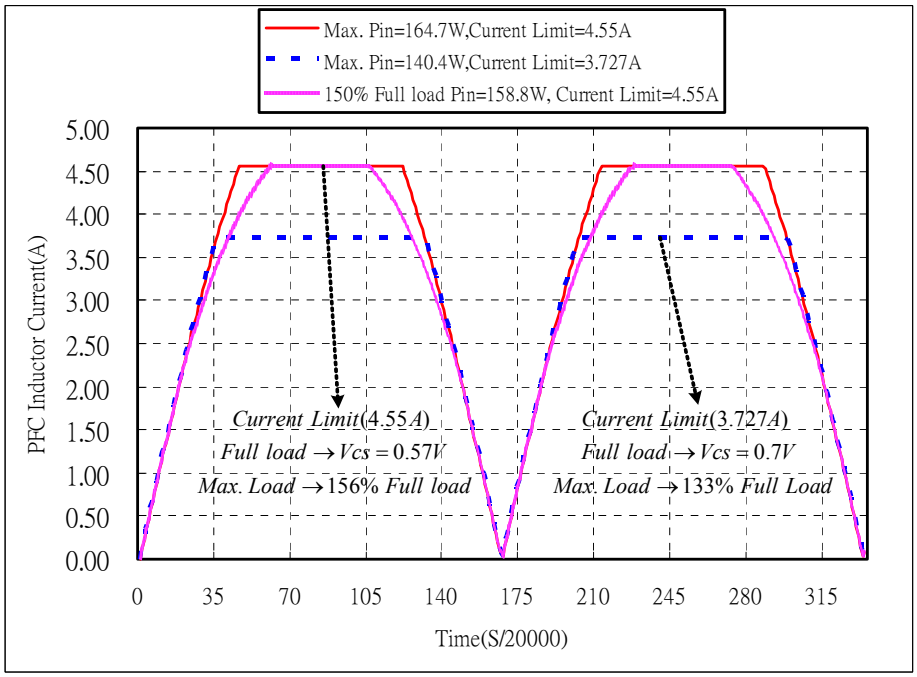


Fig 3.3 Calculated waveforms of the PFC inductor current at two kinds of current limit

From Faraday's law, the number of turns for PFC inductor can be obtained:

$$N_b = \frac{L_b \cdot i_{L,pk}}{B_{\max} \cdot A_e} \cdot 10^6 \qquad (3.4)$$

Where A_e is the effective area of the core-section

$B_{\max}$ is saturation magnetic flux density

3.2 Determine the Auxiliary Winding

The SG6961 can perform zero current detection by sensing the information on an auxiliary winding of the PFC inductor. As discusses previously, when the ZCD voltage is lower than the threshold voltage (1.75V TYP.), the PWM output is high again and initiates a new switching cycle. However, there is a prerequisite, the zero current detector voltage must exceed the rising edge threshold voltage (2.1 TYP) before it falls below 1.75V. The minimum rising edge voltage of zero current detector input will occur at the peak of the highest AC line voltage, that is to be equal to $(V_o - \sqrt{2} \cdot V_{rms.\max})/n$, and it must be larger than the ZCD input rising edge threshold voltage (2.1V TYP). Also the ZCD voltage V_{zcd} is recommended to be established as high as 120 percent of 2.3V to have a safe margin, therefore the number of turns for auxiliary winding is obtained as follows:

$$N_{aux} = \frac{V_{zcd} \cdot 1.2}{V_o - \sqrt{2} \cdot V_{rms.\max}} \cdot N_b \qquad (3.5)$$

where $V_{rms.\max}$ is the maximum input line rms voltage.

V_{zcd} is the rising edge voltage of zero current detector input.

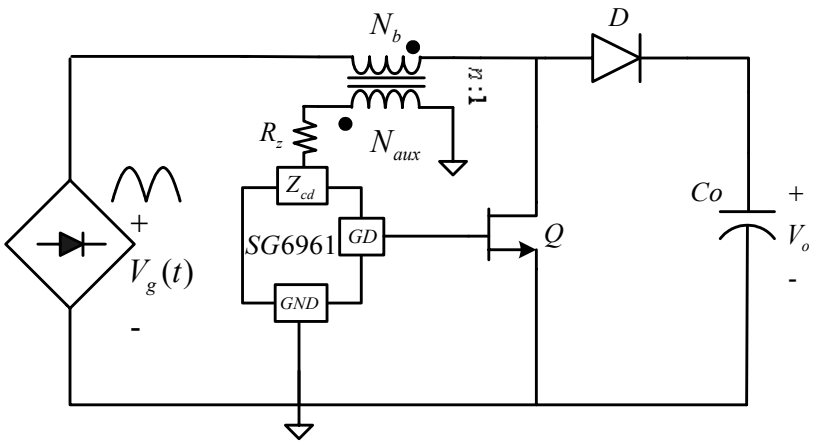


Figure 3.3. Simplified power stage

Where the resistor Rz is set to about 68k ohm.

3.3 Calculate the On-time $t_{on.fix}$

The fixed on-time for the specific output power, inductor, and input voltage can be calculated by equation (3.5):

$$t_{on.fix} = \frac{2 \cdot P_o \cdot L_b}{V_{rms}^{\ 2} \cdot \eta} \qquad (3.6)$$

Where L_b is the PFC inductor, η is the conversion efficiency, P_o is the maximum rated output power, V_{rms} is the input line rms voltage.

3.4 Determine the Output Capacitor C_o

The output capacitor is determined by the requirement of sufficient hold-up time t_{hold} .

$$C_o = \frac{2 \cdot P_o \cdot t_{hold}}{(V_o^{\ 2} - V_{o.\min}^{\ 2}) \cdot \eta} \qquad (3.7)$$

Where t_{hold} is the output capacitor hold-up time, which is measured from the time the AC input turns off to before the output voltage falls below the minimum operating voltage of the following DC/DC stage.

And the output ripple voltage ΔV_o is expressed as follows:

$$\Delta V_o = \frac{P_o}{\omega \cdot C_o \cdot V_o} \qquad (3.8)$$

Where $\omega = 2 \cdot \pi \cdot f$, f is AC line frequency

I_o is the output current

3.5 Determine the Compensation Capacitor C_{EA}

As discusses previously, in order to achieve a low input current THD, the variation of the on-time within one input AC cycle should be very small. To achieve this, the bandwidth should be lower than 20 Hertz. The capacitance C_{EA} connected between COMP and GND can be obtained as follows:

$$C_{EA} = \frac{g_m}{2 \cdot \pi \cdot BW} \qquad (3.8)$$

The error amplifier is a trans-conductance amplifier that converts voltage to current with a 125umho output conductance. Where BW is PFC control loop bandwidth and establish it as 20Hz.

3.6 Design Example

This section shows a design example of a 90W (19V/4.74A) adaptor. From the specification, all critical components are treated and final measurement results are given.

The basic design specification are shown as following：

- AC Input Voltage Range V_{rms} : 90 ~ 264 Vac
- Rated Output Power P_o : 90 W
- Minimum Switching Frequency $f_{s.\min}$: 35KHz
- High Regulated Output Voltage: 400V (at 180 ~ 264Vac)
- Low Regulated Output Voltage: 250V (at 90 ~ 132Vac)

Based on the given design guideline, the critical parameters are calculated and summarized as follows:

Table 1. Critical system parameters

L_b	530uH	$t_{on.fix}(90V_{rms})$	13.86 uS
i_{pk}	3.327A	$t_{on.fix}(132V_{rms})$	6.44 uS
N_b	65T	$t_{on.fix}(180V_{rms})$	3.46 uS
N_{aux}	7T	$t_{on.fix}(264V_{rms})$	1.61 uS
C_o	68uF/450V	$\Delta V_o(V_o = 250V)$	14.043V
C_{EA}	1uF	$\Delta V_o(V_o = 400V)$	8.77V

3.7 Reference Circuit

The complete circuit diagram is shown in Fig 3.2. And the bom List of the PFC stage is shown in Table 2.

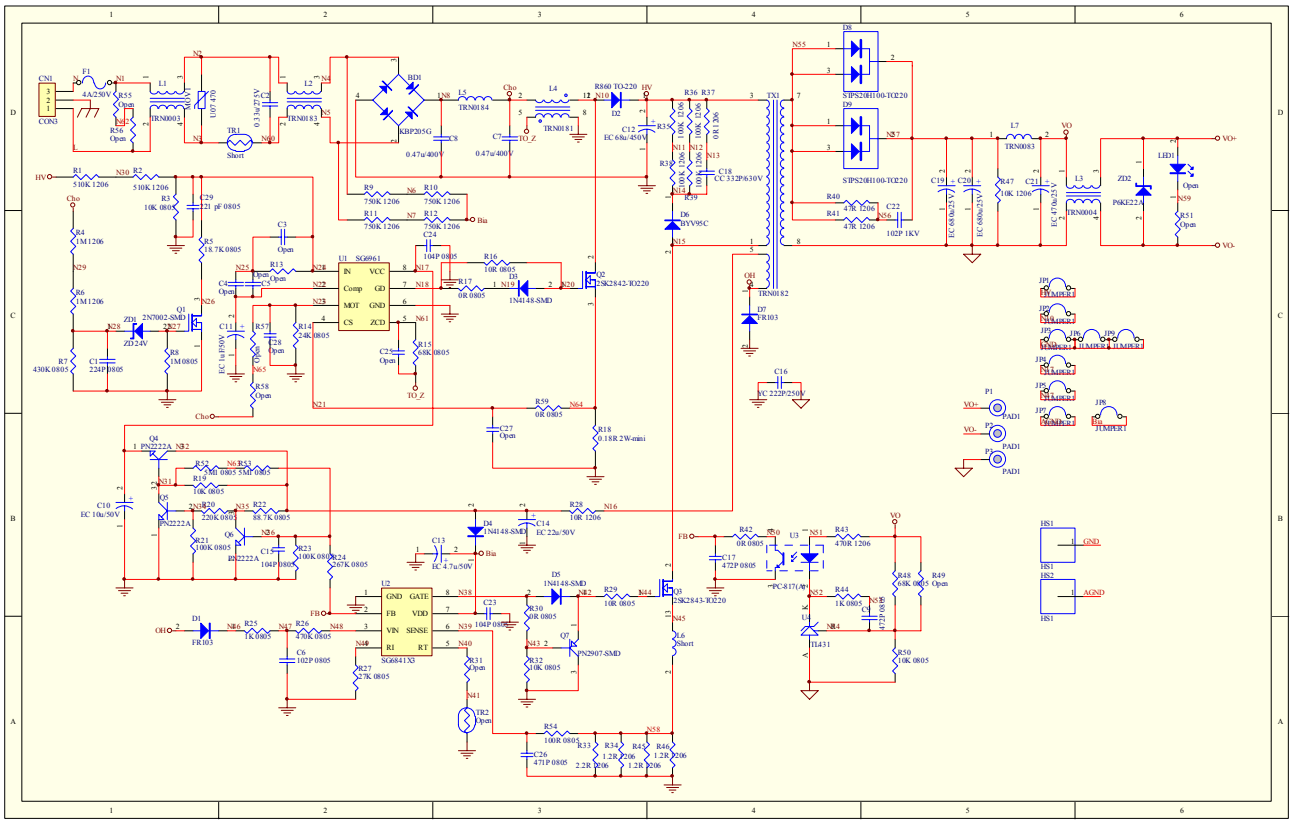


Figure 3.2 Application Circuit Diagram(90W/19V)

Table 2. BOM List of PFC Stage

Reference	Components	Reference	Components
F1	4A/250V	C2	0.33u/275V
R1	510K	C3	Open
R2	510K	C4	Open
R3	10K	C5	Open
R4	1M	C7	0.47uF/400V
R5	18.7K	C8	0.47uF/400V
R6	1M	C11	2.2uF/50V
R7	430K	C12	68uF/450V
R8	1M	C24	104 pF
R13	Open	C25	Open
R14	24K	C27	Open
R15	68K	C28	Open
R16	10 ohm	C29	221pF
R17	0 ohm	Q1	2N-7002
R18	0.18 ohm /2W	Q2	2SK-2482/TO-220
R55	Open	BD1	KBP205G
R56	Open	ZD1	ZD24V
R57	Open	D2	R860/TO-220
R58	Open	D3	1N4148
R59	0 ohm	L1	1mH
MOV1	470V/7D	L2	13mH
TR1	055	L4	RM-10 / 530uH
U1	SG6961	L5	400uH
C1	224 pF		

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LIFE SUPPORT

System General's products are not designed to be used as components in devices intended to support or sustain human life. Use of System General's products in components intended for surgical implant into the body, or other applications in which failure of System General's products could create a situation where personal death or injury may occur, is not authorized without the express written approval of System General's Chief Executive Officer. System General will not be held liable for any damages or claims resulting from the use of its products in medical applications.

MILITARY

System General's products are not designed for use in military applications. Use of System General's products in military applications is not authorized without the express written approval of System General's Chief Executive Officer. System General will not be held liable for any damages or claims resulting from the use of its products in military applications.

RIGHT TO MAKE CHANGES

System General reserves the right to change this document and/or this product without notice. Customers are advised to consult their System General sales representative before ordering.