ATAVRFBKIT / EVLB001 Dimmable Fluorescent Ballast

User Guide

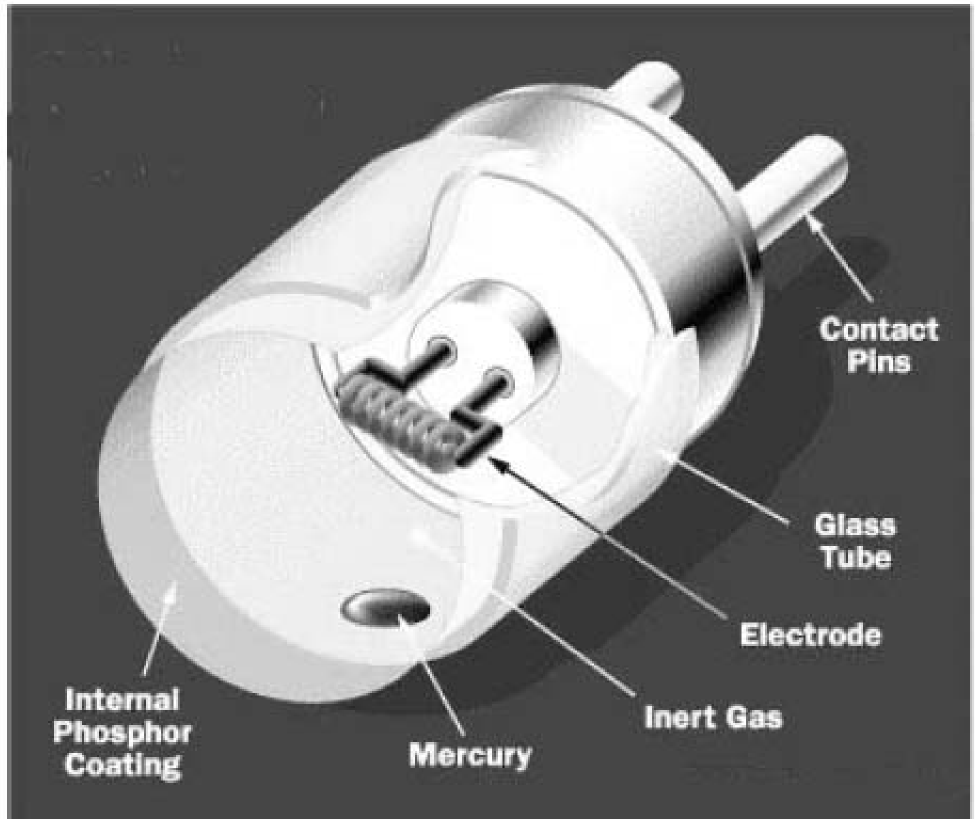
Section 1

Introduction

Efficient fluorescent lamps and magnetic ballasts have been the standard lighting fixture in commercial and industrial lighting for many years. Several lamp types, rapid start, high output, and others are available for cost effective and special applications. But incandescent lamps, in spite of the poor light to power ratio typically one fourth of fluorescent, offer one feature - dimming - that hasn't been available in fluorescent lamps until now. Dimming allows the user to conserve electrical power under natural ambient light or create effects to enhance mood or image presentation and projection for example.

Typical rapid start fluorescent lamps have two pins at each end with a filament across the pins. The lamp has argon gas under low pressure and a small amount of mercury in the phosphor coated glass tube. As an AC voltage is applied at each end and the filaments are heated, electrons are driven off the filaments that collide with mercury atoms in the gas mixture. A mercury electron reaches a higher energy level then falls back to a normal state releasing a photon of ultraviolet (UV) wavelength. This photon collides with both argon assisting ionization and the phosphor coated glass tube. High voltage and UV photons ionize the argon, increasing gas conduction and releasing more UV photons. UV photons collide with the phosphor atoms increasing their electron energy state and releasing heat. Phosphor electron state decreases and releases a visible light photon. Different phosphor and gas materials can modify some of the lamp characteristics.

Figure 1-1. Fluorescent Tube Composition



Since the argon conductivity increases and resistance across the lamp ends decreases as the gas becomes excited, an inductance (ballast) must be used to limit and control the gas current. In the past, an inductor could be designed to limit the current for a narrow range of power voltage and frequency. A better method to control gas current is to vary an inductor's volt-seconds to achieve the desired lamp current and intensity. A variable frequency inverter operating from a DC bus can do this. If the inductor is part of an R-L-C circuit, rapid start ignition currents, maximum intensity, and dimming currents are easily controlled depending on the driving frequency versus resonant frequency.

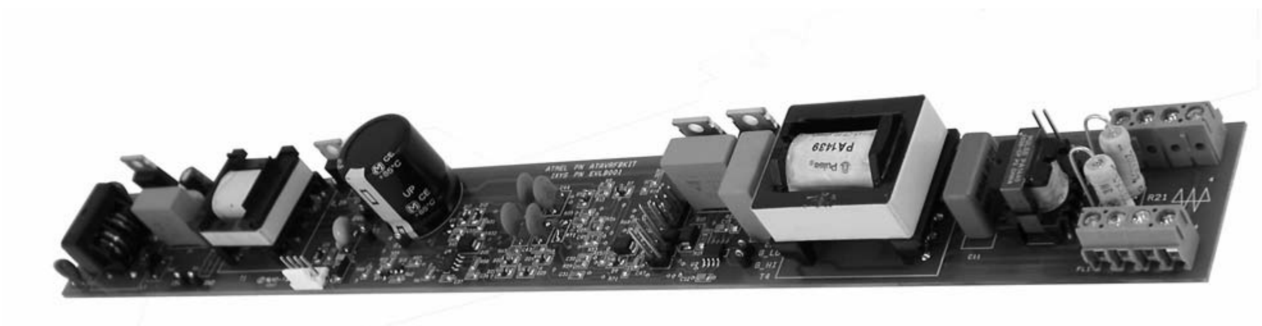
A ballast should include a power factor corrector (PFC) to keep the mains current and voltage in phase with a very low distortion over a wide range of 90 to 265 VAC 50/60 Hz. With microcontroller control, economical remote analog or digital control of lamp function and fault reporting are a reality. Moreover, adjusting the lamp power to correspond with human perceived light level is possible. An application specific microcontroller brings the designer the flexibility to increase performance and add features to the lighting product. Some of the possible features are described here in detail. The final design topology is shown in the block diagram of Figure 2-1.

Now, a new way of dimming fluorescent lamps fills the incandescent/fluorescent feature gap plus adds many additional desirable features at a very reasonable cost.

1.1 General Description

Fluorescent ballast topology usually includes line conditioning for CE and UL compliance, a power factor correction block including a boost converter to 380 V for universal input applications and a half bridge inverter. By varying the frequency of the inverter, the controller will preheat the filaments (high frequency), then ignite the lamp (reducing the frequency). Once the lamp is lit, varying the frequency will dim the light. The Atmel AT90PWMx microcontroller can be programmed to perform all these functions.

Figure 1-2. Ballast Demonstrator Board



1.2 Ballast Demonstrator Features

- Automatic microcontroller dimmable ballast
- Universal input – 90 to 265 VAC 50/60 Hz, 90 to 370 VDC
- Power Factor Corrected (PFC) boost regulator
- Power feedback for stable operation over line voltage range
- Variable frequency half bridge inverter
- 18W, up to 2 type T8 lamps
- Automatic dimmable single lamp operation
- Automatic detection of Swiss, DALI, or 0 – 10V dimming control
- Very versatile power saving options with microcontroller design for most functions

Section 2

Ballast Demonstrator Device Features

2.1 Atmel Supported Products

AT90PWMx Microcontroller

- High speed comparator for PFC zero crossover detection
- High speed configurable PWM outputs for PFC and half bridge inverter
- 6 Analog inputs for A/D conversion, 2.56V reference level
- 3 Digital inputs used for the dimming control input
- 3 High speed PWM outputs used for the PFC and half bridge driver
- A fully differential A/D with programmable gain used for efficient current sensing
- SOIC 24 pin package
- Low power consumption in standby mode

2.2 IXYS® Supported Products

IXI859 Charge pump with voltage regulator and MOSFET driver

- 3.3V regulator with undervoltage lockout
- Converts PFC energy to regulated 15VDC
- Low propagation delay driver with 15V out and 3V input for PFC FET gate

IXTP3N50P MOSFET

- 500V, low R_{DS} (ON) power MOSFET, 3 used in design

IXTP02N50D depletion mode MOSFET

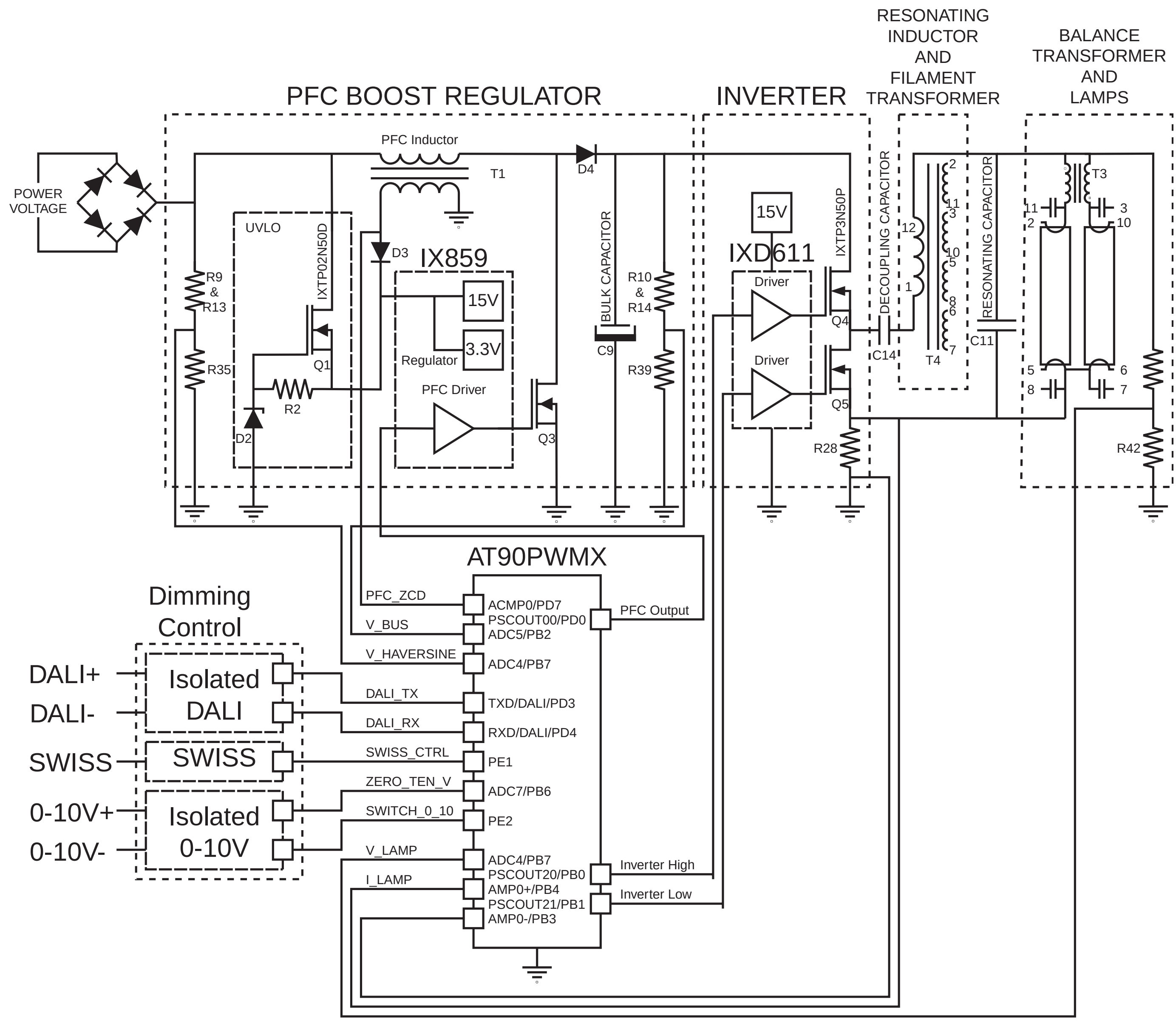
- 500V, 200mA, normally ON, TO-220 package and configured as current source

IXD611S MOSFET driver

- Up to 600mA drive current
- half bridge, high and low side driver in a single surface mount IC
- Undervoltage lockout

LDA111S Optocoupler (by Clare Inc., an IXYS company)
- 100mA continuous load rating
- 3750V_{RMS} input to output isolation

Figure 2-1. Ballast Demonstrator Block Diagram



Section 3

Microcontroller Port Pin Assignments

PD0	PCOUT00	PFC_OUTPUT - To IXI859 FET driver input
PD1	PSCIN0	DUAL_LAMP - Dual lamp detection
PD3	TXD/DALI	DALI_TX - DALI transmit line
PD4	RXD/DALI	DALI_RX - DALI receive line
PD5	ADC2	LAMP_EOL - Not supported in hardware or software
PD6	ADC3	V_LAMP - Rectified lamp voltage sense, missing lamp, open or shorted filament, preheat, ignition & run.
PD7	ACMP0	PFC_ZCD - Comparator for PFC zero current crossing sense
PB0	PSCOUT20	INVERTER_L - Low side half bridge driver output
PB1	PSCOUT21	INVERTER_H - High side half bridge driver output
PB2	ADC5	V_BUS - 380VDC bus voltage sense for regulation.
PB3	AMP0-	GND - Diff amp - A/D, 1 ohm bus current shunt resistor
PB4	AMP0+	I_LAMP - Diff amp + A/D
PB5	ADC6	TEMPERATURE - Ambient temperature in lamp housing
PB6	ADC7	ZERO_TEN_V - 0 to 10V control input
PB7	ADC4	V_HAVERSINE - Haversine input sense.
PE0	RST#	RESET - Reset pin for zero crossing detector
PE1	PE1	SWISS_CTRL - SWISS Control input
PE2	ADC0	SWITCH_0_10 - Switch ON/OFF for 0-10V interface

Section 4

Ballast Demonstrator Operation

4.1 General Requirements

- Constant power as determined by DALI or analog power setting
  380 volt DC bus as provided by a power factor correcting boost regulator (PFC)
  100% to 2% dimming setting

- One or two lamps, type T8 of 18W
  Ballast to compensate automatically
  Hardware is capable of up to 40W per lamp

- Line voltage of 90 to 265 VAC, 50 or 60 Hz

- Control method
  DALI power control – auto recognition of control means
  0-10 volt power control – auto recognition of control means
  One touch “Swiss” dimming100% ON after ignition then dim to the last or current programmed value, if any.

4.2 Startup features

Software based features that are not fully implemented at time of delivery.

End users are invited to develop features based on the following characteristics.

•Auto re-strike

-Missing lamp detection allows a default power of 100% on the remaining lamp with no dimming.

-Open filament detection for one or two lamps as determined by combination of 380VDC current plus lamp voltage prior to ignition.

-On board physical jumper to set for one or two lamp normal operation.

•Shorted filament

-Detection by voltage sense across lamp during preheat. 380VDC current monitor detects over current limit upon startup. The microcontroller will sense the expected DC current to the half bridge and resonant circuit relative to the drive frequency.

4.3 Circuit Topology

Input filter with varistor for noise suppression and protection.

PFC / boost circuit including IXI859 MOSFET driver

AT90PWM2 microcontroller 24 pin SOIC

half bridge driver

half bridge power MOSFET stage for up to 2 lamps

Voltage driven filaments for wider lamp variety and better stability under all conditions

380VDC bus voltage after the PFC boost

4.4 Startup and PFC Description

Upon application of main power, the microcontroller does not drive the PFC MOSFET Q3. The C9 capacitor is charged to the peak line voltage.

The depletion FET Q1 and the Zener Diode provide a DC voltage with enough current to supply the control portion of the ballast.

As soon as the microcontroller request the ballast to start, the PFC is enabled according to the following sequence.

Microcontroller checks that the DC bus voltage is 0.9 times the haversine peak and the under voltage lockout (UVLO) requirements are met, a series of fixed width soft-start pulses are sent to the PFC MOSFET (Q3) at 10 µS at a 20 kHz rate. At very low load currents the bus voltage should rise to 380V. If the bus rises to 410 VDC all PFC pulses stop. As the 380V drops, the zero crossing detector PD7 starts to sense a zero crossing from the PFC transformer secondary. A 380V DC bus and a zero crossing event starts the PFC control loop.

Checks are made for the presence of the rectified power (haversine) and bus voltage throughout normal operation. Mains sense at PB7 < 0.848 (90 VAC) or > 2.497 (265 VAC) peak faults the PFC to off, turns off the PFC MOSFET (Q3) and initiates a restart.

The control consists of measuring the error between VBUS and 380V (2.27V at PB2) to determine the PFC drive pulse width (PW). The PW is proportional to the error, and has to be constant over a complete half period. The update is done each time the haversine reaches zero.

The maximum current the PFC MOSFET (Q3) can sustain is 4.5A. The relation between PW and the peak current in PFC MOSFET (Q3) is:

PW = t = L x Ipk / Vhaversine_max

With L at 700µH and Ipk at 4.5A, PWmax = 8.5µS at high line (265 Vrms).
With L at 700µH and Ipk at 4.5A, PWmax = 24.7µS at high line (90 Vrms).

This also effectively limits the FET dissipation under upset conditions. Under normal operation, a pulse width maximum of 25µS is allowed for a maximum bus voltage error with the high line limitation. Regulation of 1% of the VBUS is achieved with this control scheme.

After the PFC FET ON pulse, the PFC inductor flyback boosts the voltage through the PFC diode to the bulk filter capacitor. The boost current decays as measured by the inductor secondary. After the current goes to zero, the next pulse is started. This ensures operation in a critical conduction boost mode. The current zero crossing detection of PD7 sets the PFC off time. This off time is effectively proportional to the haversine amplitude with the lowest PFC frequency occurring at the haversine crest and the highest frequency at the haversine zero. Because of the haversine voltage and di=v*dt/L, the mains current envelope should follow the voltage for near unity power factor. This assumes a nearly constant error (di) of the 380 VDC bus over each haversine period.

The PFC ON time is modified proportionally to the error between 380V and the actual value of the bus. In case the Vbus reaches the overshoot value of 410V the pulse is reduced to 0.

This control loop will determine the regulation response to ripple current on the 380V bulk filter cap and the loads for a specific application design requirements.

4.4.1 System Sequential Step Description

Main voltage applied.

Undervoltage lockout (UVLO) released.

IXI859 voltage regulator supplies 3.3V to microcontroller.

Power microcontroller ON in low current standby mode.

Disable half bridge drive output PB0 & PB1

Disable PD5 comparator (Not implemented).

PB7, scaled haversine voltage must be >0.848 Vmin (90VAC) & <2.497 (265VAC) Vmax (haversine peak) for the PFC to start.

-Check AC line condition every 200 mS maximum (10 cycles of 50 Hz).

-If the check fails, halt PD0, PB0, PB1 and set line voltage alarm high or low. Do not restart until line within specs to protect PFC.

PD0 soft start PFC with 10µS pulses at 50µS period for 800µS.

Monitor comparator at PD7 for change 1 to 0 indicating a zero crossing of the PFC inductor secondary voltage. This occurs after the 10µS start pulse burst.

If no PD7 change and after 800µS halt PD0, wait 1 second and provide PD0 with 10µS pulses for 800µS. Try 10 times and if no crossing, set PFC alarm.

After PD7 comparator transition and 380VDC (2.368V at PB2), enable PFC control loop.

-Set PB2 (380VDC sense) setpoint to 2.368V with deadband.

-If PB2 > 2.50V then inhibit PD0 pulse.

-If PB2 = < 2.368V then use the control loop to establish the PD0 PFC pulse width.

Limit pulse width to 25uS or as determined by the haversine peak voltage.

After PD0 PFC pulse, wait until PD0 = 0 & PD7 = 0 (PD0 off time) then enable PD0 pulse according to table of error from setpoint.

-If PB2 (380V sense) > A/D 255 = overshoot.

When PB7 < 0.100V, limit PD0 minimum to 5 µS to reduce distortion at haversine zero crossover.

4.5 Lamp Operation Description

T4 primary and C11 form a serial resonant circuit driven by the output half bridge. Since the output is between 380V and 0V, DC isolation is provided by C14 to drive the lamp circuit with AC. The lamp is placed across the resonating capacitor C11. The lamp filaments are driven by windings on T1 secondaries to about 3Vrms so that the resonating inductor current provides the starting lamp filament current.

Initially, the lamp is started at a frequency well above resonance at 80 kHz before ramping down to 55 kHz for ignition. 80 kHz provides a lagging power factor where most of the drive voltage appears across the inductor. A smaller voltage appears across the resonating capacitor and the lamps. However with 1 mH gapped inductance, there is sufficient inductor current to heat the filaments.

For lamp ignition, the frequency is reduced from 80 kHz to 40 kHz at 30 kHz/sec towards resonance causing the lamp voltage to rise to about 340V peak. Ignition occurs at about 40 kHz for a 18W T8 lamp. The plasma established in the lamp presents a resistive load across the resonating capacitor thereby reducing the voltage across the capacitor and shifting the reactive power in the bridge circuit to resistive power in the lamp.

A further reduction in frequency to 32 kHz at 30 kHz/sec establishes maximum brightness as the resonant circuit now has a leading (capacitive) power factor causing more voltage and current (approx. 360 Vpeak) across the capacitor and the lamp.

Dimming is accomplished by raising the drive frequency towards 100 kHz. The lower lamp (capacitor) voltage caused by changing from a leading to a lagging (inductive) power factor and the resulting drop in lamp current causes lamp dimming. The visual perception of brightness is logarithmic with applied power and must be taken into account in the control method scheme.

4.5.1 Single Lamp Operation

Single lamp operation can be detected from the 380VDC bus current through a 1 ohm sense resistor sensed by the differential input PB3/PB4. The AT90PWMx differential amplifier has the gain preset in the source code at 10. This scales the 200mV for two lamps to a reasonable A/D resolution. PB4 requires low pass filtering. Through the 1 ohm sense resistor R28, V = I*R = 80 Watts*1/380V = 210mA*1 = 210mV. At preheat, the current for one lamp is half that for two lamps. This current is also used to sense open filament condition or lamp removed under power condition. An abrupt change in the bus current is a good indicator of lamp condition that does not require a high frequency response or a minimal response due to reactive currents.

Once single lamp condition is detected, the minimum run frequency is determined by lamp current PB4 < 100mV. If the single lamp condition occurs while running, as noted by a decrease in current of more than 20% from the preset level, increase the frequency until the PB4 = 90mV. If the PB4 increases to 120mV, assume the lamp has been replaced. Increase the frequency to 80 kHz to restart the ignition process. This is necessary to preheat the new lamp filament to ensure that the hot lamp will not ignite any sooner than the cold lamp, exceeding the balance transformer range. Start the ignition sequence. With one cold lamp in parallel with one hot lamp, it may be necessary to restart several times to get both lamps to ignite.

Note that the lamp and resonant circuit use a common return ground separate from the rest of the circuit. The ballast demonstrator uses active power feedback of the sense voltage vs. drive frequency to meet power objectives. Also note that the differential amplifier is connected across the current sense resistor R28 to ensure a Kelvin connection. Layout of the amplifier + and – is critical for fast noise free loop response.

4.5.2 Lamp Sequential Step Description

After PB2 (boost voltage at 380V) = > 2.380V start preheat

Enable PD6 rectified lamp voltage sense

Enable PB0 and PB1 half bridge drive output

PB0 & PB1 12.5µS total period (80 kHz) 50% duty 180° out of phase.

Check PB4 > 20mV, then 2 lamps. If PB4 < 20mV assume a single lamp.

If PB4 < 10mV assume an empty fixture = fault & shutdown.

Determine the lamp intensity control method DALI (presence of data stream at PD4), Swiss (presence of 50/60 Hz modulated 0 – 10V at PB6) or 0 - 10V (constant non-zero voltage) at PB6.

4.5.3 Start and Ignition Sequential Step Description

Sweep PB0 and PB1 frequency down at 30 kHz/sec or 33µS/sec rate.

Stop sweep at 40 kHz or 25µS period (12.5µS pulses for each half bridge FET)

Check PB4 > 100mV (2 lamps) or > 30mV (1 lamp) for proof of ignition.

Hold ignition frequency for 10mS.

If no PD6 voltage, collapse to < 200mV for proof of ignition, increase frequency to 77 kHz for preheat for 1 second.

Repeat ignition sequence 6 times then if fails, set DALI fail flag or shut down.

Disable if dimmed frequency > 60 kHz. Disable if single lamp.

Proceed to power setting command at 30 kHz/sec rate as established by external control or if no internal control proceed to PB4 195mV at input terminals before gain (about 32 kHz) for 100% power.

If Swiss control, proceed to max power. The Swiss continuous switch closure will cause progressive increase in frequency at 33 kHz per second. The exception for a single lamp will be minimum frequency for 97mV (39 watts) at PB4 for 100% brightness. This is the default power for a single lamp with no dimming.

4.5.4 Power Control Description

Calculate input power for both lamps = PB4 (lamp current) * 380. Use this data for DALI feedback verification if required. Set programmable gain of AMP0 to 10. 78 watts will be 0.195 VDC at the input of AMP0+ or 1.95V internal A/D input.

Adjust frequency up (lower power) or down (higher power) at 30KHz/sec rate. Limit frequency to 100% (PB4 = 0.195V and 32KHz) to 80KHz dimming range. The dimming must be logarithmic for the best resolution. The largest lumen change will be at the lowest power setting. A small high frequency change 70 to 80kHz will give a large perceived dimmed range.

If PB4 > 0.220V for two lamps or > 0.110V for one lamp, set half bridge drive off due to over current. Start re-ignition sequence. Repeat 6 times and if still out of spec, set TX DALI fail signal & shutdown PFC and half bridge drive.

Section 5

Device Design & Application

5.1 Magnetics

PFC – Power Factor Correction

Without going into the derivations of the formulas used, the inductor design is as follows:

$$L = \frac{1.4 * 90VAC * 25\mu S}{4.5A\ peak} = 700\mu H$$

The ON time has been discussed earlier and the OFF time maximum will occur at high line condition at the peak of the haversine. A 16mm core was chosen for the recommended power density at 200mT and 50 kHz.

5.2 IXYS IXTP02N50D DEPLETION MODE MOSFET USED AS CURRENT SOURCE

The IXYS IXTP02N50D depletion mode MOSFET is used in this circuit to provide power and a start-up voltage to the Vcc pin of the IXI859 charge pump regulator. The IXTP02N50D acts as a current source and self regulates as the source voltage rises above the 15V zener voltage and causes the gate to become more negative than the source due to the voltage drop across the source resistor. Enough energy is available from the current source circuit during the conduction angles to keep the IXI859 (U1) pin 1 greater than 14VDC as required to enable the Under Voltage Lock Out (UVLO) circuitry in the IXI859.

5.3 IXYS IXD611 Half- bridge MOSFET driver

The IXD611 half bridge driver includes two independent high speed drivers capable of 600mA drive current at a supply voltage of 15V. The isolated high side driver can withstand up to 650V on its output while maintaining its supply voltage through a bootstrap diode configuration. In this ballast application, the IXD611 is used in a half bridge inverter circuit driving two IXYS IXTP3N50P power MOSFETs. The inverter load consists of a series resonant inductor and capacitor to power the lamps. Filament power is also provided by the load circuit and is wound on the same core as the resonant inductor. Pulse width modulation (PWM) is not used in this application, instead the power is varied and the dimming of the lamps is controlled through frequency variation. It is important to note that pulse overlap, which could lead to the destruction of the two MOSFETs due to current shoot through, is prevented via the input drive signals through the microcontroller.

Other features of the IXD611 driver include:

Wide supply voltage operation 10-35V
Matched propagation delay for both drivers
Undervoltage lockout protection
Latch up protected over entire operating range
+/- 50V/ns dV/dt immunity

5.4 IXYS IXI859 Charge Pump Regulator

The IXI859 charge pump regulator integrates three primary functions central to the PFC stage of the ballast demonstrator. First it includes a linear regulated supply voltage output, and in this application the linear regulator provides 3.3V to run the microcontroller. The second function is a gate drive buffer that switches an external power MOSFET used to boost the PFC voltage to 380V. Once the microcontroller is booted up and running, it generates the input signal to drive the PFC MOSFET through the IXI859 gate drive buffer. Finally, the third function provides two point regulated supply voltage for operating external devices. As a safety feature, the IXI859 includes an internal Vcc clamp to prevent damage to itself due to over-voltage conditions.

In general applications at start-up, an R-C combination is employed at the Vcc supply pin that ramps up a trickle voltage to the Vcc pin from a high voltage offline source. The value of R is large to protect the internal zener diode clamp and as a result, cannot supply enough current to power the microcontroller on it's own. C provides energy to boot the microcontroller. At a certain voltage level during the ramp up, the Under Voltage Lock Out point is reached and the IXI859 enables itself. The internal voltage regulator that supplies the microcontroller is also activated during this time. However, given the trickle charge nature of the Vcc input voltage, the microcontroller must boot itself up and enable PFC operation to provide charge pump power to itself. This means that the R-C combination must be sized carefully so that the voltage present at the Vcc pin does not collapse too quickly under load and causes the UVLO circuitry to disable device operation before the microcontroller can take over the charge pump operation. Also note that there is an internal comparator that only releases charge pump operation when the Vcc voltage drop below 12.85V. The charge pump is released and Vcc voltage is pumped up to 13.15V at which time the internal comparator disables the charge pump. This results in a tightly regulated charge pump voltage.

One problem with the R-C combination described above is that when a universal range is used at the Vcc pin, 90-265VAC, R must dissipate nine times the power, current squared function for power in R, over a three-fold increase of voltage from 90V at the low end to 265V on the high end. As an alternative and as used in the ballast demonstrator, the Vcc pin is fed voltage by way of a constant current source as previously described in Section 5.2. This circuit brings several advantages over the regular R-C usage. First we can reduce power consumed previously by R and replace it with a circuit that can provide power at startup. It can also provide sufficient power to run the microcontroller unlike the R-C combination. This would be an advantage in the case that a standby mode is desired. Overall power consumption can be reduced by allowing the microcontroller to enter a low power mode and shut down PFC operation without having to reboot the microcontroller. Since the R-C combination cannot provide enough power to sustain microcontroller operation, the microcontroller must stay active running the PFC section to power itself.

5.5 IXYS IXTP3N50P PolarHV™ N-Channel Power MOSFET

The IXTP3N50P is a 3A 500V general purpose power MOSFET that comes from the family of IXYS PolarHV MOSFETs. When comparing equivalent die sizes, PolarHT results in 50% lower RDS(ON), 40% lower RTHJC (thermal resistance, junction to case), and 30% lower Qg (gate charge) enabling a 30% - 40% die shrink, with the same or better performance verses the 1st generation power MOSFETs.

Within the ballast demonstrator itself the IXTP3N50 serves two functions. The first of which is the power switching pair of devices in the half-bridge circuit that drives the lamps. While a third device serves in the main PFC circuit as the power switch that drives the PFC inductor.

5.6 Clare LDA111S Optocoupler

Clare's family of single and dual optocoupler provide an optically isolated means of switching control circuits. The LDA111S contains one phototransistor that is optically coupled to an LED. Shunt resistors can be used to adjust the threshold currents required to activate the output circuitry. While both AC and DC input versions are available, the LDA111S is a DC input only model and features a 100mA continuous load rating, $3750V_{RMS}$ input to output isolation, and a 1000% current transfer ratio.

The LDA111S serves duty to isolate control signals within the ballast design.

Section 6

ATPWMX Demonstrator Software

This section of the application note describes the software architecture utilizing the following source code files and related state machines:

- Main_pwmx_fluo_demo.c

  ADC State Machine

  COMMAND CONTROL State Machine

- Pfc_ctrl.c

  PFC State Machine

- Lamp_ctrl.c

  Lamp State Machine

Associated header files:

- Main_pwmx_fluo_demo.h
- Pfc_ctrl.h
- Lamp_ctrl.h

The software uses the following peripherals:

- TIMER0, ADC, amplifier, Comparator0, PSC0, PSC2, PLL, DALI via EUSART

The application has been designed to work either with the AT90PWM3 or 2.

In order for the ballast to operate, three primary control systems should run simultaneously. One for the PFC control, one for the Lamp control, and one for the Command control of the ballast.

Furthermore, in order to work properly the state machines require input data. The analog data is provided primarily by an auto running interrupt mode ADC state machine.

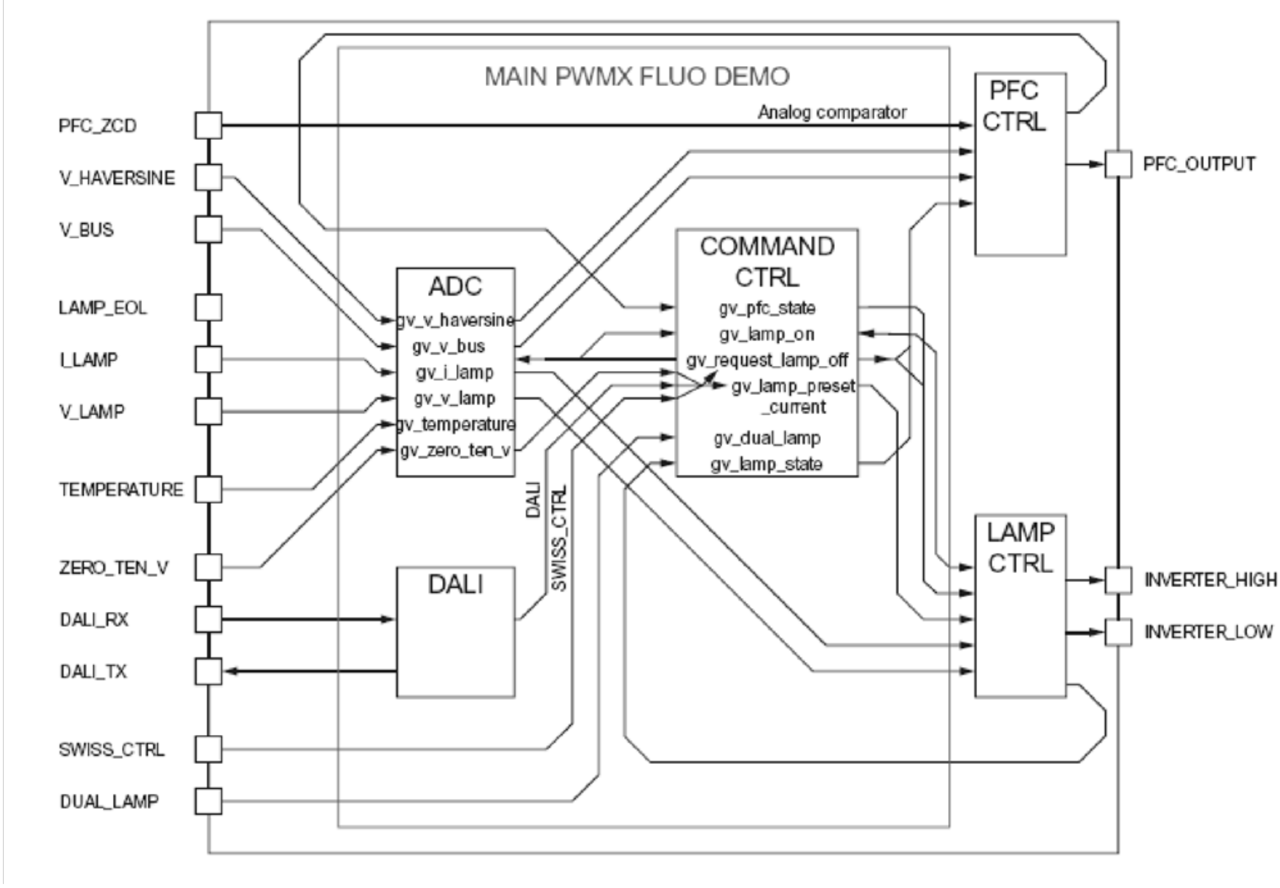
The complete software package for the application is split into the functional blocks in the diagram shown below. While the variables are identified as follows.

g_	global
gv_	global volatile
gs_	global static

Voltage and current variables are identified by the following examples.

g_v or g_i	global - voltage/current
gv_v or gv_i	global volatile - voltage/current
gs_v or gs_i	global static - voltage/current

Figure 6-1. Demo Software Architecture



6.1 Main_pwmx_fluo_demo.c

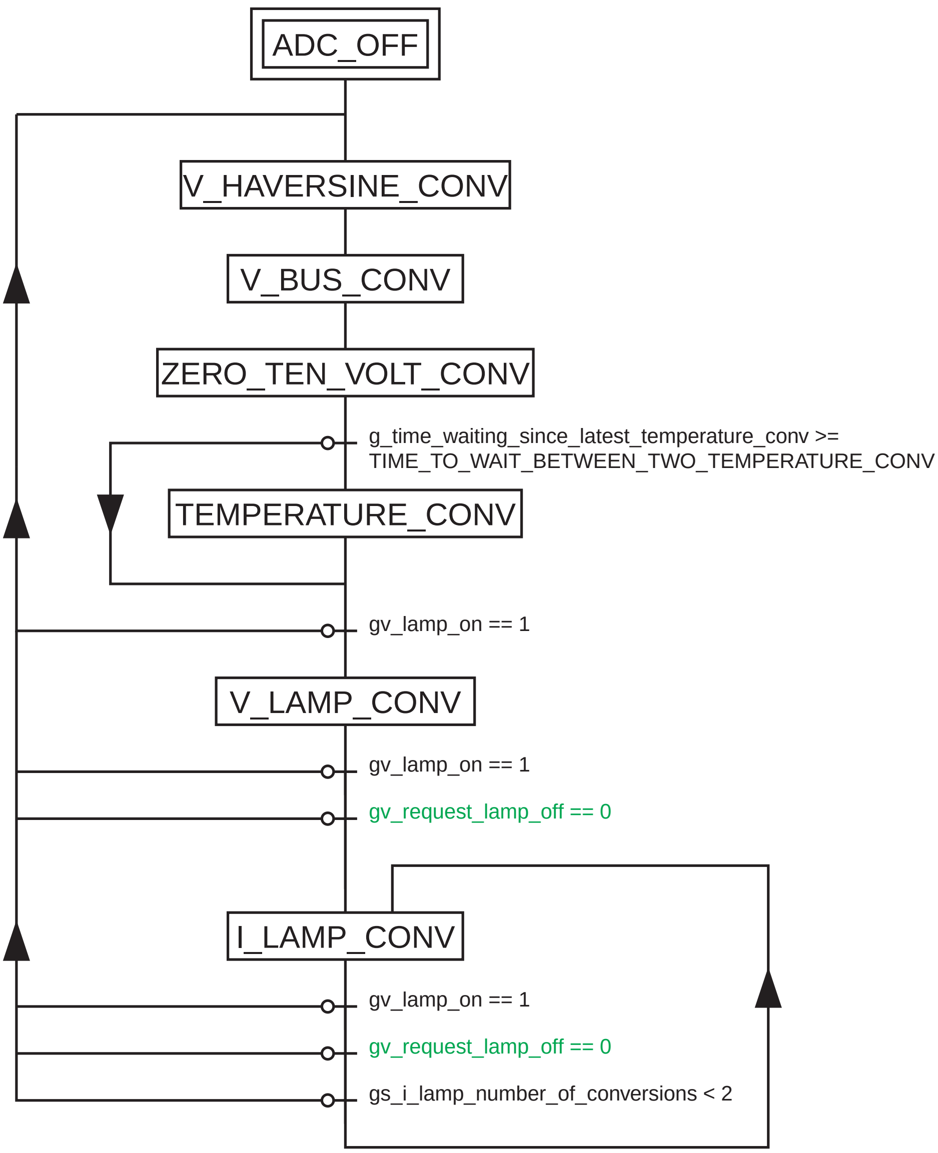
This file executes all the peripheral initialization and then schedules the different control tasks.

The ADC and the Command control state machines are also included in this file. The ADC machine is controlled via interrupts.

6.1.1 ADC STATE MACHINE

The ADC state machine functional diagram is shown below:

Figure 6-2. ADC State Machine



The different states are outlined below:

ADC_OFF

The ADC was previously off. This is the *first* conversion and is not necessarily valid.

Start the first V_HAVERSINE_CONV conversion.

V_HAVERSINE_CONV

Get back the v_haversine result.

Start the next V_BUS_CONV conversion.

V_BUS_CONV

Get back the v_bus result.

Start the next ZERO_TEN_VOLT_CONV conversion.

ZERO_TEN_VOLT_CONV

Get back the zero_ten_volt_result and make a slipper filter with 512 conversion results.

Start the V_HAVERSINE_CONV, the TEMPERATURE_CONV, or the V_LAMP_CONV conversion depending on g_time_waiting_since_latest_temperature_conv and gv_lamp_on.

TEMPERATURE_CONV

Get back the temperature_result.

Start the V_HAVERSINE_CONV or the V_LAMP_CONV conversion depending on gv_lamp_on.

V_LAMP_CONV

Get back the v_lamp result.

Start the v_haversine or the i_lamp conversion depending on gv_lamp_on and gv_request_lamp_off.

If a lamp off (gv_request_lamp_off == 1) has been requested by the command control task or a lamp fault mode on Lamp_ctrl.c file, the PSC2 and the amplifier0 are switched off and the following variables are set in at the following values:

- gv_lamp_on = 0;
- gv_lamp_state = LAMP_OFF;
- gv_pfc_state = SHUT_DOWN_PFC_AND_SLOW_DOWN_UC_SPEED;

Then a V_HAVERSINE_CONV conversion is started.

Else an I_LAMP_CONV conversion is started.

I_LAMP_CONV

Get back the i_lamp result and depending on gv_lamp_on and gv_request_lamp_off, start another I_LAMP_CONV conversion in order to increase the accuracy and resolution of the i_lamp measurement then start another cycle beginning with a V_HAVERSINE_CONV conversion.

If a lamp off (gv_request_lamp_off == 1) has been requested by the command control task or a lamp fault mode on Lamp_ctrl.c file, the PSC2 and the amplifier0 are switched off and the following variables are set at the following values:

- gv_lamp_on = 0;
- gv_lamp_state = LAMP_OFF;
- gv_pfc_state = SHUT_DOWN_PFC_AND_SLOW_DOWN_UC_SPEED;

Then a V_HAVERSINE CONV conversion is started.

6.1.2 ADC State Machine Global Variables

6.1.2.1 Input variables which have an impact on ADC state machine

- g_v_lamp_on is normally set only by the CONFIGURE_LAMP_PREHEAT state of the Lamp state machine in the Lamp_ctrl.c file.
- gv_request_lamp_off can be set by the command control state machine in the case the user requests to switch the lamp off.

6.1.2.2 Output variables which can impact the other state machines

- g_v_lamp_on which can be cleared during the V_LAMP_CONV or I_LAMP_CONV state in case the gv_request_lamp_off has been set by the command control state machine.
- gv_lamp_state within the Lamp state machine in the Lamp_ctrl.c file can be set to LAMP_OFF during the V_LAMP_CONV or I_LAMP_CONV state.
- gv_pfc_state within the PFC state machine in the Pfc_ctrl.c file can be set to SHUT_DOWN_PFC_AND_SLOW_DOWN_UC_SPEED state during the V_LAMP_CONV or I_LAMP_CONV state.

6.1.3 Miscellaneous

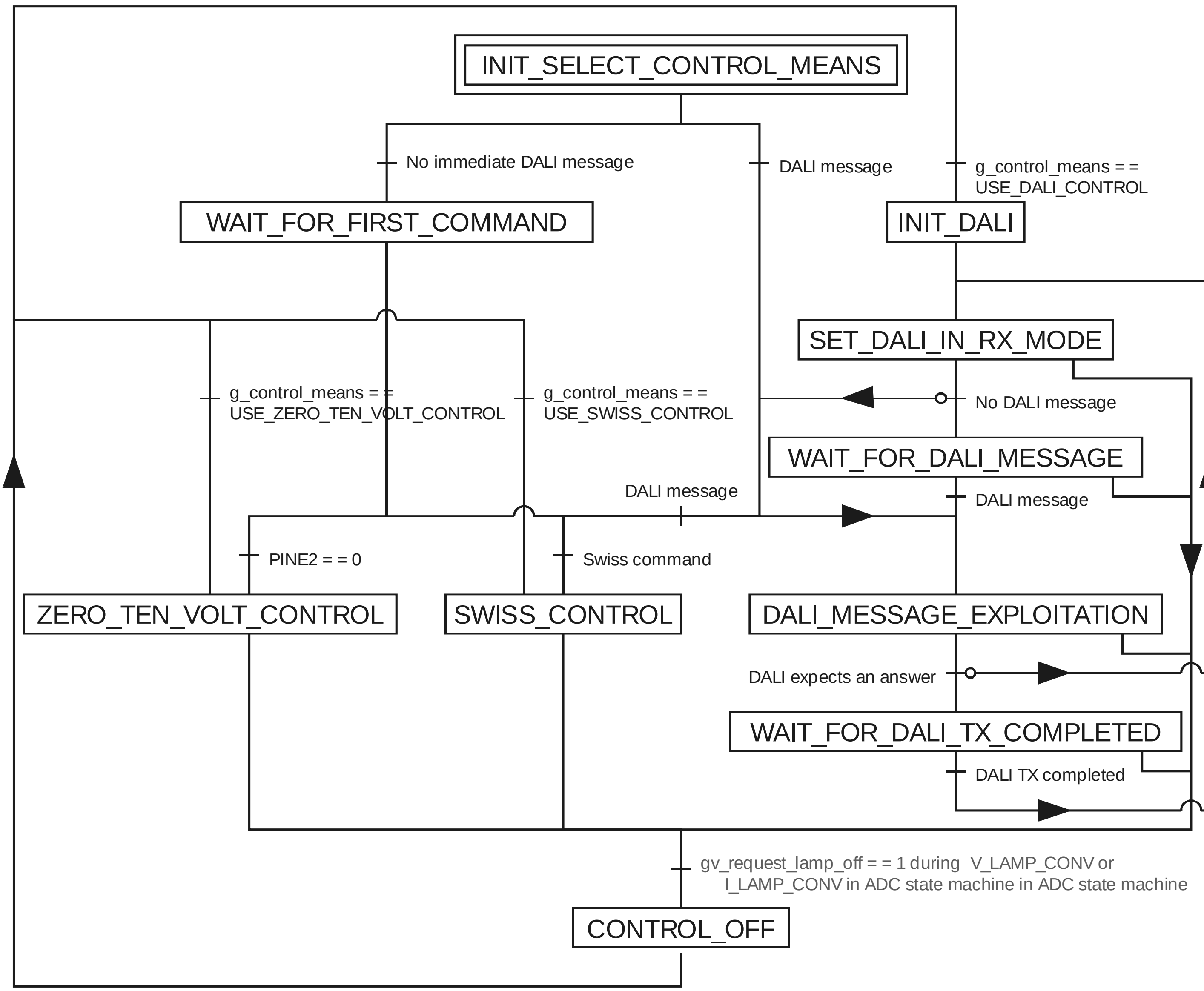
The gv_lamp_on checks during V_LAMP_CONV and I_LAMP_CONV states are normally useless because gv_lamp_on is reset only by the same states of the ADC state machine.

6.1.4 COMMAND CONTROL STATE MACHINE

The Command Control state machine centralizes the 0-10V, SWISS, and DALI controls in order to switch PFC operation On or Off and to set the lamp control instructions given by the user.

The Command Control state machine functional diagram is shown below:

Figure 6-3. Control State Machine



The different states are outlined below:

INIT_SELECT_CONTROL_MEANS

The DALI bus is initialized in order to be able to receive a DALI message in case this bus is used as the control means for the ballast. In case a DALI message arrives at once**,** g_control_means is set to USE_DALI_CONTROL, and the gv_control_state is set to DALI_MESSAGE_EXPLOITATION, otherwise gv_control_state is set to WAIT_FOR_FIRST_COMMAND.

WAIT_FOR_FIRST_COMMAND

The three control means are scrutinized, and the first command caught sets the g_control_means variable according to the command received. Then the command is applied to the corresponding command state machine.

ZERO_TEN_VOLT_CONTROL

Analog control with 0-10V laboratory supply. PINE2 allows the lamp to be switched on and off.

SWISS_CONTROL

Read the input pin.

Analyze the touch dim command.

Set the control variable values corresponding to the user request.

INIT_DALI

Initialize the DALI microcontroller peripheral and jump to SET_DALI_IN_RX_MODE.

SET_DALI_IN_RX_MODE

Set the DALI bus in RX mode and jump to the WAIT_FOR_DALI_MESSAGE state or to the DALI_MESSAGE_EXPLOITATION state in case a message had been received as soon as the DALI was ready.

WAIT_FOR_DALI_MESSAGE

Wait for a DALI message, in the case one arrives, jump to the DALI_MESSAGE_EXPLOITATION state.

DALI_MESSAGE_EXPLOITATION

Analyze the DALI message content and modify control variables according to the request. In case a request from the DALI master is expected, answer, and jump back to SET_DALI_IN_RX_MODE state in order to wait for the next command, or jump to the WAIT_FOR_DALI_TX_COMPLETED state in case the TX is not completed.

WAIT_FOR_DALI_TX_COMPLETED

Stay in this state until the DALI transmission is completed. As soon as the transmission is done, jump to SET_DALI_IN_RX_MODE in order to reinitialize the DALI bus for the next message.

6.1.5 Control state machine Global variables

6.1.5.1 Input variables which have an impact on the Control state machine:

- None

6.1.5.2 Output variables which can impact other state machines

- gv_pfc_state is set from PFC_OFF state to INIT_PFC_HAVERSINE_CHECK state on the PFC state machine in the Pfc_ctrl.c file when the user requests the lamp to switch on.
- gv_request_lamp_off is set by the control state machine.

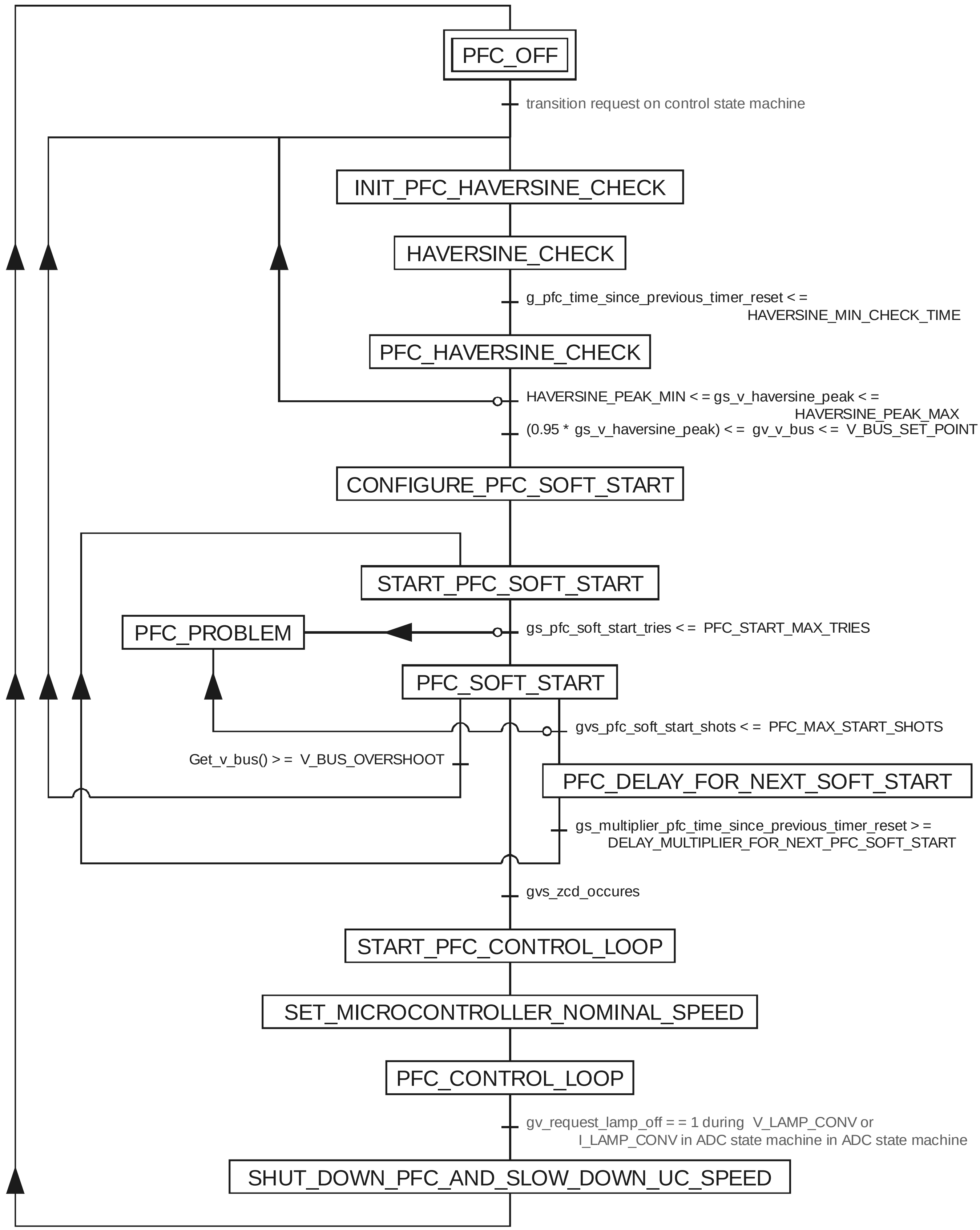
6.2 Pfc_ctrl.c

This file executes the PFC state machine according to the scheduler in the Main_pwmx_fluo_demo.c file.

6.2.1 PFC STATE MACHINE

The PFC state machine functional diagram is shown in Figure 6-4.

Figure 6-4. PFC State Machine



The different states are outlined below:

PFC_OFF

Nothing happen, the exit from this state is requested by the Command Control state machine in the Main_pwmx_fluo_demo.c file.

INIT_PFC_HAVERSINE_CHECK

Initialize the control values of the PFC.

Then jump to the HAVERSINE_CHECK state.

HAVERSINE_CHECK

Measure the haversine peak voltage during HAVERSINE_MIN_CHECK_TIME.

Then jump to the PFC_HAVERSINE_CHECK state.

PFC_HAVERSINE_CHECK

PFC haversine peak must be between HAVERSINE_PEAK_MIN and HAVERSINE_PEAK_MAX (90VAC and 265VAC).

If the haversine value is OK, set the max pulse width allowed and jump to the CONFIGURE_PFC_SOFT_START state.

Else go back to INIT_PFC_HAVERSINE_CHECK state.

CONFIGURE_PFC_SOFT_START

Configures the peripherals PSC0 and comparator0 to soft start the PFC.

Then jump to START_PFC_SOFT_START.

START_PFC_SOFT_START

Check that the soft start has been tried less than PFC_START_MAX_TRIES

If OK then start PSC0 and jump to PFC_SOFT_START state.

Else immediately jump to the PFC_PROBLEM state.

PFC_SOFT_START

The PFC soft start consists of PFC_MAX_START_SHOTS pulses configured by PFC_SOFT_START_CONFIGURATION.

If a zero crossing detection appears, jump to the START_PFC_CONTROL_LOOP state

Else go to INIT_PFC_HAVERSINE_CHECK, PFC_DELAY_FOR_NEXT_PFC_SOFT_START, or PFC_PROBLEM state depending on the different conditions detailed in the PFC diagram.

PFC_DELAY_FOR_NEXT_PFC_SOFT_START

In case the soft start fails, the software has to wait DELAY_FOR_NEXT_PFC_SOFT_START*DELAY_MULTIPLIER_FOR_NEXT_PFC_SOFT_START, before trying a new soft start by going back to the START_PFC_SOFT_START state.

START_PFC_CONTROL_LOOP

A zero crossing detection occurs so the PFC is now started, and the PFC can be configured to autoretrigg mode.

The power will then be sufficient to set the microcontroller at its nominal speed on the next SET_MICROCONTROLLER_NOMINAL_SPEED state.

SET_MICROCONTROLLER_NOMINAL_SPEED

The PFC is now running, so the microcontroller can now run at its full speed and the lamp can be switched on.

Then the gv_pfc_state is set to PFC_CONTROL_LOOP. This directly impacts the lamp state machine which goes from a LAMP_OFF state to a CONFIGURE_LAMP_PREHEAT state.

PFC_CONTROL_LOOP

PFC is now running... This is the normal PFC loop control.

In the case g_v_request_lamp_off is equal to 1 during a V_LAMP or an I_LAMP state of the ADC state machine, the PFC will be shut down and the microcontrollers speed will be decreased in order to reduce power consumption in the new SHUT_DOWN_PFC_AND_SLOW_DOWN_UC_SPEED state.

SHUT_DOWN_PFC_AND_SLOW_DOWN_UC_SPEED

Switch off the PFC.

Switch the microcontroller to a low power consumption mode.

Then go back to PFC_OFF state.

6.2.2 PFC State Machine Global variables

6.2.2.1 Input variables which have an impact on PFC state machine:

- gv_pfc_state is set from PFC_OFF state to INIT_PFC_HAVERSINE_CHECK state on the Control state machine in Main_pwmx_fluo_demo.c file when the user requests to switch the lamp on.
- gv_pfc_state is also set from PFC_CONTROL_LOOP state to SHUT_DOWN_PFC_AND_SLOW_DOWN_UC_SPEED state on the Control state machine in Main_pwmx_fluo_demo.c file when the user requests to switch the lamp off.

6.2.2.2 Output variables which can impact other state machines:

- gv_lamp_state is set from the LAMP_OFF state to the CONFIGURE_LAMP_PREHEAT state when the PFC is ready on the PFC_CONTROL_LOOP state.

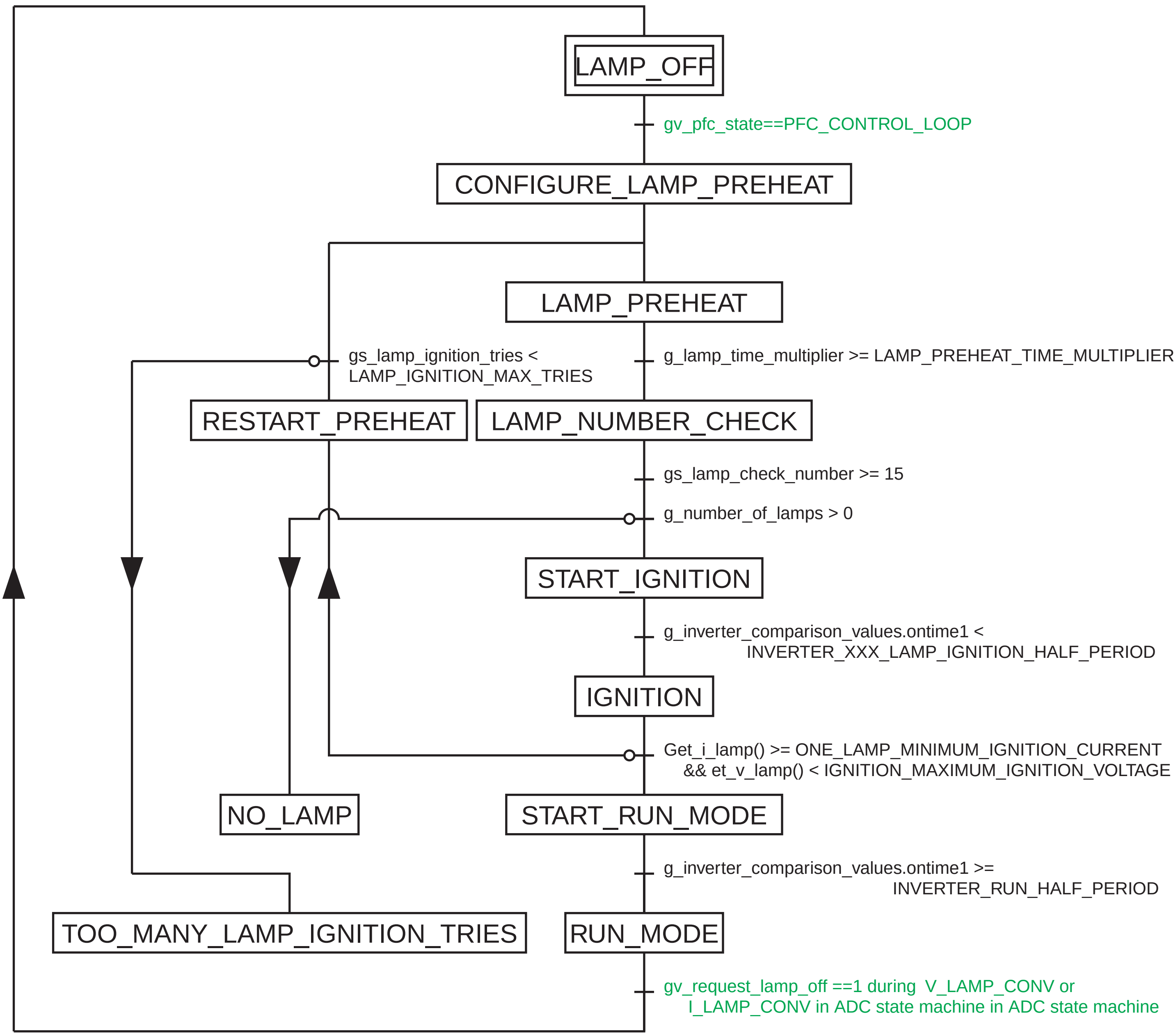
6.3 Lamp_ctrl.c

This file executes the Lamp state machine according to the scheduler in the Main_pwmx _fluo_demo.c file.

6.3.1 Lamp State Machine

The different states are outlined below:

Figure 6-5. Lamp State Machine



LAMP_OFF

Nothing happens, the exiting of this state takes place as soon as the gv_pfc_state is set to PFC_CONTROL_LOOP.

CONFIGURE_LAMP_PREHEAT

This is the first time the lamp is attempted to be started once the user has requested to switch it on.

Configure the amplifier0, which is used to measure the current, then configure the PSC2 according to the definitions in the config.h file, and initialize all the lamp control variables.

Then jump to the LAMP_PREHEAT state.

LAMP_PREHEAT

Starts the preheat sequence for LAMP_PREHEAT_TIME.

Then jump to the LAMP_NUMBER_CHECK state.

LAMP_NUMBER_CHECK

Check the preheat current in order to know whether there is one or two lamps

Then jump to the START_IGNITION state.

In the case there is no lamp, jump to the NO_LAMP state.

START_IGNITION

Decrease the frequency from the init frequency down to INVERTER_IGNITION_HALF_PERIOD.

Then jump to the IGNITION state.

IGNITION

The ignition sequence consists of maintaining the ignition frequency determined by INVERTER_IGNITION_HALF_PERIOD for 10ms, and then checking if ignition occurs by measuring lamp current and voltage.

In case it is... START_RUN_MODE.

In case it isn't... RESTART_PREHEAT.

RESTART_PREHEAT

Reconfigure the Inverter with the Restart parameters, then go to LAMP_PREHEAT.

If Ignition fails too many times... Go to TOO_MANY_LAMP_IGNITION_TRIES.

START_RUN_MODE

Increase the frequency from the init frequency, INVERTER_IGNITION_HALF_PERIOD.

Then jump to the RUN_MODE state.

RUN_MODE

Normal control loop to have the light in accordance with the gv_lamp_preset_current variable that is permanently updated in the command control state machine in the Main_pwmx_fluo_demo.c file.

The transition from the RUN_MODE state to the LAMP_OFF state is done in the ADC state machine during the V_LAMP_CONV or I_LAMP_CONV state in the case the gv_request_lamp_off has been set by the command control task in the Main_pwmx_fluo_demo.c file.

TOO_MANY_LAMP_IGNITION_TRIES

If the ignition has failed LAMP_IGNITION_MAX_TRIES, a lamp switch off is requested by setting the gv_request_lamp_off and the LAMP_OFF state takes effect during the next I_LAMP_CONV or the V_LAMP_CONV state of the ADC state machine in the Main_pwmx_fluo_demo.c file.

NO_LAMP

If no lamp is detected during the LAMP_NUMBER_CHECK, a lamp off is requested by setting the gv_request_lamp_off and the effective return to the LAMP_OFF state takes place during the next I_LAMP_CONV or the V_LAMP_CONV state of the ADC state machine in the Main_pwmx_fluo_demo.c file.

6.3.2 Lamp state machine Global variables

6.3.2.1 Input variables which have an impact on the Lamp state machine

- The transition from LAMP_OFF to PFC_CONTROL_LOOP is done when the gv_pfc_state is set to PFC_CONTROL_LOOP in Pfc_ctrl.c file.
- The transition from the RUN_MODE state to the LAMP_OFF state is done in the ADC machine during the V_LAMP_CONV or I_LAMP_CONV state in the case gv_request_lamp_off has been set by the command control task in the Main_pwmx_fluo_demo.c file.

6.3.2.2 Output variables which can impact other state machine

- A lamp off (gv_request_lamp_off == 1) can be set by the lamp fault mode. The effect of this request takes place in the I_LAMP_CONV or V_LAMP_CONV in the ADC state machine in the Main_pwmx_fluo_demo.c file.

Section 7

Conclusion

The ballast demonstrator shows that the AT90PWMx microcontroller can control and regulate fluorescent lamps from any of the three (DALI, 0 – 10VDC & SWISS) methods of dimming. It can automatically sense the control method used thereby providing lamp controller manufacturers with maximum flexibility in their design. One or more lamps can be controlled with flexibility and precision. Universal input and power factor control adds to the flexibility of the design with a minimal addition of more expensive active components.

Additionally, the programmability of the microcontroller offers the lamp manufacturer the flexibility to add more design features than are shown here to enhance their market position. The ballast demonstrator, with it's many features, does not address all the possibilities available to the lamp controller designer.

7.1 Appendix 1: SWISS DIM

The SwissDIM allows dimming control using a simple switch connected to the mains phase.

SwissDIM operation

The SwissDIM operation is as follows:

With the lamp switched on:

A short push switches the luminary off and stores the current light level.

A long push gradually dims the light level. (Change direction by briefly taking your finger off the button and pressing down again)

With the lamp switched off:

A short push switches the lamp on to the last light level used. (Optional: Use a soft start from minimum level to last level used)

A longer push starts on the last light level used and gradually raises the light level to the required brightness.

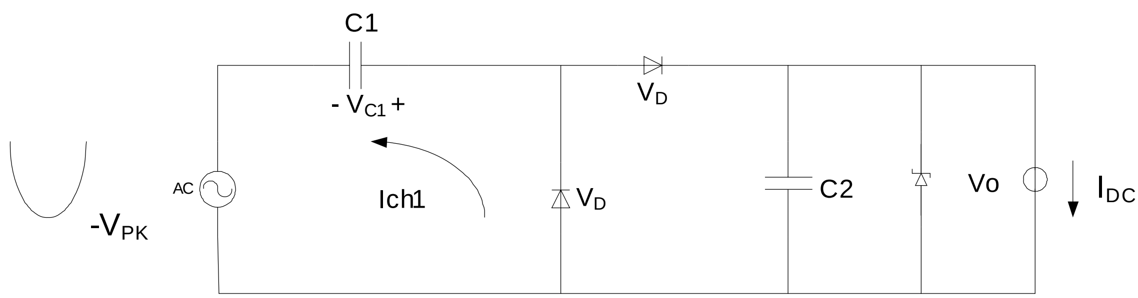
The lamps are dimmed for as long as the switch is pressed or until the minimum or maximum dimmer setting is reached.

7.2 Appendix 2: Capacitor Coupled Low Voltage Supply

Small currents for the low voltage supply can be obtained from the AC line at low loss by means of capacitor coupling as shown in the figures below. To estimate the required size of the coupling capacitor, use the following relationships for current, charge, voltage and capacitance.

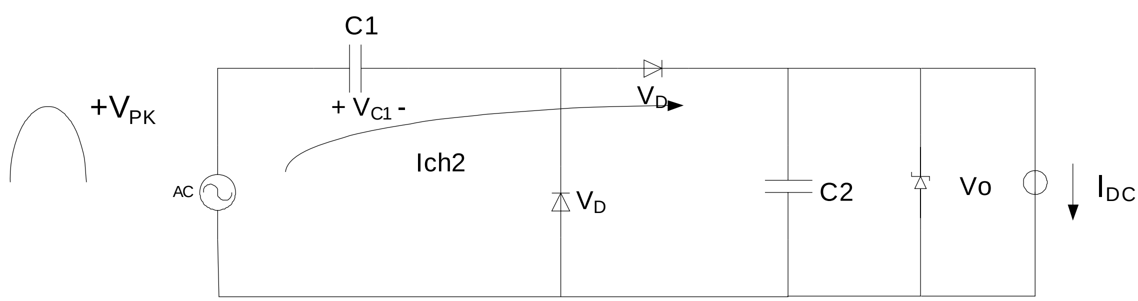
1. $dQ/dt = I_{DC}$

Figure 7-1. Negative Line Half Cycle



"Negative" line half-cycle:
C1 charges to Vpk - V_D with polarity shown.

Figure 7-2. Positive Line Half Cycle



"Positive" line half-cycle:
C1 charges to Vpk - V_D - Vo with polarity shown.

1. $dV = 2Vpk-Vo-2V_D$
2. $dQ = CdV$ or $C = dQ/dV$

For example, to obtain 15 ma at 20 VDC from a 220 Vrms 50 Hz line:

1. dQ/dt = (15 millijoules/sec)/(50 cycles/sec) or 0.3 millijoules / cycle.

2.Over 1 cycle, the coupling capacitor (C1) will charge from –220V x 1.4 to +220V x 1.4 – 20V- V_D. dV = 2*Vpk-Vo-2V_D.   dV ~= 600V.

3. The required C1 ~ 0.3 millijoules/600V or 0.5 uF

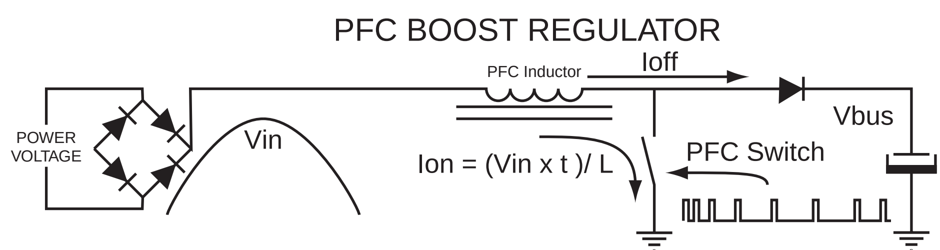
In practice, C1 may have to be larger depending on the amount of ripple allowed by C2 and to account for component tolerances, minimum voltage, and current in the regulator diode. C1 must be a non-polarized type with a voltage rating to withstand the peak line voltage including transients. A high quality film capacitor is recommended.

7.3 Appendix 3: PFC Basics

The function of the PFC boost regulator is to produce a regulated DC supply voltage from a full wave rectified AC line voltage while maintaining a unity power factor load. This means that the current drawn from the line must be sinusoidal and in phase with the line voltage.

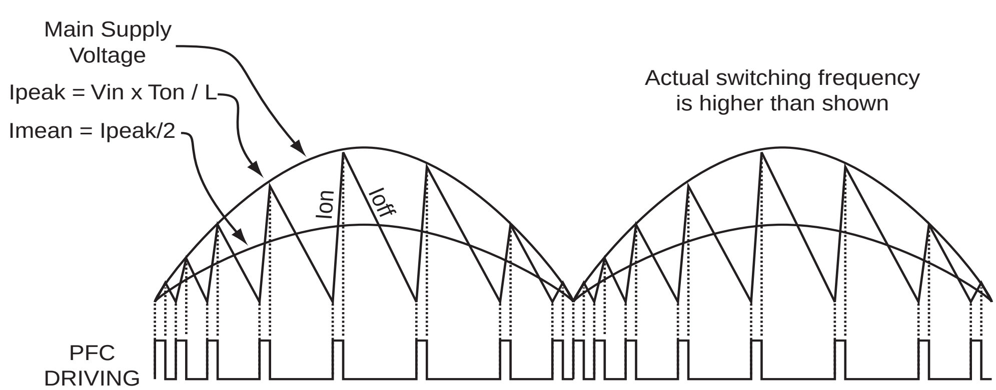
The ballast PFC circuit accomplishes this by means of a boost converter operating (See Figure 7-3) at critical conduction so that the current waveform is triangular (See Figure 7-4).

Figure 7-3. PFC Boost Regulator



The boost switch ON time is maintained constant over each half cycle of the input voltage sinusoid. Therefore the peak current for each switching cycle is proportional to the line voltage which is nearly constant during Ton. (Ipeak = Vin x Ton/L). Since the average value of a triangular waveform is half its peak value, the average current drawn is also proportional to the line voltage.

Figure 7-4. Main voltage supply cutting



7.4 Appendix 4: Bill Of Material

Figure 7-5. Bill of Materials 1

Item	Quantity	Reference	Part	Manufactures Part #	Distributors Part #	Distributor
1	1	BR1	600V	DF10S	DF10SDI-ND	DigiKey
2	1	BR2	0.5A 200V	RH02	RH02DICT-ND	DigiKey
3	2	C1,C3	1800 pF 250VAC	WYO182MCMBF0K	75-WYO182MCMBF0K	Mouser
4	2	C2,C28	1nF 50V	ECJ-2VB1H102K	PCC102BNCT-ND	Digikey
6	3	C4,C13,C14	.1uF 600V	MKP1840410634	75-MKP1840410634	Mouser
7	2	C5,C42	1 nF 250VAC	ECK-NVS102ME	P11418CT-ND	DigiKey
8	1	C6	47 uF	ECA-1JM470	P5192-ND	DigiKey
9	3	C7,C29,C41	10uF 25V	T491C106K025AS	399-1633-1-ND	
10	3	C8,C25,C35	1uF	GRM219F51E105ZA01D	490-1731-1-ND	
11	1	C9	47uF 455V	ECO-S2WP470BA	P7422-ND	DigiKey
12	2	C10,C46	.022 uF	ECJ-2VF1H223Z	PCC1860CT-ND	DigiKey
13	1	C11	.01uF 1500V FILM	MKP100.01/2000/5	505-M100.01/2000/5	Mouser
14	12	C12,C15,C23,C24,C26,C27, C30,C32,C33,C36,C40,C47	.1uF	GRM216F51E104ZA01D	490-1726-1-ND	
15	2	C16,C17	4.7 nF 630V	ECJ-3FB2J472K	PCC2294CT-ND	DigiKey
16	4	C18,C20,C21,C22	220nF 100V	ECJ-4YB2A224K	PCC2304CT-ND	DigiKey
17	1	C19	.001uF	GRM2165C1H102JA01D	490-1622-1-ND	
18	1	C31	100pF	ECJ-2VC1H101J	PCC101CGCT-ND	
19	2	C37,C48	.01uF	GRM216R71H103KA01D	490-1664-1-ND	
20	4	C38,C39,C43,C44	180 pF 1 KV	140-102S6-181J	140-102S6-181J	Mouser
21	5	D1,D4,D10,D15,D27	1A-600V/FR	MURS160-13	MURS160DICT-ND	DigiKey
22	1	D2	15V Zener	MMSZ5245B-7-F	MMSZ5245BDICT-ND	DigiKey
23	18	D3,D5,D7,D9,D11,D12,D14, D16,D17,D18,D19,D20,D21, D22,D24,D25,D26,D28	LL4148-13	LL4148-13	LL4148DICT-ND	DigiKey
24	3	D6,D8,D13	MBRS140CT	MBRS140TR	MBRS140CT-ND	DigiKey
25	1	D23	1n4740 10V Zener	MMSZ5240B-7	MMSZ5240BDICT-ND	DigiKey
26	3	J1,FL1,FL2	CONNECTOR	1935187	277-1579-ND	DigiKey
27	4	ISO1,ISO2,ISO3,ISO4	LDA111S	CLARE LDA111S		
28	4	JP2,JP3,J3,J4	JUMPER	929834-03-36	929834-03-36-nd	DigiKey
29	1	J2	HEADER6PIN	10-88-1121	WM6912-ND	
30	1	J5	CON4	640456-4	A1922-ND	DigiKey
31	1	L1	CM CHOKE	ELF-15N007A	PLK1069-ND	DigiKey
32	1	Q1	IXTP02N50D	IXYS XTP02N50D		
33	2	Q7,Q8	BC846BCT	BC847BLT1	BC847BLT1OSCT-ND	DigiKey
34	3	Q3,Q4,Q5	IXTP3N50P	IXYS IXTP3N50P		
35	3	Q6,Q9,Q10	BC857B	BC857BLT1	BC857BLT1OSCT-ND	DigiKey
36	1	RT1	10K @ 25C	01C1002JP	71-01C1002JP	Mouser

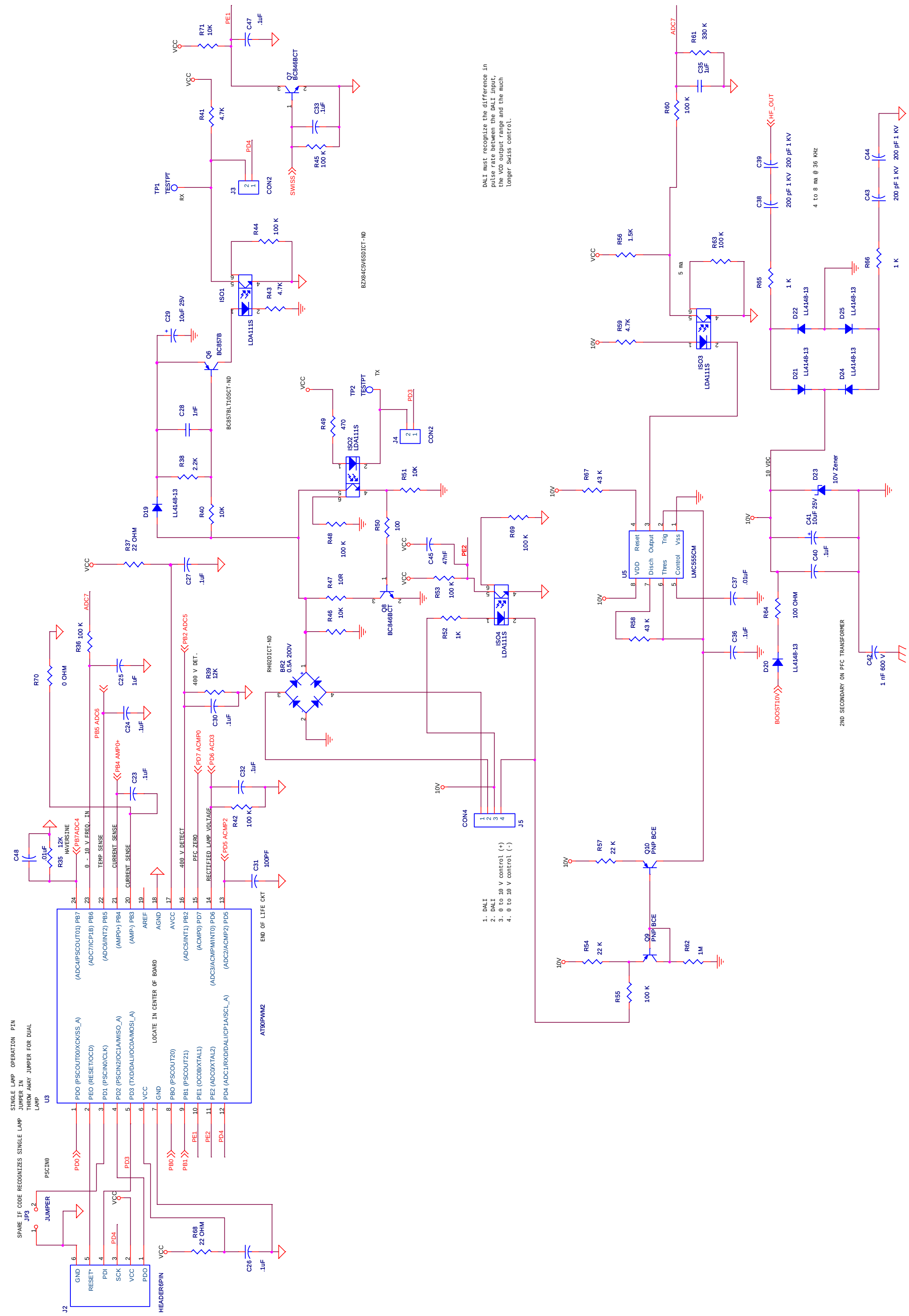
Figure 7-6. Bill of Materials 2

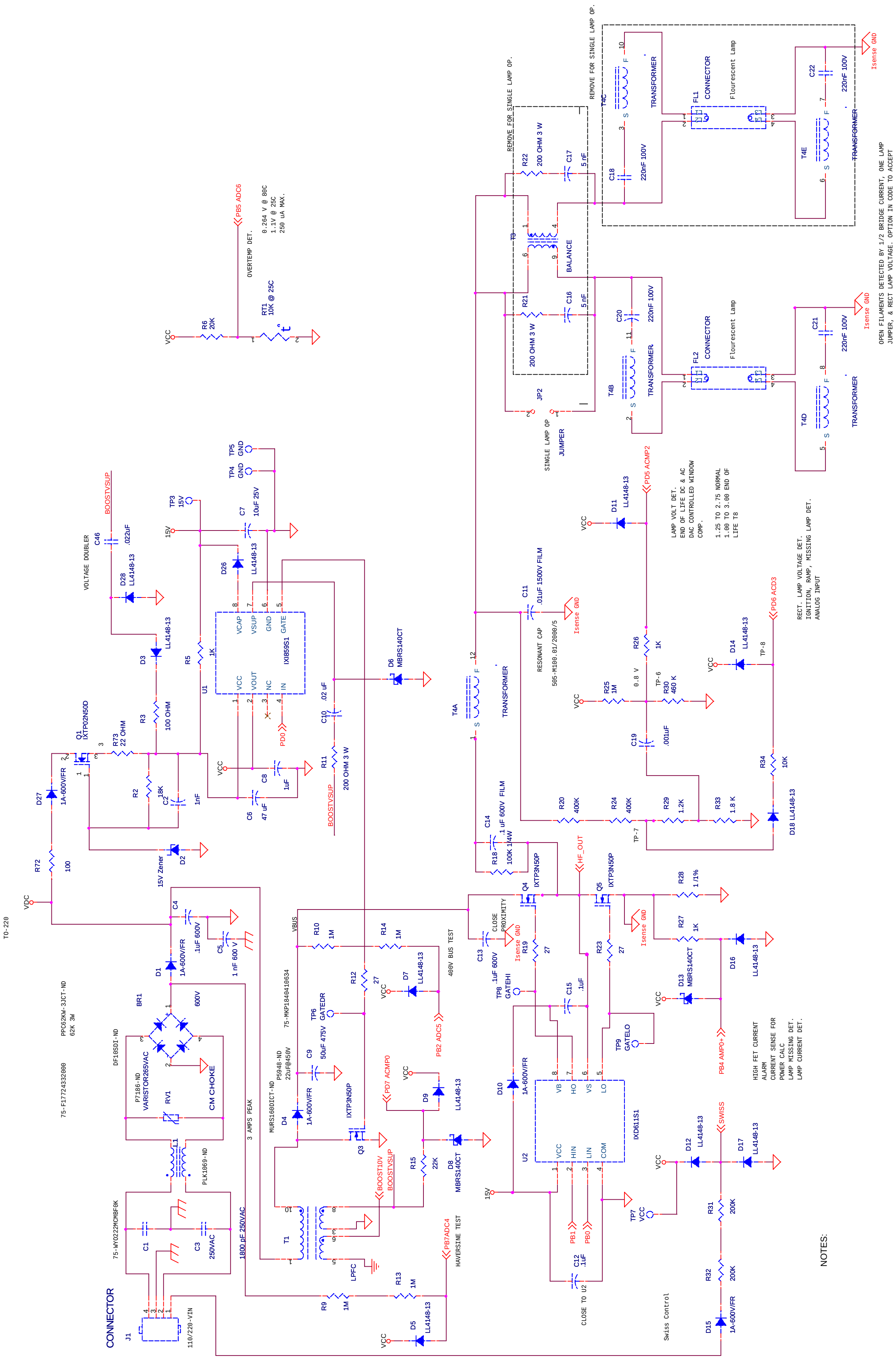
Item	Quantity	Reference	Part	Manufactures Part #	Distributors Part #	Distributor
37	1	RV1	VARISTOR265VAC	ERZ-V05D471	P7186-ND	DigiKey
38	6	R9,R10,R13,R14,R25,R62	1M			
39	1	R2	18K			
40	3	R3,R64,R50	100 OHM			
41	6	R5,R26,R27,R52,R65,R66	1K			
42	1	R6	20K			
43	2	R21,R22	200 OHM 3 W	ERG-3SJ201	P200W-3BK-ND	
44	3	R12,R19,R23	27OHM			
45	1	R15	22K			
46	1	R18	100K 1/4W			
47	2	R20,R24	402K			
48	1	R28	1 /1%			
49	1	R29	1.2K			
50	1	R30	464 K			
51	2	R31,R32	200K			
52	1	R33	1.8 K			
53	5	R34,R40,R46,R51,R71	10K			
54	2	R35,R39	12K			
55	10	R36,R42,R44,R45,R48 R53,R55,R60,R63,R69	100 K			
56	2	R37,R68	22 OHM			
57	1	R38	2.2K			
58	1	R47	10 OHM			
59	1	R56	1.5K			
60	2	R54,R57	22 K			
61	2	R58,R67	43 K			
62	3	R41,R43,R59	4.7K			
63	1	R61	330 K			
64	2	TP1,TP2	TESTPT	5001	5001K-ND	
65	1	TP3	15V	5001	5001K-ND	
66	2	TP4,TP5	GND	5001	5001K-ND	
67	1	TP6	GATEDR	5001	5001K-ND	
68	1	TP7	VCC	5001	5001K-ND	
69	1	TP8	GATEHI	5001	5001K-ND	
70	1	TP9	GATELO	5001	5001K-ND	
71	1	T1	LPFC XFORM	Pulse Eng. PA1438		
72	1	T3	BALANCE XFORM	Pulse Eng. PA1440		
73	1	T4	TRANSFORMER	Pulse Eng. PA1439		

Figure 7-7. Bill of Materials 3

Item	Quantity	Reference	Part	Manufactures Part#	Distributors Part#	Distributor
74	1	U1	IXI859S1	IXYS IXI859S1		
75	1	U2	IXD611S1	IXYS IIXD611S1		
76	1	U3	AT90PWM2	Atmel AT90PWM2		
77	1	U5	LMC555CM	LMC555CM	LMC555CM-ND	DigiKey
78	1	C45	47nF	GRM216E41H473MA01D	490-1747-1-ND	
79	1	R49	470 OHM			
80	1	R70	0 OHM			
81	1	Q1 Heat Sink (Optional)	Heat Sink	530614B00000	HS278-ND	
82	1	R11 (Optional)	200 OHM 3 W	ERG-3SJ201	P200W-3BK-ND	
83	2	SH3, SH4	Jumper	STC02SYAN	S9000-ND	DigiKey

7.5 Appendix 5: Schematics




CONNECTOR
CM CHOKE
VOLTAGE DOUBLER
OVERTEMP DET.
0.264 V @ 80C
1.1V @ 25C
250 uA MAX.
TRANSFORMER
BALANCE
REMOVE FOR SINGLE LAMP OP.
SINGLE LAMP OP
JUMPER
Flourescent Lamp
RESONANT CAP
LAMP VOLT DET.
END OF LIFE DC & AC
DAC CONTROLLED WINDOW
COMP.
1.25 TO 2.75 NORMAL
1.00 TO 3.00 END OF
LIFE T8
RECT. LAMP VOLTAGE DET.
IGNITION, RAMP, MISSING LAMP DET.
ANALOG INPUT
HIGH FET CURRENT
ALARM
CURRENT SENSE FOR
POWER CALC
LAMP MISSING DET.
LAMP CURRENT DET.
OPEN FILAMENTS DETECTED BY 1/2 BRIDGE CURRENT, ONE LAMP
JUMPER, & RECT LAMP VOLTAGE. OPTION IN CODE TO ACCEPT
ONE LAMP W/DALI FLAG OR FAULT.
NOTES:
3 AMPS PEAK
400V BUS TEST
HAVERSINE TEST
CLOSE TO U2
Swiss Control
110/220-VIN
TO-220

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