Design and experimental operation of a control strategy for the buck–boost DC–AC inverter

P. Sanchis, A. Ursúa, E. Gubía and L. Marroyo

Abstract: The buck–boost DC–AC inverter generates an alternating output voltage as the differential voltage of two DC–DC individual buck–boost converters that are driven with two 180° phase-shifted DC-biased sinusoidal references. The peak value of the inverter alternating output voltage does not depend on the direct input voltage. In addition, an advantage over the Boost DC–AC inverter is that the output voltages of both Buck–Boost converters are also independent of the direct input voltage. The difficulty of the topology lies in the control of both buck–boost DC–DC converters as they are required to work with variable operating-points. A double-loop control strategy is proposed for the buck–boost DC–DC converter with a new inner control loop for the inductor current and also a new outer control loop for the output voltage. These control schemes include different compensations that make possible a fast and accurate control of both converters with variable operating points. With these compensations, the controllers are easy to design, implement and develop. Furthermore, feedforward loops are included to increase the robustness of the inverter to external disturbances in both the input voltage and output load. The proposed control strategy is designed and implemented on a prototype 1.5 kW buck–boost DC–AC inverter. The control strategy is validated by means of both simulation and experimental tests. The results show that the proposed strategy achieves a robust, reliable and accurate control of the inverter even in hard situations such as nonlinear loads, sudden load changes and transient short circuits.

1 Introduction

The buck–boost DC–AC inverter consists of two individual buck–boost DC–DC converters that are driven with two 180° phase-shifted DC-biased sinusoidal output voltage references to generate a differential alternating output voltage [1, 2]. The power scheme of the buck–boost inverter is shown in Fig. 1. The idea of obtaining an alternating output voltage by means of combining two DC–DC converters has been analysed in the literature. In [3] the concept is analysed by means of the theory of phase-modulated inverters. In [1, 2, 4, 5], the particular operation of the boost and buck–boost DC–AC inverters is studied. These inverters show several advantages. The most important is that their output voltage is a naturally filtered alternating voltage whose peak value is independent of the direct input voltage, that is, it can be generated in a single stage from lower direct voltages. However, the buck–boost inverter incorporates an additional advantage in comparison with the boost inverter, which is that the individual output voltages of the buck–boost DC–DC converters are not required to be greater than the direct input voltage.

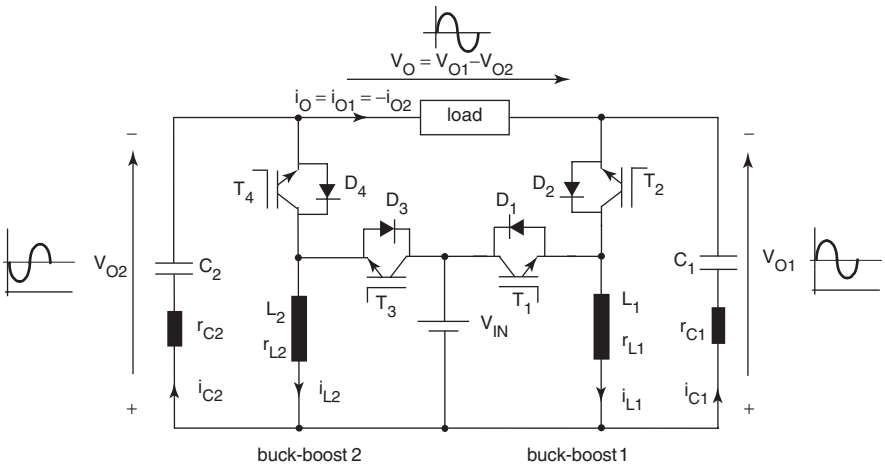

Fig. 1 *Buck–boost DC–AC inverter power scheme*

Due to the operation principle of the buck–boost inverter, both buck–boost converters have to be controlled

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IEE Proceedings online no. 20045139

doi:10.1049/ip-epa:20045139

Paper first received 25th August and in revised form 18th November 2004. Originally published online: 8th April 2005

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in a variable operating-point condition. Here lies the complexity of this inverter. Several techniques have been proposed to control the buck–boost [6–16]. Many of them are based on the well-known small-signal linear models such as current-mode control [6–9], robust control, H_∞ control and fuzzy logic control [10–14]. However, small-signal models are calculated for a particular point of operation and are valid to control the DC–DC converter only for small variations around this point. In the buck–boost inverter, the output voltages of both buck–boost converters experience large variations, and therefore these control techniques are not appropriate to achieve an accurate and stable control of both the buck–boost converters in such a variable operating condition. The sliding-mode control is a technique that can deal with this condition [2, 15, 16]. However, it has some disadvantages related to the required complex theory, the variable switching frequency, the lack of control of the average inductance current and the constraints in the selection of the controller parameters [17, 18].

To control both buck–boost converters, this paper proposes a double-loop control strategy that is able to control them in a variable operating point condition. An initial first theoretical approach of the proposed control strategy was introduced in [4]. Now, a prototype has been physically implemented and experimentally tested. The control strategy is based on the averaged continuous-time model of the buck–boost converter [19] and consists of a new inner control loop for the inductor current and an also new outer control loop for the output voltage. Both loops include compensations to decouple the converter model seen by the controller from the point of operation. In this way, the strategy is able to control both buck–boost converters in a variable operating condition such as that one required by the buck–boost inverter. Additionally, the control strategy makes use of some feed-forward compensations to improve the robustness against both input voltage and output AC disturbances. Simulation and experimental results validate the good qualities of the proposed control strategy. As shown, both buck–boost output voltages, and then the differential output alternating voltage, are accurately controlled, with high robustness against external disturbances. In addition, the direct control of the current makes possible to achieve a high reliability against transient short circuits and nonlinear loads, which can be in fact a source of small short circuits. The proposed control technique can be therefore considered as an advantageous alternative to the previously mentioned techniques.

2 Control scheme for buck–boost DC–DC converter

2.1 Buck-Boost averaged continuous-time model

The proposed control strategy is now developed and customised for the buck–boost 1 of Fig. 1. The control scheme for the second buck–boost is the same.

The averaged continuous-time model of buck–boost 1 is given by the following expressions, where i_{C1}, i_{L1} and i_{O1} are the capacitor, inductor and output currents, v_{L1}, v_{IN} and v_{O1} are the inductor, input and output voltages, and d_1 is the averaged continuous-time duty cycle

$$v_{L1} = v_{IN} d_1 - (1 - d_1) v_{O1} \tag{1}$$

$$i_{C1} = (1 - d_1) i_{L1} - i_{O1} \tag{2}$$

Concerning the inductance L_1 and capacity C_1, whose internal resistances are r_{L1} and r_{C1}, their differential equations are

$$v_{L1} = r_{L1} i_{L1} + L_1 \frac{di_{L1}}{dt} \tag{3}$$

$$i_{C1} + r_{C1} C_1 \frac{di_{C1}}{dt} = C_1 \frac{dv_{O1}}{dt} \tag{4}$$

The model given by (1) to (4) describes the buck–boost dynamic behaviour up to half the switching frequency [19]. These equations show bilinear dynamics that make the control of the buck–boost quite difficult. To deal with it, a double-loop control scheme is proposed with a new inner control loop for the inductor current and an also new outer control loop for the output voltage.

2.2 Proposed inner control loop for inductor current

The proposed inner control loop for the inductor current is shown in Fig. 2. Capital letters are used for the variables in the block diagram. The system to be controlled is defined by (1) and (3). In this system the term $v_{O1}+v_{IN}$ behaves as a variable gain, and v_{O1} as an external disturbance. The input to the system is the duty cycle d_1. If this variable is chosen to be the control variable, the variable gain $v_{O1}+v_{IN}$ makes very difficult, almost impossible, the design of a controller that stabilises the system under a variable operating condition. The proposal is to choose the inductor voltage v_{L1} as the control variable instead of the duty cycle d_1, as shown in Fig. 2. From the inductor voltage reference generated by the controller v_{L1ref}, the duty cycle d_1 can be obtained by means of the following expression, derived from (1):

$$d_1 = \frac{v_{Lref} + v_{O1}}{v_{O1} + v_{IN}} \tag{5}$$

The proposed control scheme can also be considered from another point of view. First, the variable gain $v_{O1}+v_{IN}$ is compensated by means of its inverse value. This compensation can be made thanks to the much higher bandwidth of the current loop in comparison with the output voltage bandwidth. Secondly, the influence of v_{O1} is cancelled by adding to the loop its sensed and filtered value with opposite polarity, which acts in fact as a feedforward compensation. With these compensations, the plant to be controlled is just the inductor transfer function, and then a

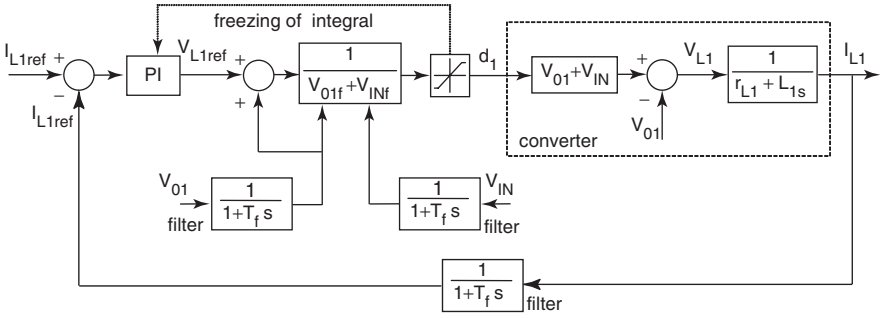

Fig. 2 *Proposed inner control loop for inductor current*

simple proportional–integral (PI) controller can be used. The required division in (5) is not a problem as the denominator is always greater than zero, and can be done by means of either simple analogue circuits or digital programming. Finally, the duty cycle is limited in order to avoid extreme voltages and a non-constant switching behaviour, with the corresponding freezing action of the integral term.

2.3 Proposed outer control loop for output voltage

The scheme of the outer control loop proposed for the output voltage is shown in Fig. 3. Again, capital letters are used for the variables. This scheme is based on the same philosophy as the current loop. The system to be controlled is defined now by the (2) and (4), and the current control loop. If the reference for the current loop i_{L1ref} were chosen to be the control variable, the plant seen by the controller would exhibit a gain defined by $1-d_1$. This gain is variable because the buck–boost operates in a variable operating condition. The proposal is now to use the capacitor current as the control variable. However, the reference for the inductor current cannot be directly obtained by means of (2) as that implies the use of the duty cycle. The dynamics of the duty cycle are defined by the inner current loop, and its use to calculate the reference for this loop would couple both loops and could make the system unstable. The proposed solution is to compensate $1-d_1$ with $(v_{IN}+v_{O1})/v_{IN}$, as shown in the control scheme of Fig. 3. With this solution, duty cycle variations up to the voltage loop bandwidth will be successfully compensated and voltage references in this frequency range will be accurately tracked by the control loop. In addition, the current i_{O1}, which is the same as i_O, acts as an external perturbation that affects the control loop, especially during sudden load variations. A feedforward compensation is again used to minimize this effect. With these compensations, the current reference i_{L1ref} is then obtained from the following expression, in which the control variable is the reference for the capacitor current i_{C1ref}:

$$i_{L1ref} = \frac{v_{IN} + v_{O1}}{v_{IN}} \left(i_{C1ref} + i_{O1} \right) \tag{6}$$

Again, the proposed compensations can be done by means of simple analogue circuits or digital programming. As the inductor current can be considered instantaneously controlled from the point of view of the voltage control loop, the plant to be controlled appears as the capacitor transfer function. Therefore a PI controller can be again used and easily designed by traditional techniques. The current reference is limited and the corresponding freezing action is taken over the integral part in this situation.

3 Control of buck–boost DC–AC inverter

To achieve an alternating voltage at the output of the inverter, both buck–boost DC–DC converters are driven with two DC-biased 180° phase-shifted voltage references

$$v_{Oref} = \sqrt{2} V_{rms} \sin(2\pi f t) \tag{7}$$

$$v_{O1ref} = V_{DC} + \frac{1}{2} v_{Oref} = V_{DC} + \frac{1}{\sqrt{2}} V_{rms} \sin(2\pi f t) \tag{8}$$

$$v_{O2ref} = V_{DC} - \frac{1}{2} v_{Oref} = V_{DC} - \frac{1}{\sqrt{2}} V_{rms} \sin(2\pi f t) \tag{9}$$

where v_{Oref} is the reference for the buck–boost inverter, v_{O1ref} and v_{O2ref} are the references for both individual buck–boost converters, f and V_{rms} are the frequency and RMS value of the output voltage, and V_{DC} is the DC-bias voltage. The main disadvantage of the independent references shown in (8) and (9) is that the output voltage is not directly controlled. It can therefore be affected by DC offsets and show a poor rejection to external disturbances. An alternative is to drive one buck–boost with an independent reference (e.g. buck–boost 1), and then use the other buck–boost to control directly the inverter output voltage [4, 18]

$$v_{O2ref} = v_{O1} - v_{Oref} = v_{O1} - \sqrt{2} V_{rms} \sin(2\pi f t) \tag{10}$$

This alternative is used in the implementation of the control strategy on the prototype inverter.

4 Simulation analysis

4.1 Prototype inverter

To validate the proposed control strategy a prototype buck–boost inverter has been designed and built and the proposed control strategy implemented. The parameters of the prototype inverter are

$$\begin{aligned} &L_1 = L_2 = 128\,\mu\text{H} \quad C_1 = C_2 = 80\,\mu\text{F} \\ &f_s = 20\,\text{kHz} \quad P_N = 1.5\,\text{kW} \\ &v_{IN} = 48\,\text{V} \quad V_{rms} = 125\,\text{V} \\ &V_{DC} = 108\,\text{V} \quad f = 60\,\text{Hz} \end{aligned} \tag{11}$$

where the only parameters that have not been mentioned before are f_s, which is the switching frequency, and P_N, which denotes the rated power. The inductances exhibit internal resistances of around 10 mΩ. Those of the capacitors are close to 350 mΩ.

The simulation results have been obtained by means of Matlab/Simulink® and are shown in this Section. The physical implementation of the prototype inverter is described in the following Section together with the experimental results.

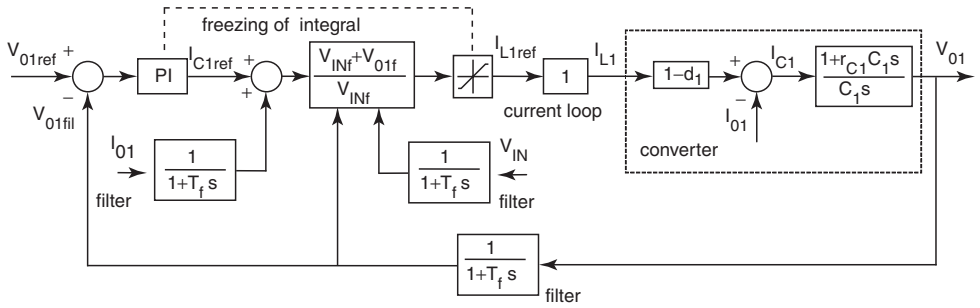

Fig. 3 *Proposed outer control loop for output voltage*

The prototype inverter incorporates the proposed control strategy. The double-loop control scheme already described together with the proposed current and voltage control loops is implemented in each buck–boost. The controllers are designed to track voltage references of 60 Hz. The specifications for the PI controller of the current loop are a bandwidth of 4 kHz and a phase margin of 50°. For the PI controller of the voltage loop, the bandwidth is set to 500 Hz and the phase margin to 50°. With these specifications, the proportional and integral constants (K_P and T_n, respectively) are 3.51 and 1.64×10^{-4} for the current loop, and 0.202 and 4.31×10^{-4} for the voltage loop. The saturation limits for the current reference can be selected as a trade-off between the maximum allowable overcurrent in transient situations and the rated characteristics of the inverter elements. According to these design guidelines, the limits are set to 125 and −50 A for the prototype inverter. Finally, the references for both buck–boost of the inverter are set in the way described by (8) and (10).

4.2 Simulation results

Simulation results for the inverter operating at rated power are shown in Fig. 4. As shown, the proposed control scheme achieves an accurate control of the voltages and currents, with a Total harmonic distortion (THD) of the inverter output voltage of 0.68%.

The robustness of the control strategy against disturbances in the input voltage is shown in Fig. 5. Now, a 10% 120 Hz square-wave disturbance has been added to the input voltage. Due to the compensations included in the loops, both buck–boost reject effectively this disturbance, and then the inverter output voltage remains stable and controlled.

The reliability of a generation unit when supplying loads in an autonomous electric network, particularly its ability to overcome transient situations with no activation of its protections, is a very important aspect. Transient short circuits are a typical example of these situations. They can appear as a consequence of the connection of non-linear loads consisting of a diode bridge and a flat capacitor. They can also appear due to faults in the loads connected to the inverter. In this case, the short circuit lasts until the load protection fuse blows. These situations are tested in Fig. 6 and 7. In Fig. 6, a nonlinear load consisting of a diode bridge, a flat capacitor and a resistive load, is suddenly connected while the inverter is already supplying 70% of nominal power to a linear load. Figure 7 shows the inverter response to a short circuit of 1ms at the output when it is supplying rated power. In both situations, the currents are controlled up to their saturation limits (125 A and –50 A) during the short circuits, and the system returns to normal behaviour when they finish with high stability and no oscillations.

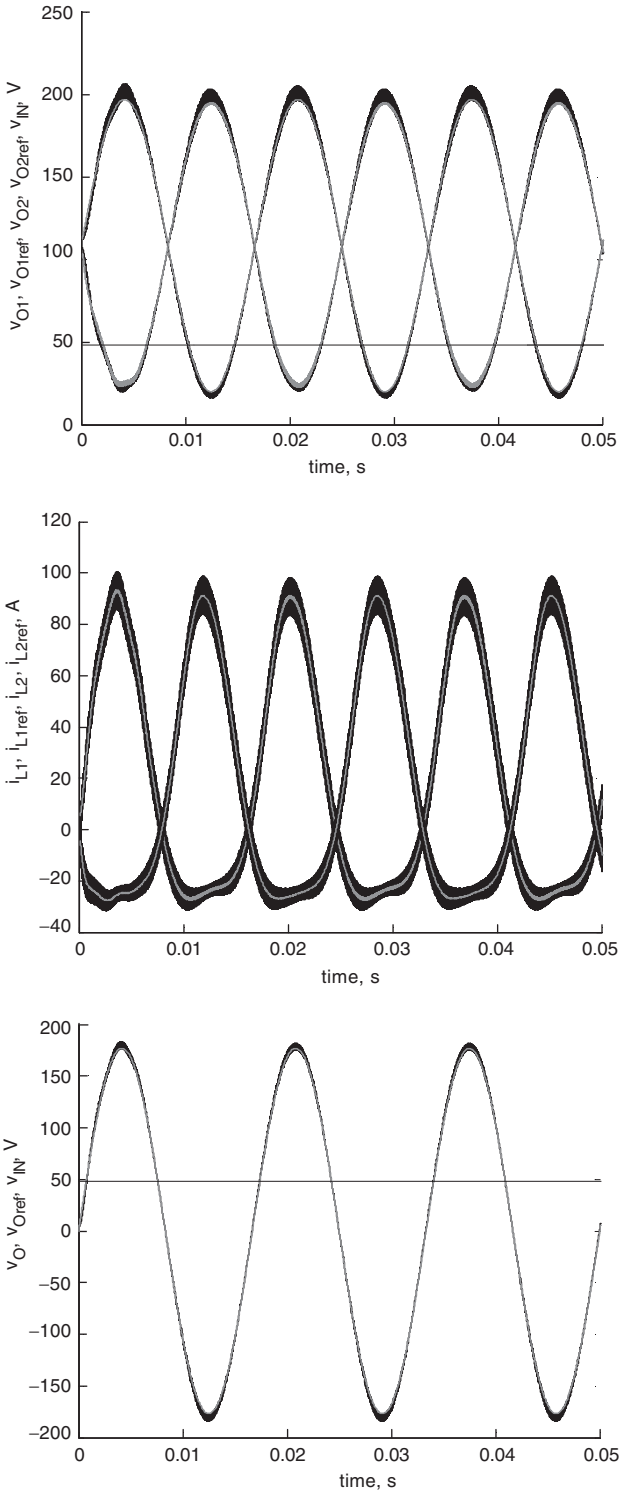

Fig. 4 *Simulated inverter operation at rated power*

5 Experimental validation

5.1 Physical implementation of 1.5 kW prototype inverter

The parameters of the prototype inverter were indicated in (11). Inductors L_1 and L_2 are two 128 μH 60 A-rated RMS-current inductors. The choice of inductor RMS-current is based on the theoretical current waveform, which has been obtained by means of solving the corresponding differential equation by numerical methods. Capacitors C_1 and C_2 are two 80 μF 500 V electrolytic capacitors. For the switching stage of both buck–boost circuit two Semikron SKM150GB123D modules are used [20]. Both are mounted on a Semikron P16/350 heatsink. Drivers for the IGBT are of type SKHI 23/12, also from Semikron, and the on- and off-gate resistances are 6.8 Ω.

The overall implementation of the control strategy is shown in Fig. 8. The voltage control loops of both buck–boost converters as well as the generation of their references are digitally implemented on a DS1104 board from dSPACE [21]. The current control loops are implemented together with the generation of the PWM switching commands in an analogue board. This board receives from the DS1102 board the current references. The duty cycles d_1 and d_2 are calculated from the current control loops, and then the PWM switching commands are generated for the SKHI 23/12 drivers. The duty cycles are limited to between

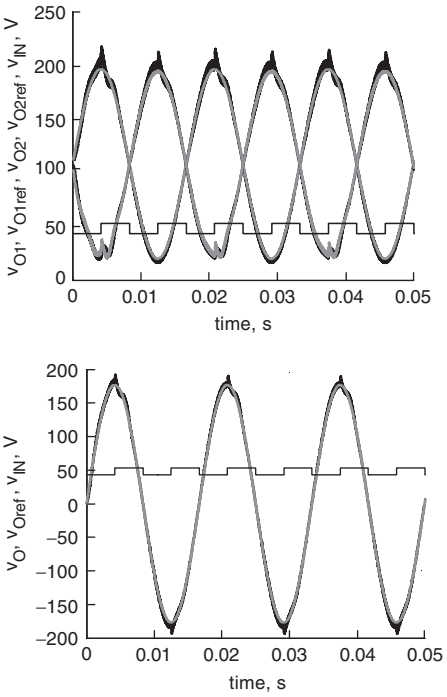

Fig. 5 *Simulated robustness against disturbance in the input voltage of 10% 120 Hz square wave*

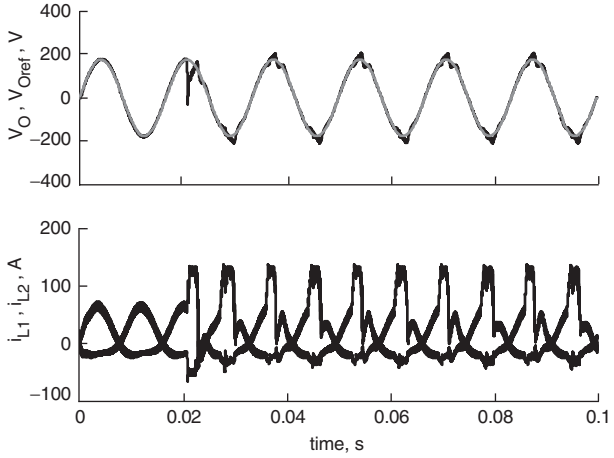

Fig. 6 *Simulated system response to 400 W nonlinear load connection while supplying 70% linear load*

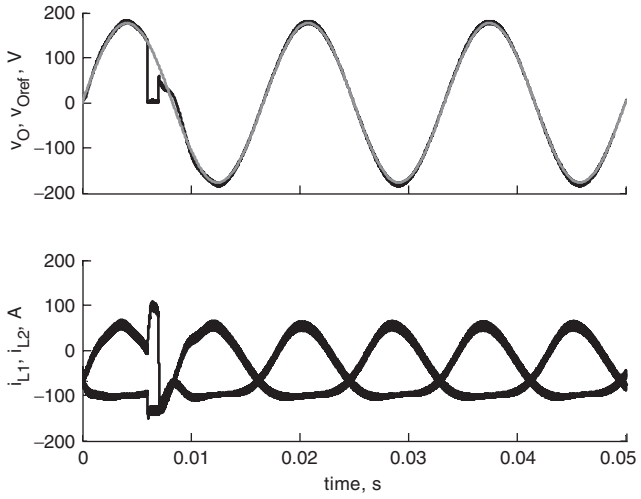

Fig. 7 *Simulated system response to transient short circuit from $t = 6$ ms to $t = 7$ ms*

0.05 and 0.95. Analogue protections for the currents and voltages are included in the analogue the board. When they are activated an inhibit signal stops the operation of the boards and drivers. Finally the parameters for the PI controllers are those indicated in the previous Section.

The electronic circuitry that implements the current control loop and the generation of the PWM switching commands for the buck–boost 1 is shown in Fig. 9. The circuitry for the buck–boost 2 is the same, and both are integrated in the analogue board. Current measuring is made by means of a LEM LA 125-P current sensor, while voltages measuring are carried out by means of LEM LV 25-P voltage sensors. The operational amplifiers are TL084 and the comparators are LM311. The mathematical division required to compensate $v_{O1} + v_{IN}$ is made by means of an AD632 from Analog Devices. From the duty cycle, a UC3637 from Unitrode generates the PWM switching commands for the SKHI 23/12 drivers, which have been included in Fig. 9 to clarify the operation of the circuit. The B-outputs of the UC3637 are used by the control circuitry of buck–boost 2. The 1.5 nF capacitors together with the 4.7 kΩ resistances at the output of the LM311 comparators are used to implement a dead time of 2 μs. The inhibit signal

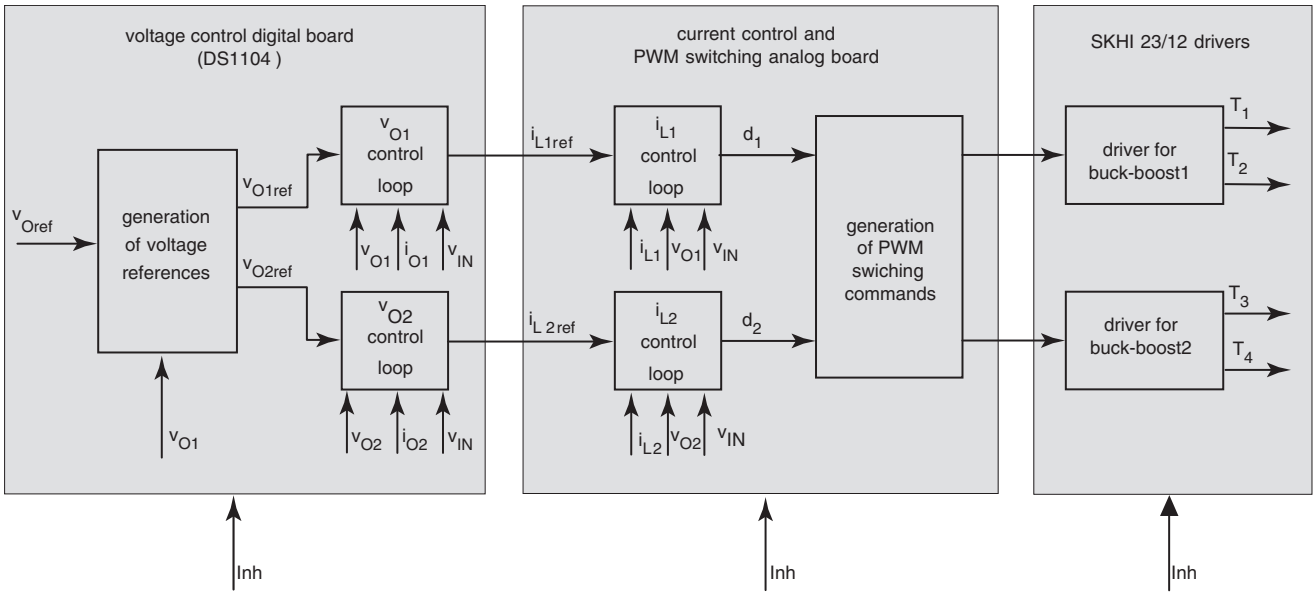

Fig. 8 *Overall implementation of proposed control strategy*

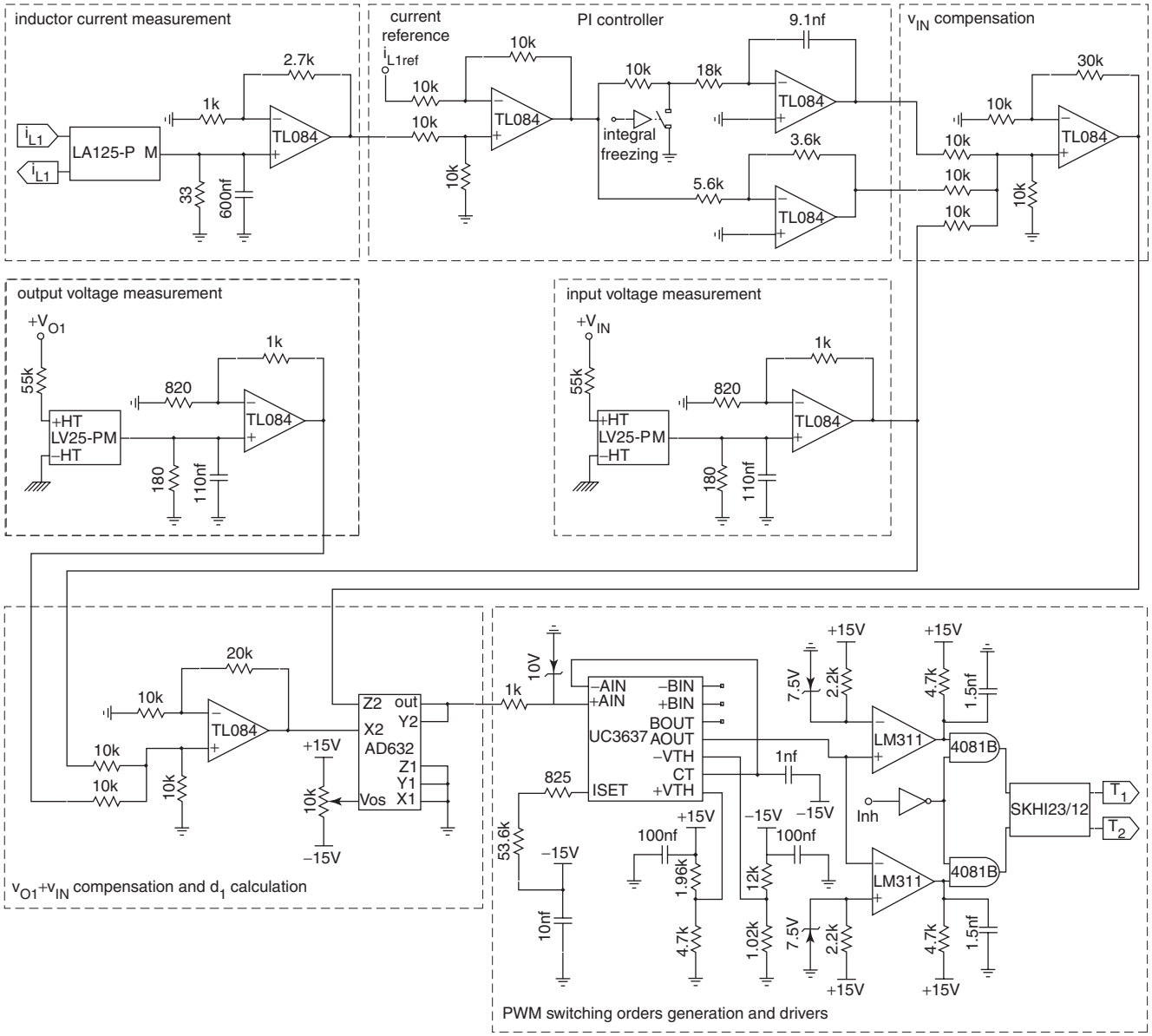

Fig. 9 *Circuitry for current control loop and generation of PWM switching commands for buck–boost 1 (buck–boost 2 is identical)*

can cancel the switching commands by means of HEF4081B AND-gates.

5.2 Experimental results

The prototype inverter with the proposed control strategy has been experimentally tested in different situations, which are summarised in Fig. 10. As shown in this figure, the tests include linear and nonlinear load operation, and transient short circuits. The linear load is a 10 Ω resistive load, which makes the inverter operate at full power. The nonlinear load consists of a Semikron SKB 30/08 diode bridge, a 680 μF capacitor and a 68 Ω resistive load. The short circuit test is carried out by means of directly short-circuiting the inverter output through a fuse. The short-circuit finishes when the fuse blows. A Tektronix TDS 5054 digital phosphor oscilloscope is used to register the obtained waveforms.

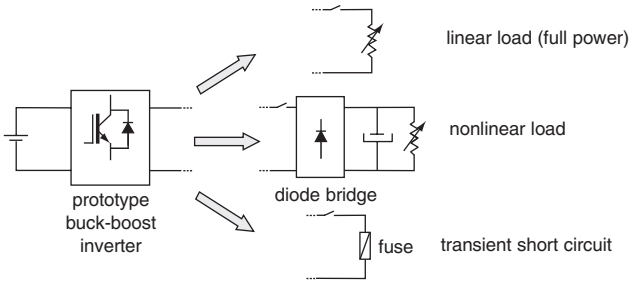

Fig. 10 *Experimental tests on prototype inverter*

Figure 11 shows the results when the inverter operates at full power and supplies the 10 Ω resistive linear load. Figure 11*a* shows the buck–boost output voltages v_{O1} and v_{O2}, and the inverter input and output voltages, v_{IN} and v_O. Figure 11*b* shows the inverter output voltage v_O and current i_O. Finally Fig. 11*c* presents the inductor currents i_{L1} and i_{L2} of both buck–boost together with the output voltages v_{O1} and v_{O2}. The practical results shown in these graphs validate the proposed control strategy and the simulation results. Figure 11*a* and 11*c* show how the proposed control strategy achieves an accurate control of the inductor currents and output voltages, and consequently of the inverter output voltage at full power. Other than validating the proposed control strategy, these results highlight the advantages of the buck–boost inverter. The DC–AC conversion is carried out in a single stage from DC levels that are lower than the

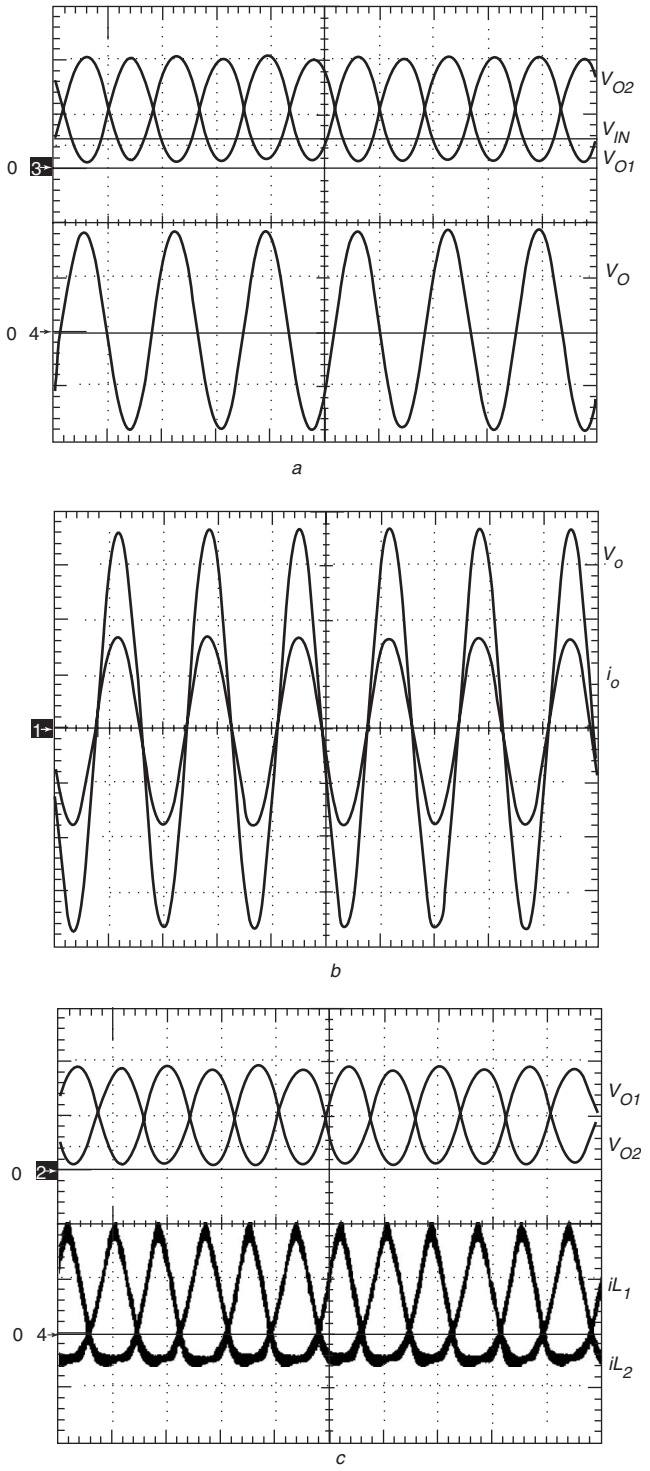

Fig. 11 *Experimental results at full power with linear load (10 ms/div)*
a Input and output voltages v_{O1}, v_{O2}, v_{IN}, v_O 100V/div
b Inverter output voltage and current v_O 50V/div; i_O 10A/div
c Inductor currents and output voltages of both buck–boost v_{O1}, v_{O2} 100V/div; i_{L1}, i_{L2} 50A/div

AC peak voltage. Furthermore, the buck–boost output voltages v_{O1} and v_{O2} are not required to be greater than the input voltage v_{IN} as it happens with the boost DC–AC inverter. On the contrary, a disadvantage of the buck–boost inverter lies in the inductor current waveforms, which can achieve high peak values and increase the losses in both the IGBTs and the inductors. The robustness against output current disturbances is shown in Fig. 12, where the 10 Ω resistive linear load, which consumes full power, is suddenly

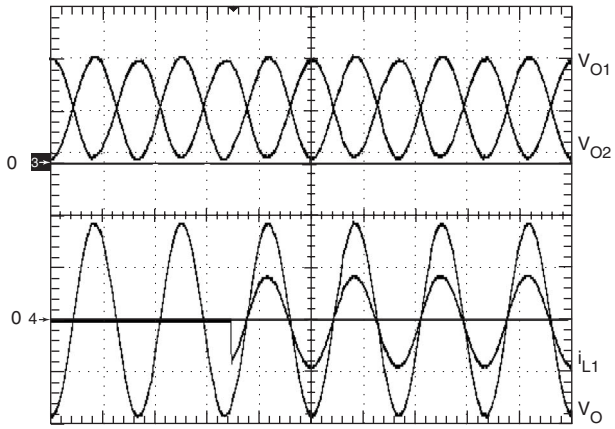

Fig. 12 *Experimental response to connection of linear load demanding full power (v_{O1}, v_{O2}, v_O 100 V/div; i_O 20 A/div; 2 μs/point)*

connected to the inverter. As shown, the output voltages reject this disturbance even when the load is connected at the maximum voltage.

The inverter starting response is tested in Fig. 13. Initially, both buck–boost capacitors are precharged up to their DC component. In Fig. 13*a* the starting of the inverter is carried out softly from zero volts. In Fig. 13*b* the starting is carried out at the peak values of the output voltage waveforms. The inverter starting response is in both situations stable and accurately controlled.

The operation with the nonlinear load is shown in Fig. 14. This test shows both the nonlinear load connection

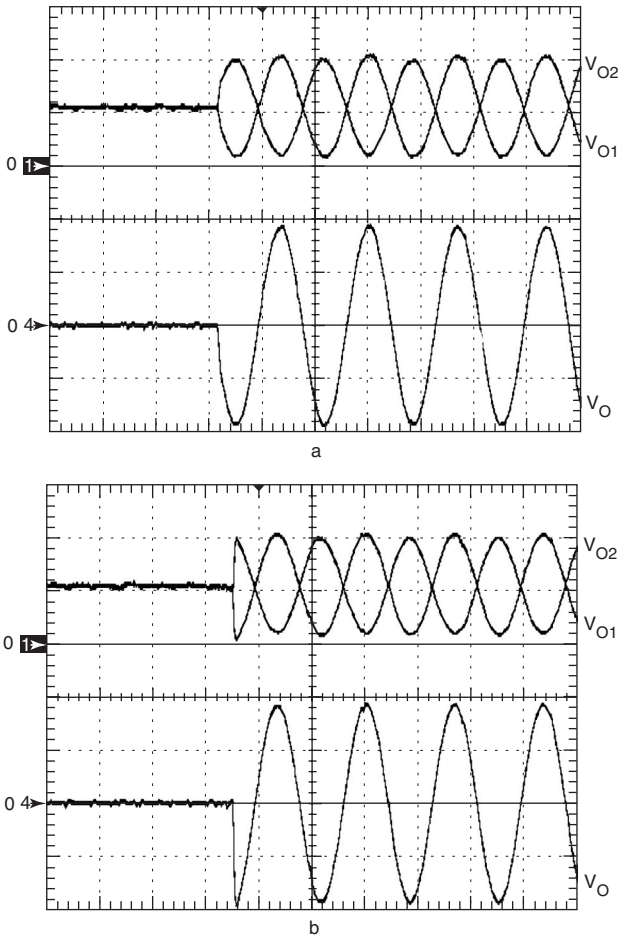

Fig. 13 *Experimental inverter starting response (v_{O1}, v_{O2}, v_O 100 V/div; 10 ms/div)*

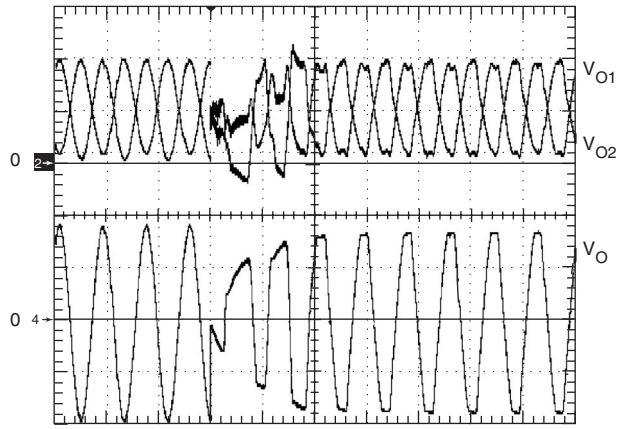

Fig. 14 *Experimental response to nonlinear load connection (v_{O1}, v_{O2}, v_O 100 V/div; 20 ms/div)*

and the normal operation with this load. The connection is in fact a short circuit, as the capacitor is discharged, and this short circuit appears again shortly at the maximum and minimum peaks of the voltage waveforms. The response of the inverter is stable and controlled. The stability of the system in these situations in which small short circuits appear can be achieved thanks to the inner current control loops, which control the currents to its maximum programmed value during the short circuits.

Finally the last test involves a direct short circuit at the output of the inverter by means of the sudden connection of a fuse. The upper and lower limits of the current reference are set to 20- and 20 A to make possible a long short circuit (almost nine cycles). Higher limits decrease the melting time of the fuse and the short-circuit duration. The results are shown in Fig. 15, where the short circuit lasts around 140 ms. During this time, the output voltage v_O goes zero, the buck–boost voltages v_{O1} and v_{O2} are the same, and the current i_{L1} is always controlled to its upper and lower limits. Although it has not been included, current i_{L2} has the same evolution except for the 180° phase shift. This test validates the high reliability of the inverter in these situations. As the currents are controlled to their limit values, no protections are activated and the system returns back to its normal operation when the short-circuit finishes. Obviously, long-short circuits have to be always avoided, and the protections can be programmed to be activated when the short circuit lasts more than a given maximum time.

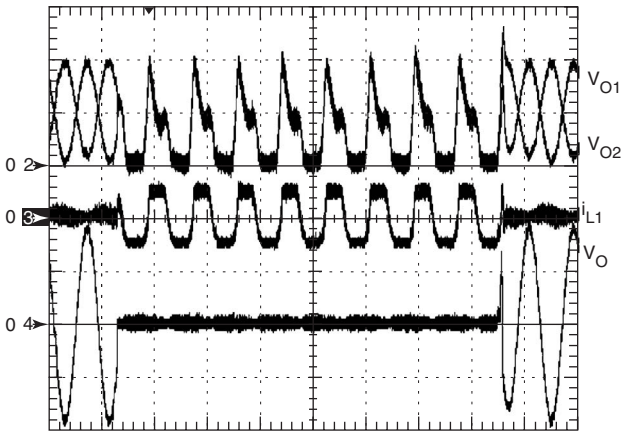

Fig. 15 *Experimental response to transient short circuit (v_{O1}, v_{O2}, v_O 100 V/div; i_{L1} 40 A/div; 20 ms/div*

6 Conclusions

The two buck–boost DC–DC converters of the buck–boost DC–AC inverter are required to work in a variable operating-point situation. To deal with this condition, a double-loop control strategy for these DC–DC converters have been proposed that consists of a new inner control loop for the inductor current and an also new outer control loop for the output voltage. These loops include different compensations that make possible the control of the buck–boost DC–DC converter with variable operating points. In addition, feedforward additional loops were included to improve the robustness against disturbances in the input voltage and output current.

The proposed control strategy was designed and implemented on a 1.5 kW buck–boost DC–AC inverter. Several simulation and experimental tests were carried out to validate the strategy. The results show that the proposed strategy achieves a stable and accurate control of both DC–DC converters, and then of the inverter output voltage. Additionally to the tests carried out at normal operation with linear loads, the strategy is also tested in challenging situations. Experimental results with nonlinear loads consisting of a diode bridge and a flat capacitor, as well as with transient short circuits, show that the proposed strategy is capable to deal with these situations and control the system with high robustness and reliability.

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