Driving Your MOSFETs Wild to Obtain Greater Efficiencies, Power Densities, and Lower Overall Costs.

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***Abstract*— Gate driver selection guidelines and rules for driving Standard, Q-Class and F-Class MOSFETs are presented. A summary of key gate driver application issues and recommended use rules are given. A series of tables providing the recommended gate driver type, gate resistor value, and recommended application output power are provided for $f_{(PWM)}$ switching frequencies from 100KHz to 4MHz.**

I. Introduction

Power supply and system designers are constantly being pressed for greater efficiencies, greater power densities, and lower overall cost per Watt. Of particular interest are two families of low gate charge, $Q_{g\,(on)}$, ***MOSFETs*** available from IXYS specifically developed to reduce both switching speed and switching losses, the Q-Class and the F-Class. The Q-Class and the F-Class ***MOSFETs*** improve upon the standard MOSFET $Q_{g\,(on)}$ with a proprietary technique, which reduces the gate to drain feedback capacitance, C_{rss}. The F-Class MOSFETs make further improvements upon this with parameters optimized for soft and resonant switching applications. IXYS now offers a full selection of single and dual gate drivers to efficiently drive the Q-Class and F-Class MOSFETs as well as a wide selection of standard MOSFETs. Table 1 gives a summary of the new gate drivers available from IXYS. Included are the three gate driver selection tables, Table 2 for standard MOSFETs, Table 3 for Q-Class MOSFETs, and Table 4 for F-Class MOSFETs. A more expanded set of selection tables which take into account all of the MOSFET voltage and current ratings as well as IGBTs, IGBT modules, and MOSFET modules will be provided soon at www.ixys.com.

II. Circuit Application Assumptions

The gate driver selection tables, Table 2 through Table 4, take into account the MOSFET type, its operating voltage, its rated drain current, its PWM switching frequency, and its recommended SMPS output power rating. The Table 2 and Table 3 for the standard MOSFETs and the Q-Class MOSFETs respectively assume hard switching SMPS applications with total t_r and t_f limited to no more than 2% of the PWM period. Table 4 for the
F-Class MOSFETs assume resonant mode - soft switching applications with total t_r and t_f at 10% of the PWM period. All three tables provide the recommended gate driver and

the recommended maximum value of the external gate resistor. The gate resistor values are chosen as a maximum allowable value for maintaining stability and minimizing spurious switching noise generation, and still keep within their respective t_r and t_f limits. The three tables also provide a computed total gate drive circuit power dissipation for a first order snapshot of the expected efficiency in relation to the recommended SMPS power output column contained in the tables.

It is assumed in discussions to follow that the gate driving circuit is a lossy system, where the gate driver, the gate resistor, and any internal gate resistance of the driven MOSFET dissipates energy. The author has taken liberty to use a somewhat arbitrary set of "rules of thumb" in the discussion of allowable t_r and t_f times with respect to the total switching period for "hard" or non-resonant switched systems at 1% of the total PWM period, and for "soft" or resonant switched systems at 10% for the total cycle PWM period. It is believed that times less than t_r and t_f recommended in these two different instances increases the difficulty in containing or controlling switched EMI or electrical noise, and switching times greater than those recommended tend to reduce the overall efficiency or energy savings of the SMPS system.

III. IXYS GATE DRIVERS

Table 1 provides a snapshot of the new IC gate drivers produced by IXYS and referred to in this article. There are other gate drivers not presented here with features and functions not available from those in Table 1 that IXYS has developed and is developing, so please visit our web site at www.ixys.comfor the latest information. There are alternate sources to some of the gate drivers presented in Table 1 so if interested, please contact IXYS for alternate source manufacturers. The gate drivers in Table 1 are segregated by their output current capability.

New Gate Driver Family From IXYS

Gate Driver Part #	Product Family	Description	Output Current	Packages Available	Package Codes
IXDD402	Dx402	Dual, Noninv with EN	2 x 2Amp	PI, SI, SI-16	PI -- 8 Pin Dip
IXDF402	Dx402	Dual, Noninv & Inv	2 x 2Amp	PI, SI, SI-16	SI—SO8 or SO14
IXDI402	Dx402	Dual Inv	2 x 2Amp	PI, SI, SI-16	SI-16--SO16
IXDN402	Dx402	Dual Noninv	2 x 2Amp	PI, SI, SI-16	CI--TO220
IXDD404	Dx404	Dual, Noninv with EN	2 x 4Amp	PI, SI, SI-16	YI--TO262
IXDF404	Dx404	Dual, Noninv & Inv	2 x 4Amp	PI, SI, SI-16	
IXDI404	Dx404	Dual Inv	2 x 4Amp	PI, SI, SI-16	
IXDN404	Dx404	Dual Noninv	2 x 4Amp	PI, SI, SI-16	
IXDD408	DD408	Noninv with EN	8Amp	PI, SI, CI, YI	
IXDD409	Dx409	Noninv with EN	9Amp	PI, SI, CI, YI	
IXDI409	Dx409	Inverting	9Amp	PI, SI, CI, YI	
IXDN409	Dx409	Noninverting	9Amp	PI, SI, CI, YI	
IXDD414	Dx414	Noninv with EN	14Amp	PI, SI, CI, YI	
IXDI414	Dx414	Inverting	14Amp	PI, SI, CI, YI	
IXDN414	Dx414	Noninverting	14Amp	PI, SI, CI, YI	

Table 1

In applying of all of the gate drivers from IXYS and those available from other vendors, here are some universal rules:

1. The gate driver power pins, V_{CC} and GND, need to be bypassed by a low Electrical Series Resistance, ESR, and a low ESL, Electrical Series Inductance, capacitor. An example of such a capacitor is a high quality surface mountable monolithic ceramic bypass capacitor.
2. This bypass capacitor must be placed physically as close to the gate driver as possible, within 3mm (0.125") or so. The best physical placement of the bypass capacitor is to let it straddle the V_{CC} and GND pins on the other side, (the solder side as opposed to the component side) of the driver V_{CC} and GND power pads.
3. The value of this bypass capacitor must be at a minimum 50 times the value of the driven device input gate capacitance, C_{ISS}.
4. The gate resistor must be non-inductive, with carbon composition being the best, carbon film or metal film the second best, and the wirewound being the worst. It is not recommended that wirewound resistors be used as gate resistors.
5. The path of the area enclosed by the gate driver output, to the gate resistor, to the gate terminal of the driven device, with respect to the gate driver GND terminal to the source terminal of the driven device must be minimized.

Overall inductances of the gate driver output to the driven MOSFET as well as the driven MOSFET source to the driver GND must be minimized.

6. The total distance traversed from the gate driver to the driven MOSFET must be minimized, the shorter the better.

III. Driving Standard MOSFETS

The Table 2 provides a gate driver selection table for three different current ratings of standard IXYS MOSFETs. The second column shows the gate charge, $Q_{g\,(on),}$ the third column the peak gate current, I_g, needed to swing the MOSFET gate from 0V to V_{CC} =+15V and back to 0V within 1%, (t_r=0.5% and t_f=0.5% for a total of 1%) of the PWM frequency period, $f_{(PWM)}$=100KHz, or

$$I_g=Q_{g\,(on)}*(1/.\,01)*f_{(PWM)}.$$

The fourth column provides the recommended maximum value of external gate resistor, whose value is calculated as:

$$R_g=2/3*V_{CC}/I_g$$

where V_{CC} =15V. The fifth column is the total power dissipated in the gate driving circuit, which is represented by

$$P_g= Q_{g\,(on)}* V_{CC} * f_{(PWM)}.$$

The sixth column is the recommended gate driver product family. The asterisk next to the driver signifies the driver must be heat sunk and must be either in the surface mountable TO262 or the through hole TO220 packages. The data is repeated for $f_{(PWM)}$=200KHz and $f_{(PWM)}$=400KHz. The very last column shows the recommended power output rating of the SMPS system using the MOSFET given in the first column. It can be seen from Table 2 that in a typical half bridge SMPS output configuration where there is an upper and a lower MOSFET switch of similar size, and with the recommended power output rating of 500Watts, approximately 0.04% of the energy is lost in the gate drive system at 100KHz, a negligible value for today's 95% efficient system. At 400KHz, still only 0.2% of the total energy output is predicted to be consumed by the gate drive system, or approximately 4% of the total energy budget for a ~95% efficient SMPS system.

Driving Standard IXYS MOSFETs

		f_{PWM} = 100kHz				f_{PWM} = 200KHz				f_{PWM} =400KHz				
Standard MOSFET	Q_g in nC	Peak I_g in Amp	R_g in Ohm	Total Pg W	Gate Drvr	Peak I_g in Amp	R_g in Ohm	Total Pg W	Gate Drvr	Peak I_g in Amp	R_g in Ohm	Total Pg W	Gate Drvr	Rcmd Pwr Out
IXFH6N100	88	0.9	11.4	0.1	Dx402	1.8	5.7	0.3	Dx404	3.5	2.8	0.5	Dx404	500W
IXFH12N100	122	1.2	8.2	0.2	Dx402	2.4	4.1	0.4	Dx404	4.9	2.0	0.7	DD408	1KW
IXTK21N100	250	2.5	4.0	0.4	Dx404	5.0	2.0	0.8	DD408	10.0	1.0	1.5	Dx414*	2KW

Table 2

IV. DRIVING Q-CLASS MOSFETS

The Q-Class series of MOSFETs are optimized for low gate charge, $Q_{g\,(on)}$, to reduce gate drive energy loss. Table 3 provides the gate driver selection table for the Q-Class MOSFETs whose current and voltage ratings were selected to be similar to the ones in Table 2 for comparison purposes. The most straightforward way of improving the efficiency of an existing SMPS system design is to simply replace the standard MOSFET used with an equivalent Q series MOSFET of the same $R_{ds\,(on)}$ and voltage rating, --- a no brainer! An examination of the two tables, Table 2 and Table 3 at $f_{(PWM)}$=400KHz shows that the total energy lost in the gate drive system, P_g, has been reduced by 50% to 80%.

Driving Q-Class MOSFETs

		f_{PWM} = 200KHz				f_{PWM} = 400KHz				f_{PWM} = 800KHz				
Q-Class MOSFET	Q_g in nC	Peak I_g in Amp	R_g in Ohm	Total Pg W	Gate Drvr	Peak I_g in Amp	R_g in Ohm	Total Pg W	Gate Drvr	Peak I_g in Amp	R_g in Ohm	Total Pg W	Gate Drvr	Rcmd Pwr Out
IXFH6N100Q	48	0.96	10.4	0.1	Dx402	1.9	5.2	0.28	Dx402	3.84	2.6	0.57	Dx404	500W
IXFH12N100Q	90	1.8	5.6	0.3	Dx404	3.6	2.8	0.5	DD408	7.2	1.4	1.1	Dx409*	1KW
IXFH21N100Q	170	3.4	2.9	0.5	Dx408*	6.8	1.5	1.0	Dx409*	13.6	0.7	2.0	Dx414*	2KW

Table 3

It is my belief that non-resonant hard switching techniques not be used for $f_{(PWM)}$ much above 1MHz. As one increases the $f_{(PWM)}$ up to and beyond 1MHz, EMI and generated switching noise becomes a bigger and bigger problem, device energy losses as a result of finite storage times of the diodes used become an increasing problem which must be dealt with, and the charging and discharging of the stray and parasitic capacitors which are part of the switching devices become a growing energy loss problem which must also be dealt with. If the desired application requires rapid transient response capability that only a multi-MHz converter can provide, one might investigate the use of multi-phase converters where transient response capability increases with the increase in the number of phases and yet keeps the PWM switching frequency well under 1 MHz.

V. DRIVING F-CLASS MOSFETS

The single most effective way to improve power densities of SMPS is to increase $f_{(PWM)}$. The F-Class MOSFETs were designed to eliminate several key limitations of power MOSFETs to efficiently switch in the multi-MHz region. In addition to reduced $Q_{g\,(on)}$, the F-Class MOSFET has approximately $1/10^{th}$ the internal gate resistance of standard

MOSFETs, and its forward transconductance, g_{fs}, is stabilized. The reduced internal gate resistance significantly improves switching times, and the stabilization of g_{fs} minimizes spurious oscillations during soft or resonant switching.

The Table 4 provides a gate driver selection chart for the F-Class MOSFETs used in soft or resonant switching applications. Table 4 was developed with the total allowable t_r and t_f to be less than 10% of the total switching cycle. Again, for comparison purposes, similar current and voltage rating F-Class MOSFETs were selected for Table 4.

Driving F-Class MOSFETs

	f_{PWM} = 1MHz				f_{PWM} = 2MHz				f_{PWM} = 4MHz				
Q-Class MOSFET	Q_g in nC	Peak I_g in Amp	R_g in Ohm	Total Pg W	Gate Drvr	Peak I_g in Amp	R_g in Ohm	Total Pg W	Gate Drvr	Peak I_g in Amp	R_g in Ohm	Total Pg W	Gate Drvr	Rcmd Pwr Out
IXFH6N100F	54	1.08	9.3	0.8	Dx402	2.16	4.6	1.6	DD408*	4.32	2.3	3.2	DD408*	500W
IXFH12N100F	77	1.54	6.5	1.2	DD408*	3.08	3.2	2.3	DD408*	6.16	1.6	4.6	Dx409*	1KW
IXFK21N100F	160	3.20	3.1	2.4	DD408*	6.40	1.6	4.8	Dx409*	12.80	0.8	9.6	Dx414*	2KW

Table 4

VI. Conclusion

A summary of the new family of gate driver products from IXYS was provided in Table 1. The new gate drivers provide an extremely low cost alternative for discrete low voltage MOSFET or transistor buffers. Gate driver selection tables for the standard, Q-Class, and the F-Class MOSFETs were provided in Table 2, Table 3, and Table 4 respectively. Similar current and voltage rating MOSFETs were used in all of the tables for easy comparison between the tables to highlight the necessary tradeoffs. The selection tables provided a calculated estimate for the maximum peak gate current, I_g, maximum gate resistance value, R_g, and the expected gate drive system power dissipation, P_g, for three sets of PWM switching frequencies, $f_{(PWM)}$. These tables were created to assist the reader in his next SMPS project design challenge of ever increasing power density, greater efficiency, and lower cost without compromising product quality and reliability. Additional gate driver selection tables for all of the standard MOSFETs and the remainder of Q and F series will be provided on IXYS web site www.ixys.net.

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