26V Step-Up Converters for Two to Six White LEDs

DESCRIPTION

The EUP2561 is a constant current step-up converter specially designed for driving white LEDs. The step-up converter topology allows series connection of the white LEDs so the LED currents are identical for uniform brightness. The EUP2561 can drive 6 LEDs in series. The brightness of the LEDs can be adjusted through a voltage level on the CTRL pin or by applying a PWM signal to CRTL pin.

1MHz current-mode, pulse-width modulated (PWM) operation allows for small input and output capacitors and a small inductor while minimizing ripple on the input supply/battery. Programmable soft-start eliminates inrush current during startup.

The EUP2561 is available in a space-saving, 8-pin 3mm x 3mm DFN package.

FEATURES

- 2.6V to 5.5V Input Range
- 26V (max) Output with Overvoltage Protection
- Up to 87% Efficiency
- Flexible Analog or PWM Dimming Control
- Internal High Power 30V MOSFET Switch
- < 1μA shutdown Current
- Fast 1MHz PWM Operation
- Small, Low-Profile Inductors and Capacitors
- 3mm × 3mm DFN-8 Package
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- Cell Phones and Smart Phones
- PDAs, Palmtops, and Wireless Handhelds
- e-Books and Subnotebooks
- White LED Display Backlighting

Typical Application Circuit

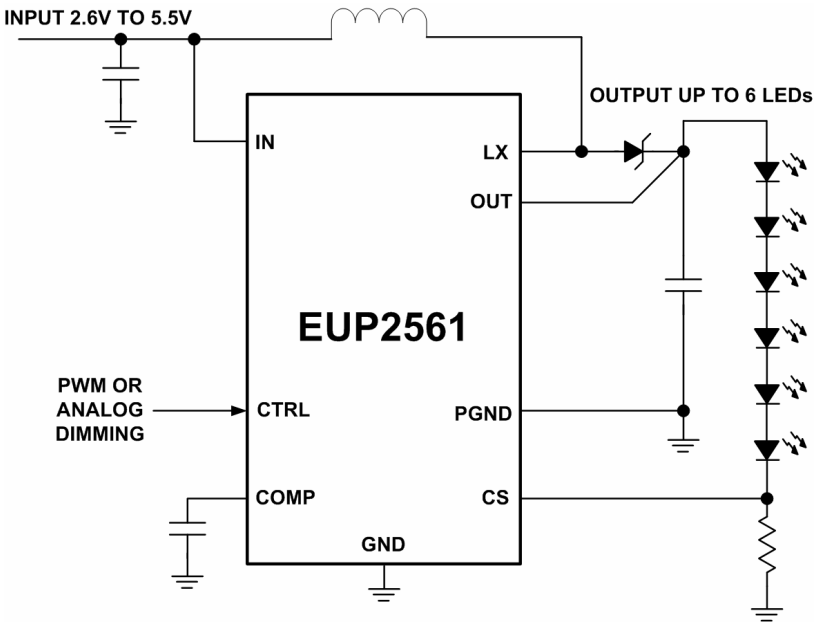
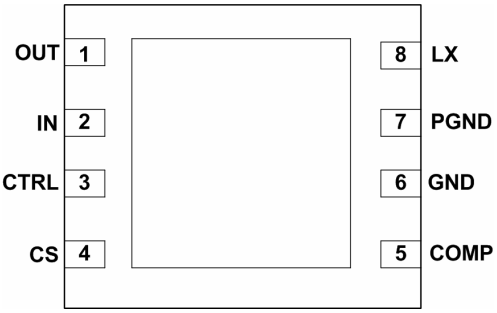


Figure 1. White LED Application

Pin Configurations

Part Number	Pin Configurations
EUP2561 DFN-8	

Pin Description

PIN	Pin	DESCRIPTION
OUT	1	Regulated Output Voltage.
IN	2	Input Supply Voltage.
CTRL	3	Brightness Control Input. LED brightness is controlled by the voltage applied to CTRL. Varying the voltage from 0.24V to 1.62V adjusts the brightness from dim to bright, respectively. Any voltage above 1.62V does not increase brightness.
CS	4	Current-Sense Feedback Input. Connect a resistor from CS to GND to set the LED bias current. The voltage at CS regulates to VCTRL / 10 or 0.162V, whichever is lower.
COMP	5	Compensation Input. Connect a 0.1μF capacitor (CCOMP) from COMP to GND. CCOMP stabilizes the converter and controls soft-start. CCOMP discharges to GND when in shutdown.
GND	6	Common Ground. Connect to PGND and the exposed pad directly under the IC.
PGND	7	Power Ground. Connect to GND and the exposed pad directly under the IC.
LX	8	Inductor Connection. This pin is high impedance during shutdown.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUP2561JIR1	DFN-8	xxxx 2561A	-40 °C to 125°C

EUP2561 □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
J: DFN-8

Block Diagram

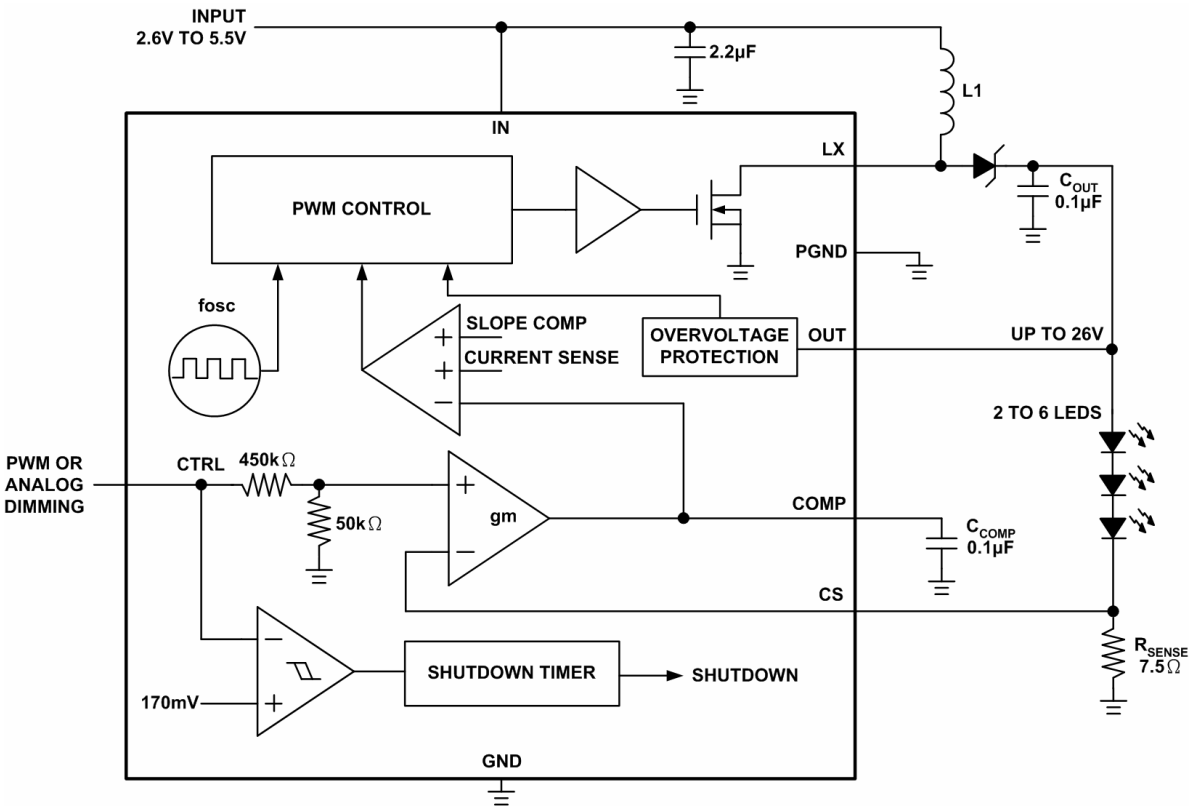


Figure 2.

Absolute Maximum Ratings

- IN to GND ---------- -0.3V to 6V
- PGND to GND ---------- -0.3V to 0.3V
- LX,OUT to GND ---------- -0.3V to 30V
- CTRL to GND ---------- -0.3V to the lower of 6V or (V_{IN} +0.5V)
- COMP,CS to GND ---------- -0.3V to (V_{IN} +0.3V)
- I_{LX} ---------- 1A
- Thermal Resistance
  DFN-8 ---------- 50°C /W
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- -65°C to 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- ESD Ratings
  Human Body Mode ---------- 2kV

Recommended Operating Conditions

- Supply Voltage, V_{IN} ---------- 2.6V to 5.5V
- Operating Temperature Rang ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 3V, V_{OUT} = 20V, C_{OUT} = 0.1µF, C_{COMP} = 0.15µF, R_{SENSE} = 7.5Ω, V_{CTRL} = 1.5V, Figure 2, **TA = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

Parameter	Conditions		EUP2561			Unit
			Min	Typ	Max.	
Supply Voltage			2.6		5.5	V
UVLO Threshold	V_{IN} rising or falling		2.10	2.38	2.55	V
UVLO Hysteresis				50		mV
Quiescent Current	No Switching			0.38	0.65	mA
Shutdown Supply Current	CTRL=GND, V_{OUT}=V_{IN}	T_A=25°C		0.3	2	µA
		T_A=85°C		1		
OVLO Threshold	V_{OUT} rising		26	27	29	V
OVLO Hysteresis				2		V
OUT Input Bias Current	V_{OUT}=26V,V_{CTRL}> 0.24V		10	20	30	µA
	V_{OUT}=V_{IN}, CTRL=GND			0.01	1	
Output Voltage Range			(V_{IN}-V_{D1})		25.5	V
ERROR AMPLIFIER						
CTRL to CS Regulation	V_{CTRL} = 1V, V_{IN}= 2.6V to 5.5V		0.095	0.100	0.105	V
CS Input Bias Current	V_{CS}=V_{CTRL}/10	T_A=25°C		0.01	1	µA
		T_A=85°C		0.03		
CTRL Input Resistance	V_{CTRL} ≤ 1.0V		290	500	860	kΩ
CTRL Dual-Mode Threshold			100	170	240	mV

Electrical Characteristics (continued)

(V_{IN} = 3V, V_{OUT} = 20V, C_{OUT} = 0.1µF, C_{COMP} = 0.15µF, R_{SENSE} = 7.5Ω, V_{CTRL} = 1.5V, Figure 2, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

Parameter	Conditions	EUP2561			Unit
		Min	Typ	Max.	
CTRL Dual-Mode Hysteresis			10		mV
CTRL Shutdown Enable Delay	(Note 2)	6.5	8.2	10.5	ms
CS-to-COMP Transconductance	V_{COMP} = 1.0V	32	50	82	µS

Electrical Characteristics

(V_{IN} = 3V, V_{OUT} = 20V, C_{OUT} = 0.1µF, C_{COMP} = 0.15µF, R_{SENSE} = 7.5Ω, V_{CTRL} = 1.5V, Figure 2, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

Parameter	Conditions		EUP2561			Unit
			Min	Typ	Max.	
OSCILLATOR						
Operating Frequency			0.80	1.0	1.25	MHz
Minimum Duty Cycle	PWM mode			12		%
	Pulse skipping			0		
Maximum Duty Cycle	CTRL=IN CS=GND		88	92		%
N-CHANNEL SWITCH						
LX On-Resistance	I_{LX}=190mA			1.38	2.25	Ω
LX Leakage Current	V_{LX}=28V, CTRL=GND	T_A=25°C		0.01	5	µA
		T_A=85°C		1		
LX Current Limit	Duty cycle=90%		450	700	950	mA

Note 1: VD1 is the diode forward-voltage drop of diode D1 in Figure 2.

Note 2: Time from CTRL going below the dual-mode threshold to IC shutdown.

Application Information

Soft-Start

The EUP2561 attain soft-start by charging C_{COMP} gradually with a current source. When V_{COMP} rises above 1.25V, the internal MOSFET begins switching at a reduced duty cycle. When V_{COMP} rises above 2.25V, the duty cycle is at its maximum. See the Typical Operating Characteristics for an example of soft-start operation.

Shutdown

The EUP2561 enter shutdown when V_{CTRL} is less than 100mV for more than 8.2ms. In shutdown, supply current is reduced to 0.3µA by powering down the entire IC except for the CTRL voltage-detection circuitry. C_{COMP} is discharged during shutdown, allowing the device to reinitiate soft-start when it is enabled. Although the internal N-channel MOSFET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown. However, with two or more LEDs, the forward voltage is large enough to keep leakage current low, less than 1µA(typ). Typical shutdown timing characteristics are shown in the Typical Operating Characteristics.

Overvoltage Protection

Overvoltage lockout (OVLO) occurs when V_{OUT} is above 27V.The protection circuitry stops the internal MOSFET from switching and causes V_{COMP} to decay to 0V. The device comes out of OVLO and into softstart when V_{OUT} falls below 25V.

Adjusting LED Current

Adjusting the EUP2561 output current changes the brightness of the LEDs. An analog input (CTRL) and the sense-resistor value set the output current. Output current is given by:

$$I_{LED} = \frac{V_{CTRL}}{10 \times R_{SENSE}}$$

The V_{CTRL} voltage range for adjusting output current is 0.24V to 1.62V. To set the maximum current, calculate RSENSE when V_{CTRL} is at its maximum as follows:

$$R_{SENSE} = \frac{1.62V}{10 \times I_{LED(MAX)}}$$

Power dissipation in RSENSE is typically less than 5mW, making a standard chip resistor sufficient.

PWM Dimming Control

CTRL is also used as a digital input allowing LED brightness control with a logic-level PWM signal applied directly to CTRL. The frequency range is from 200Hz to 200kHz, while 0% duty cycle corresponds to zero current and 100% duty cycle corresponds to full current. The error amplifier and compensation capacitor form a lowpass filter so PWM dimming results in DC current to the LEDs without the need for any additional RC filters; see the Typical Operating Characteristics.

Capacitor Selection

The exact values of input and output capacitors are not critical. The typical value for the input capacitor is 2.2µF and the typical value for the output capacitor is 0.1µF. Larger value capacitors can be used to reduce input and output ripple, but at the expense of size and higher cost. C_{COMP} stabilizes the converter and controlls soft-start. Connect a 0.1µF capacitor from COMP to GND. For stable operation, C_{OUT} must not exceed 10 times C_{COMP}.

Inductor Selection

Inductor values range from 10µH to 47µH. A 22µH inductor optimizes the efficiency for most applications while maintaining low $15mV_{P-P}$ input ripple. With input voltages near 5V, a larger value of inductance can be more efficient. To prevent core saturation, ensure that the inductor-saturation current rating exceeds the peak inductor current for the application. Calculate the peak inductor current with the following formula:

$$I_{PEAK} = \frac{V_{OUT(MAX)} \times I_{LED(MAX)}}{0.8 \times V_{IN(MIN)}} + \frac{VIN(MIN) \times 0.8\mu s}{2 \times L}$$

Schottky Diode Selection

The EUP2561 high switching frequency demands a high-speed rectification diode (D1) for optimum efficiency. A Schottky diode is recommended due to its fast recovery time and low forward-voltage drop. Ensure that the diode's average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed V_{OUT}. The RMS diode current can be calculated from:

$$I_{DIODE(RMS)} \cong \sqrt{I_{OUT} \times I_{PEAK}}$$

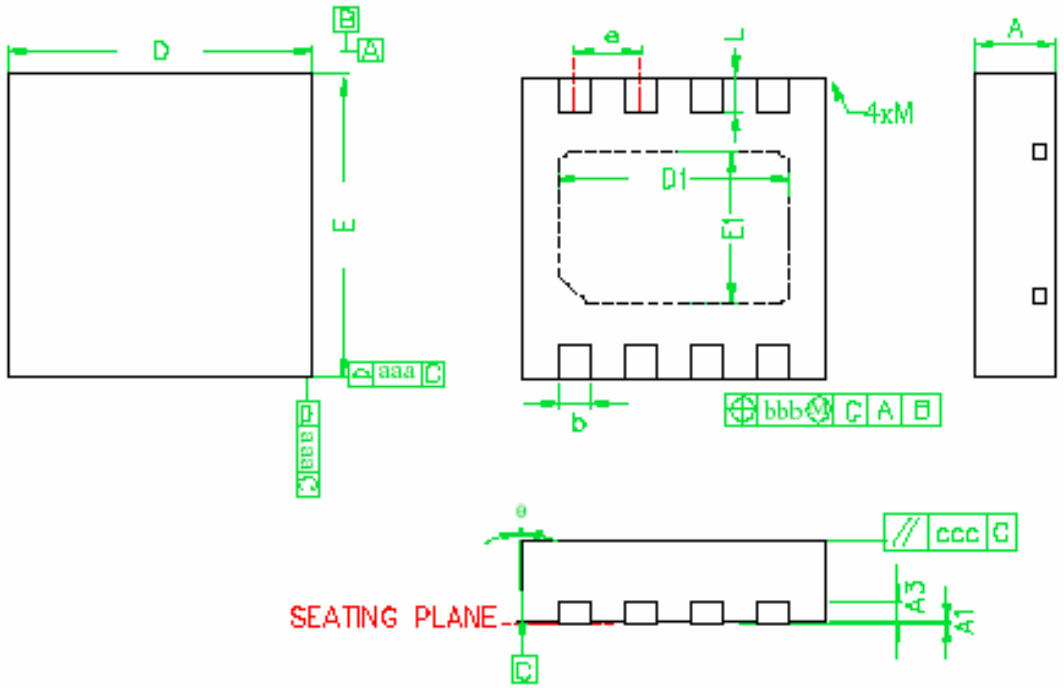
PC Board Layout

Due to fast switching waveforms and high-current paths, careful PC board layout is required. An evaluation kit is available to speed design.

When laying out a board, minimize trace lengths between the IC and R_{SENSE}, the inductor, the diode, the input capacitor, and the output capacitor. Keep traces short, direct, and wide. Keep noisy traces, such as the LX node trace, away from CS. The IN bypass capacitor (C_{IN}) should be placed as close to the IC as possible. PGND and GND should be connected directly to the exposed paddle underneath the IC. The ground connections of C_{IN} and C_{OUT} should be as close together as possible. The traces from IN to the inductor and from the Schottky diode to the LEDs may be longer.

Packaging Information

DFN-8



NOTE

1. All dimensions are in millimeters, θ is in degrees
2. M: The maximum allowable corner on the molded plastic body corner
3. Dimension D does not include mold protrusions or gate burrs. Mold protrusions and gate burrs shall not exceed 0.15mm per side
4. Dimension E does not include interterminal mold protrusions or terminal protrusions. Interminal mold protrusions and/or terminal protrusions shall not exceed 0.20mm per side
5. Dimension b applies to plated terminals. Dimension A1 is primarily Y terminal plating, but may or may not include a small protrusion of terminal below the bottom surface of the package
6. Burr shall not exceed 0.060mm
7. JEDEC MO-229

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.81	0.9	1.00
A1	0	0.015	0.03
A3	------	0.20 REF	------
B	0.25	0.30	0.37
D	2.85	3.00 BSC	3.15
D1	------	2.3 BSC	------
E	2.85	3.00 BSC	3.15
E1	------	1.5 BSC	------
e	------	0.65 BSC	-----
L	0.25	0.35	0.45
aaa	------	0.25	------
bbb	------	0.10	------
ccc	------	0.10	------
M	------	------	0.05
θ	-12	------	0