



偉詮電子股份有限公司
Weltrend Semiconductor, Inc.

WT7525
PC POWER SUPPLY SUPERVISOR
Data Sheet

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GENERAL DESCRIPTION

The WT7525 provides protection circuits, power good output (PGO), fault protection latch (FPOB), and a protection detector function (PSONB) control. It can minimize external components of switching power supply systems in personal computer.

The Over / Under Voltage Detector (OVD / UVD) monitors V33, V5, V12A and V12B input voltage level. The Over Current Detector (OCD) monitor IS33, IS5, IS12A and IS12B input current sense. When OVD or UVD or OCD detect the fault voltage level, the FPOB is latched HIGH and PGO go low. The latch can be reset by PSONB go HIGH. There is 2.4 ms delay time for PSONB turn off FPOB.

When OVD and UVD and OCD detect the right voltage level, the power good output (PGO) will be issue.

FEATURES

- The Over / Under Voltage Detector (OVD / UVD) monitors V33, V5, V12A and V12B input voltage level.
- The Over Current Detector (OCD) monitors IS33, IS5, IS12A and IS12B input current sense.
- Both of the power good output (PGO) and fault protection latch (FPOB) are Open Drain Output.
- 75 / 300 ms time delay for UVD.
- 300 ms time delay for PGO.
- 38 ms for PSONB input signal De-bounce.
- 73 us for internal signal De-glitches.
- 2.4 ms time delay for PSONB turn-off FPOB.

PIN ASSIGNMENT AND PACKAGE TYPE

Pin assignment

WT7525-140				WT7525-160				WT7525-161									
PGI	□	1	14	□	PGO	PGI	□	1	16	□	PGO	PGI	□	1	16	□	PGO
GND	□	2	13	□	VCC	GND	□	2	15	□	VCC	GND	□	2	15	□	VCC
FPOB	□	3	12	□	V5	FPOB	□	3	14	□	V5	FPOB	□	3	14	□	V5
PSONB	□	4	11	□	V33	PSONB	□	4	13	□	V33	PSONB	□	4	13	□	V33
IS12AB	□	5	10	□	V12A	IS12A	□	5	12	□	V12A	IS12A	□	5	12	□	VCC2
RI	□	6	9	□	IS33	RI	□	6	11	□	IS33	RI	□	6	11	□	V12A
V12B	□	7	8	□	IS5	NC	□	7	10	□	IS5	IS5	□	7	10	□	IS33
						V12B	□	8	9	□	IS12B	V12B	□	8	9	□	IS12B



ORDERING INFORMATION

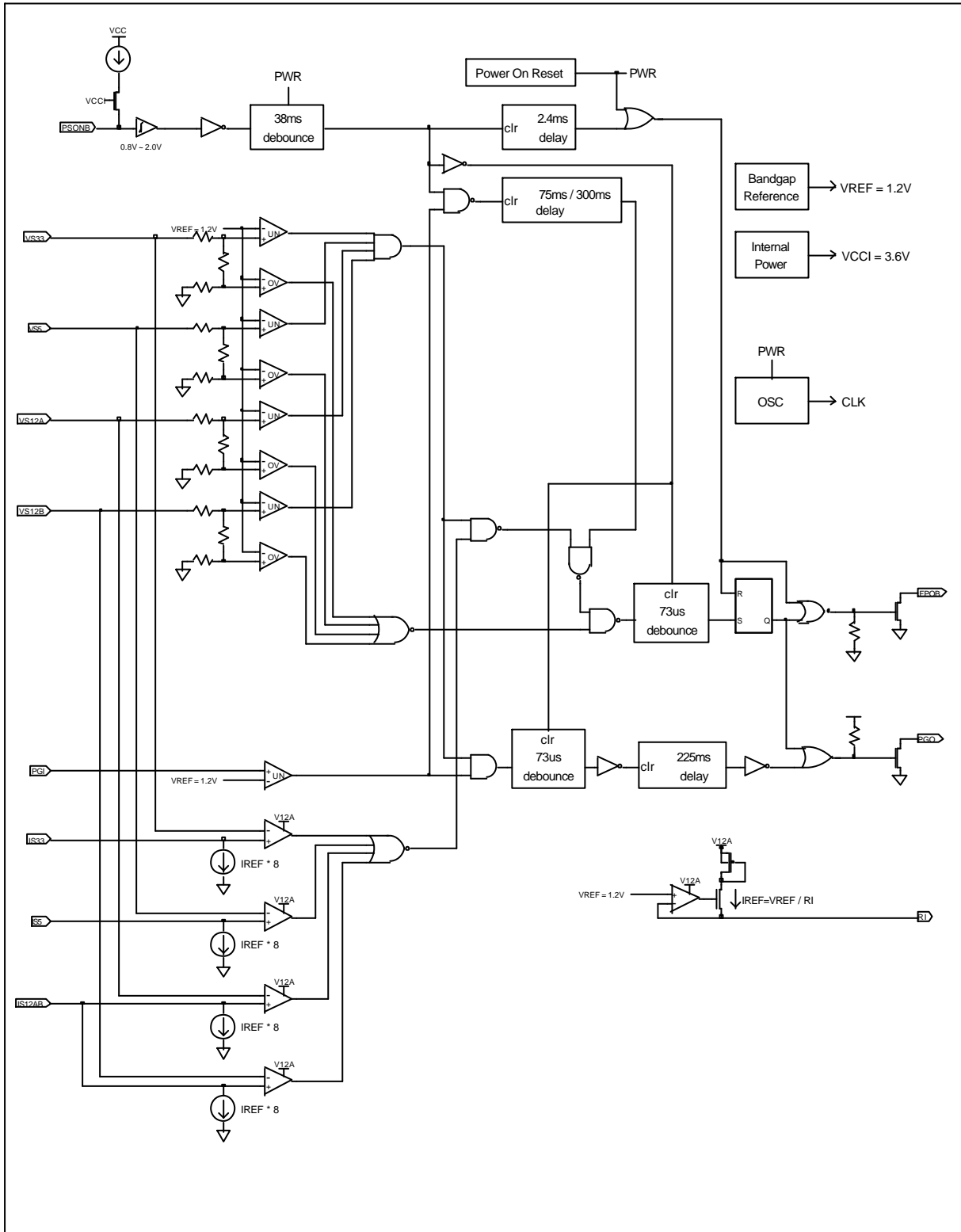
Package type	ORDERING INFORMATION
14-Pin Plastic DIP	WT7525N140
14-Pin Plastic SOP	WT7525S140
16-Pin Plastic DIP	WT7525N160
16-Pin Plastic SOP	WT7525S160
16-Pin Plastic DIP	WT7525N161
16-Pin Plastic SOP	WT7525S161

PIN DESCRIPTION

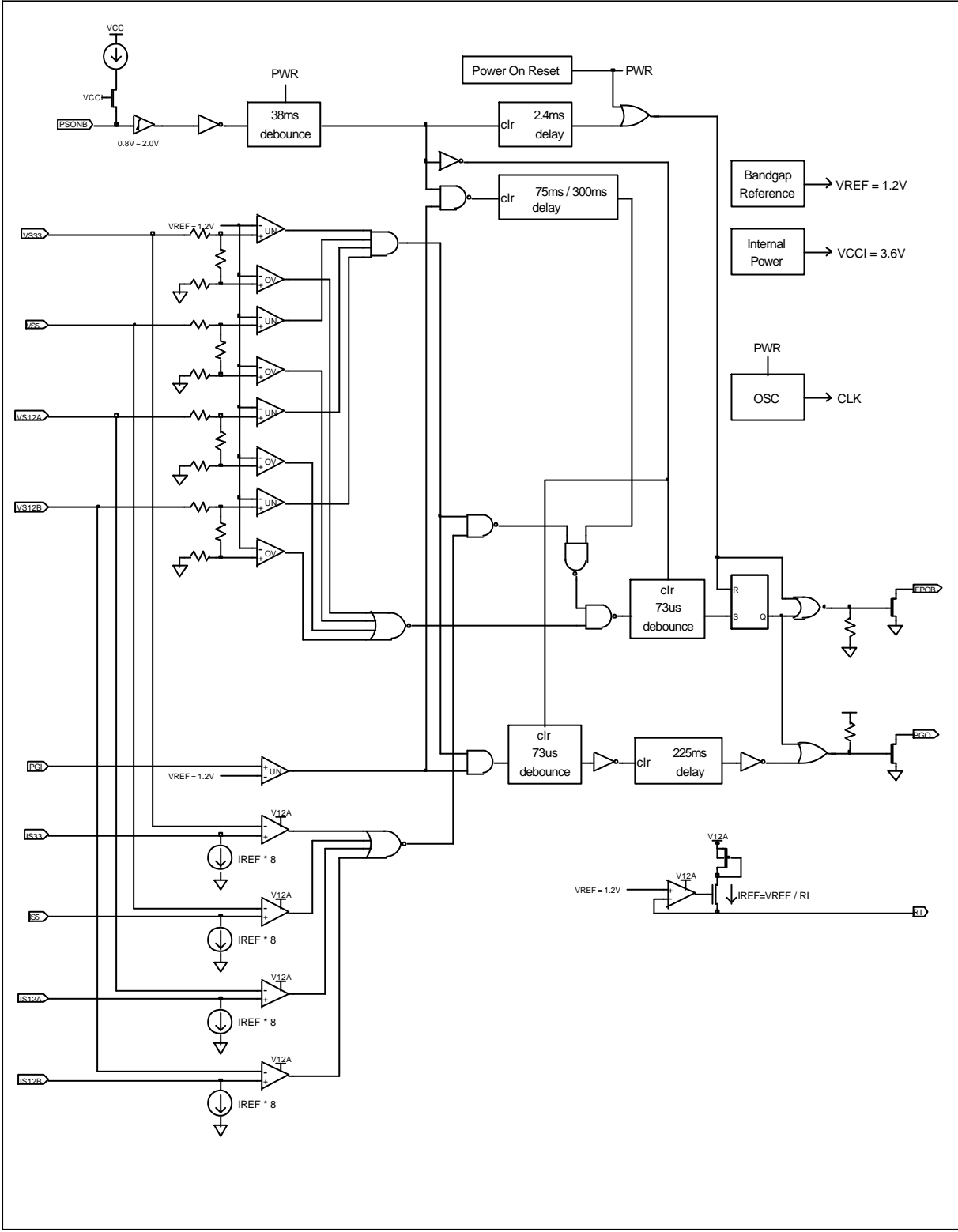
Pin Name	TYPE	Description
PGI	I	Power good input signal pin
GND	P	Ground
FPOB	O	Fault protection output pin, open drain output
PSONB	I	On/Off switch input
IS12A	I	12VA over current protection sense input
IS12AB	I	12VAB over current protection sense input
RI	I	Current sense adjust input
V12B	I	12VB over/under voltage input pin
IS12B	I	12VB over current protection sense input
IS5	I	5V over current protection sense input
IS33	I	3.3V over current protection sense input
V12A	I	12VA over/under voltage input pin
VCC2	I	Current sense power supply
V33	I	3.3V over/under voltage input pin
V5	I	5V over/under voltage input pin
VCC	I	Power supply
PGO	O	Power good output signal pin, open drain output

BLOCK DIAGRAM

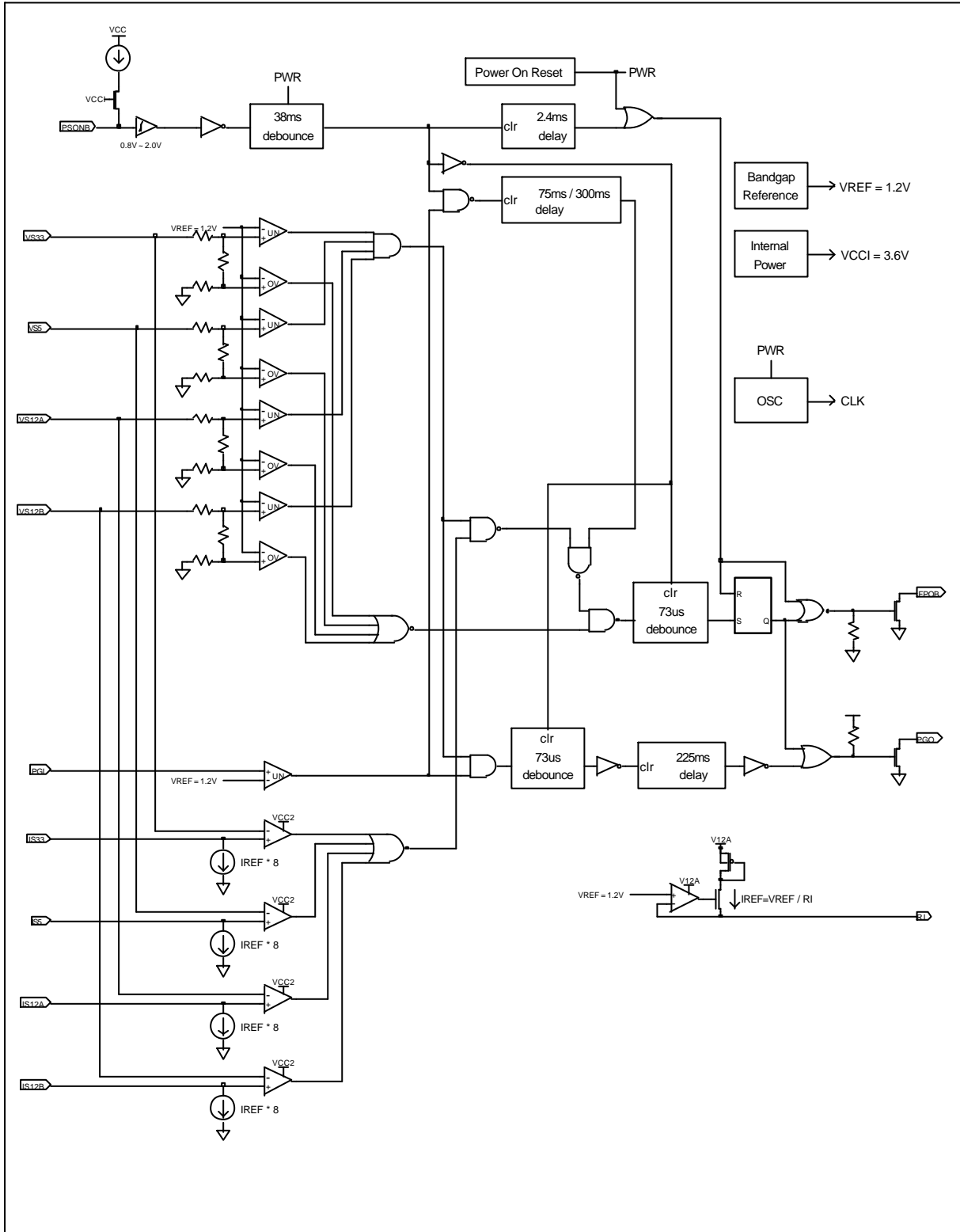
WT7525-140



WT7525-160



WT7525-161



ABSOLUTE MAXIMUM RATINGS

Parameter		Min.	Max.	Unit
Supply voltage, VCC, VCC2, V12A		-0.3	16	V
Input voltage	PGI	-0.3	VCC+0.3	V
	PSONB, V5, V33, I5, I33	-0.3	7	V
	V12B, I12AB	-0.3	16	V
Output voltage	FPOB, PGO	-0.3	7	V
Operating temperature		-40	125	
Storage temperature		-55	150	

*Note: Stresses above those listed may cause permanent damage to the devices

RECOMMENDED OPERATING CONDITIONS

Parameter		Conditions	Min.	Typ.	Max.	Unit
Supply voltage, VCC			4	12	15	V
Supply voltage, VCC2			9.5	12	15	V
Input voltage	PSONB, V5, V33, PGI				7	V
	V12A, V12B				15	V
Output voltage	FPOB, PGO				7	V
Output sink current	FPOB	0.7V			30	mA
	PGO	0.4V			10	mA
Supply voltage rising time			1			ms
Output current for RI	RI		10		65	uA

ELECTRICAL CHARACTERISTICS, at Ta=25°C and V_{CC}=5V.
Over Voltage Detection

Parameter		Condition	Min.	Typ.	Max.	Unit
Over voltage threshold	V33		3.7	3.9	4.1	V
	V5		5.7	6.1	6.5	V
	V12AB		13.3	13.8	14.3	V
I _{LEAKAGE}	Leakage current (FPOB)	V(FPOB) = 5V		5		uA
V _{OL}	Low level output voltage (FPOB)	I _{sink} = 10mA		0.3		V
		I _{sink} = 30mA		0.7		V

PGI and PGO

Parameter		Condition	Min.	Typ.	Max.	Unit
Under voltage threshold	V33		2.55	2.69	2.83	V
	V5		4.1	4.3	4.47	V
	V12AB		9.5	10	10.5	V
Input threshold voltage(PGI)			1.16	1.20	1.24	V
I _{LEAKAGE}	Leakage current(PGO)	PGO = 5V		5		uA
V _{OL}	Low level output voltage(PGO)	I _{sink} = 10mA		0.4		V

PSONB

Parameter		Condition	Min.	Typ.	Max.	Unit
Input pull-up current		PSONB= 0V		150		uA
High-level input voltage			2.0			V
Low-level input voltage					0.8	V

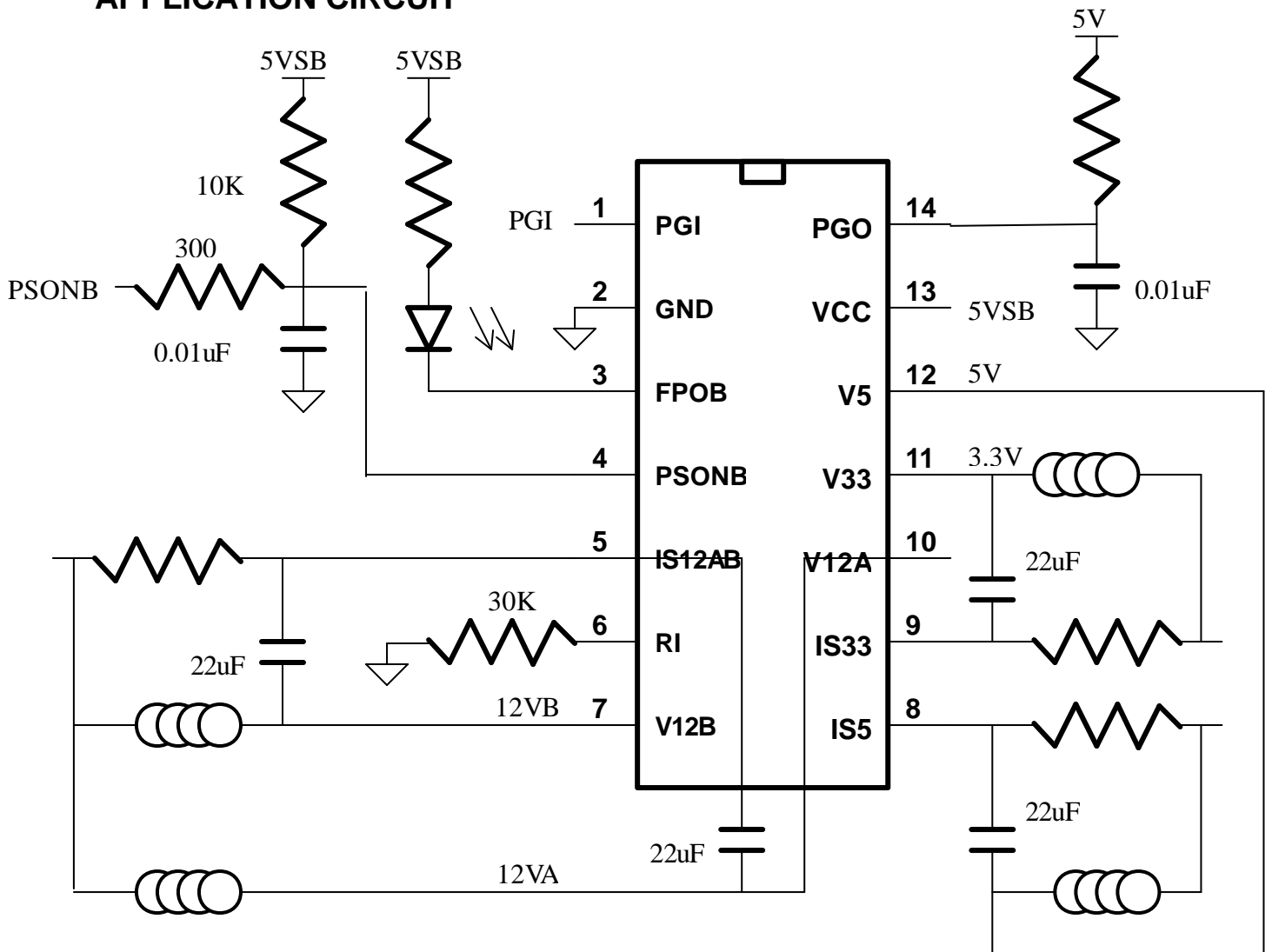
TOTAL DEVICE

Parameter	Condition	Min.	Typ.	Max.	Unit
I _{cc} Supply current	PDON_N= 5V			1	mA
V _{cc} low voltage			3		V

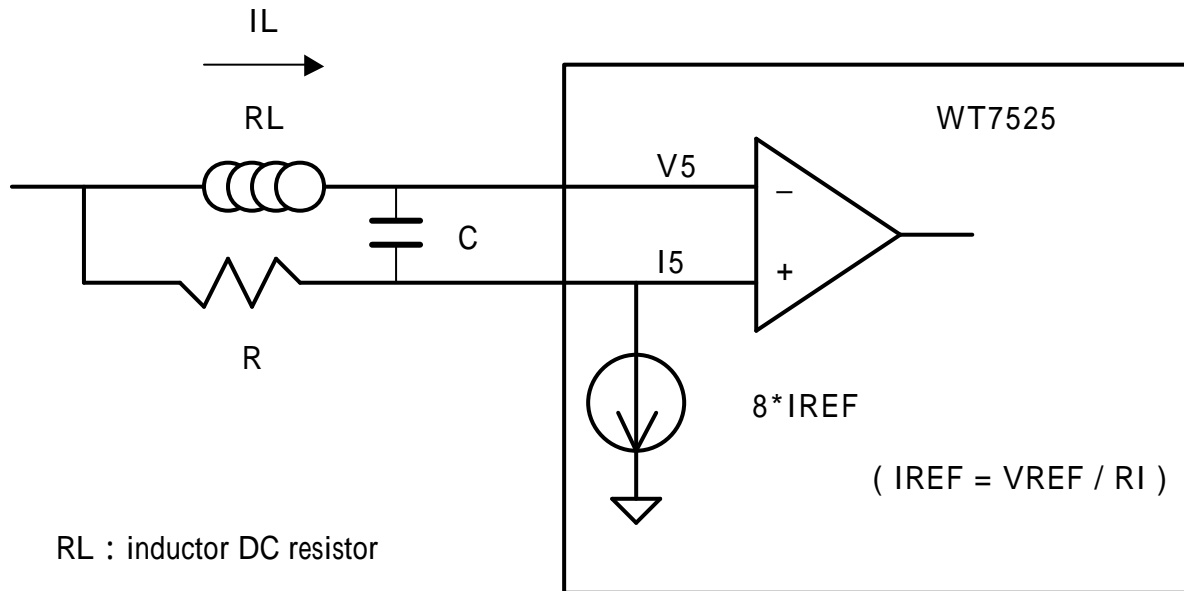
SWITCHING CHARACTERISTICS, V_{cc}=5V

Parameter	Condition	Min.	Typ.	Max.	Unit
t _{db1} De-bounce time (PSONB)		32	38	61	mS
t _{dleay1} Delay time (PGI to PGO)		200	300	490	mS
t _{db2} De-bounce time (PSONB)		32	38	61	mS
t _q De-glitch time		63	73	120	uS
t _{delay2} PSONB to FPOB delay time		t _{db2} +2.0	t _{db2} +2.4	t _{db2} +3.8	mS
t _{delay3} Internal UVD/OCD delay time	after FPOB go low & PGI > 1.2V	65	75	122	mS
	after FPOB go low & PGI < 1.2V	260	300	488	mS

APPLICATION CIRCUIT



APPLICATION NOTE



If $I_L * R_L > (8 * I_{REF}) * R$, then OCP active.

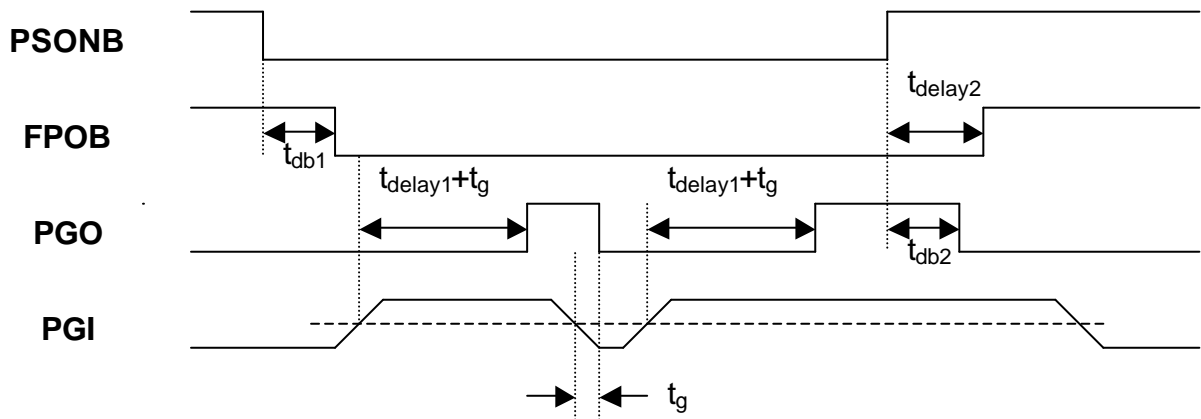
And the capacitor C is used to avoid power on fail or dynamic load fail. We suggest $C > 1\mu F$.

EX : How to select the resistor of R? Assume $R_I=30K$, $R_L=3m$, $OCP=20A$.

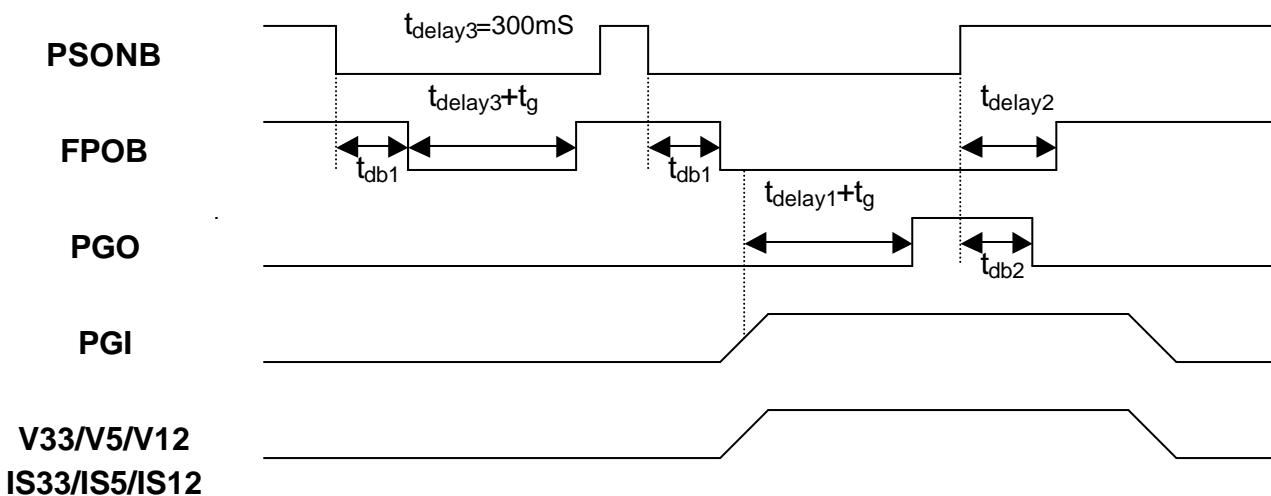
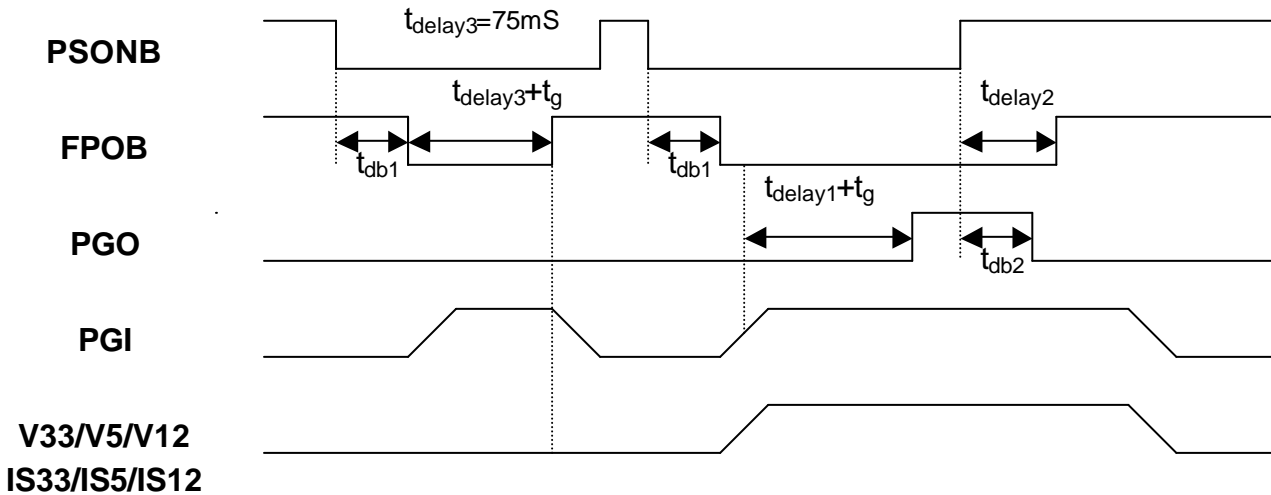
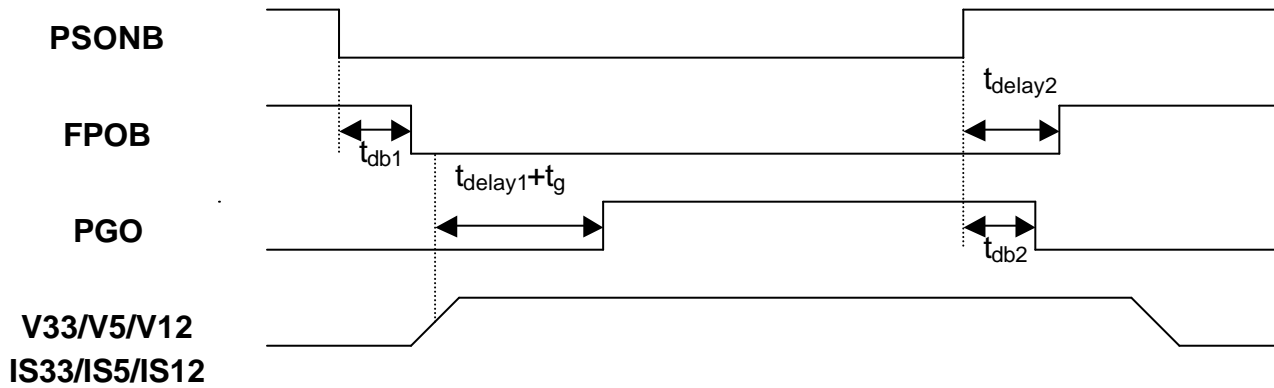
$$\begin{aligned}
 \text{Sol : } R &= (I_L * R_L) / (8 * I_{REF}) \\
 &= (20A * 3m) / \{ 8 * (1.2V / 30K) \} \\
 &= 187.5
 \end{aligned}$$

APPLICATION TIMMING

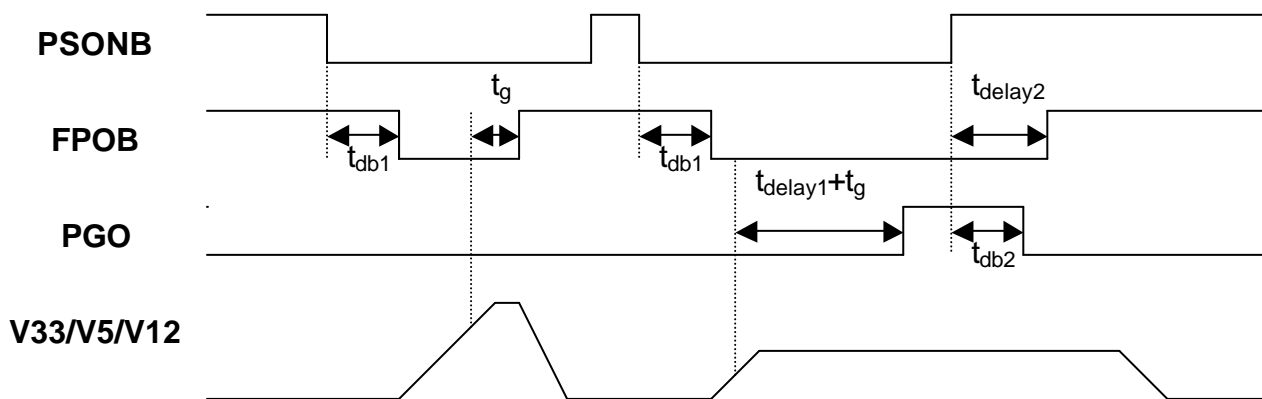
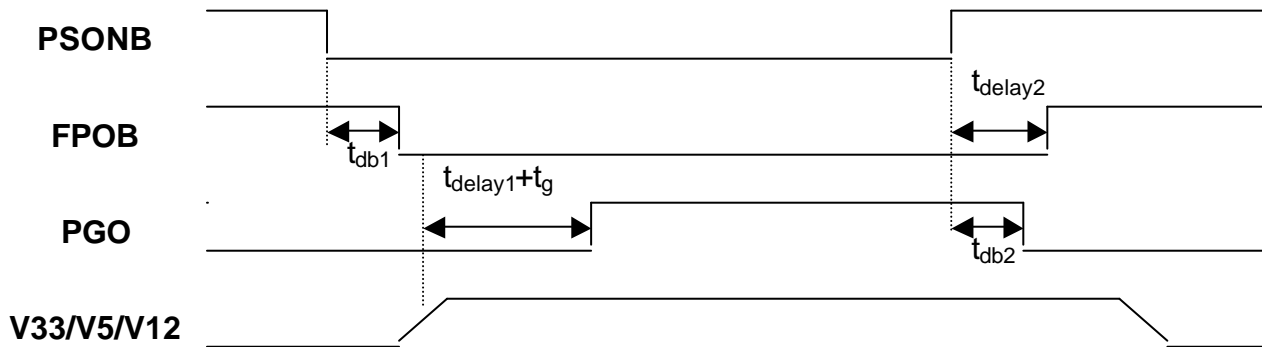
1.) PGI (UNDER_VOLTAGE) :



2.) V33, V5, V12 (UNDER_VOLTAGE) or IS33 , IS5 , IS12 (OVER_CURRENT) :

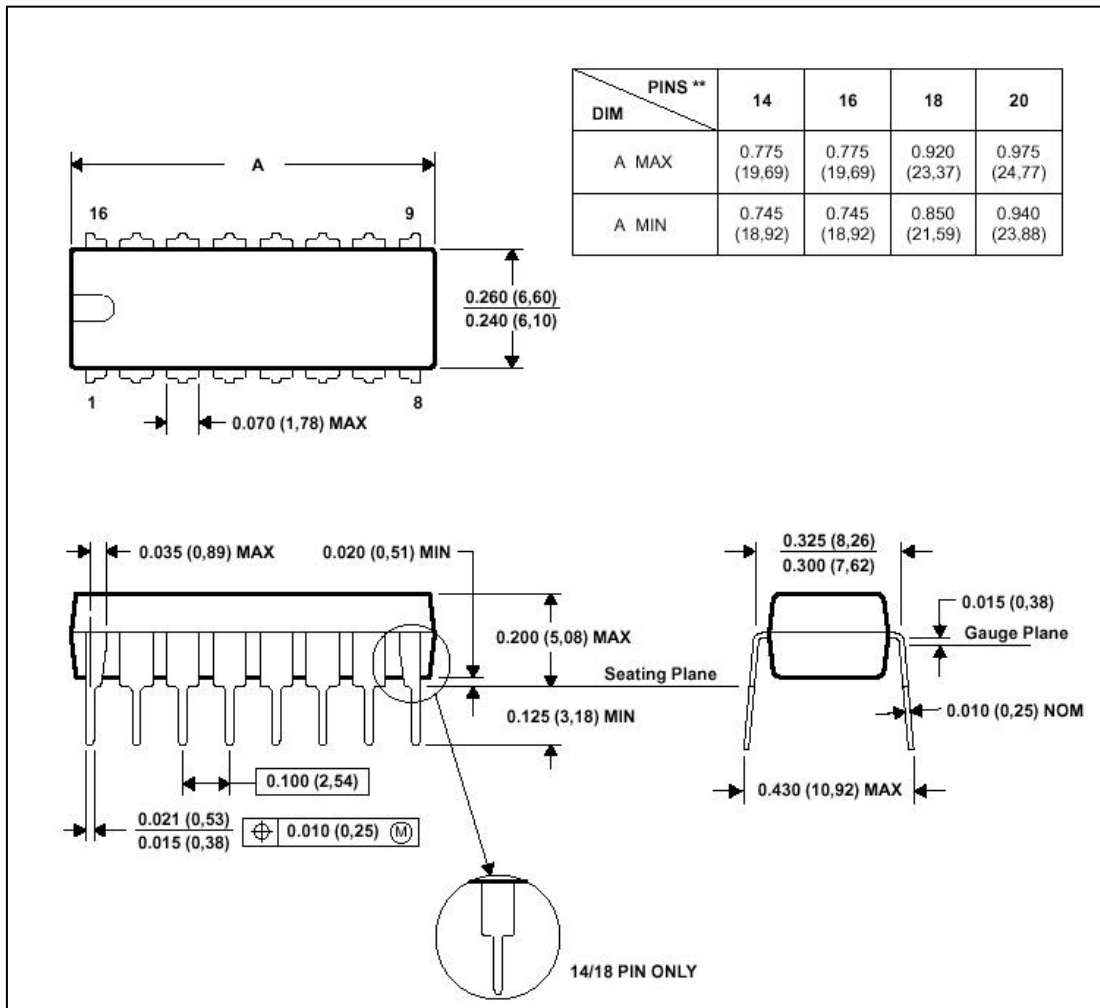


3.) V33, V5, V12 (OVER_VOLTAGE) :



MECHANICAL INFORMATION

PLASTIC DUAL-IN-LINE PACKAGE

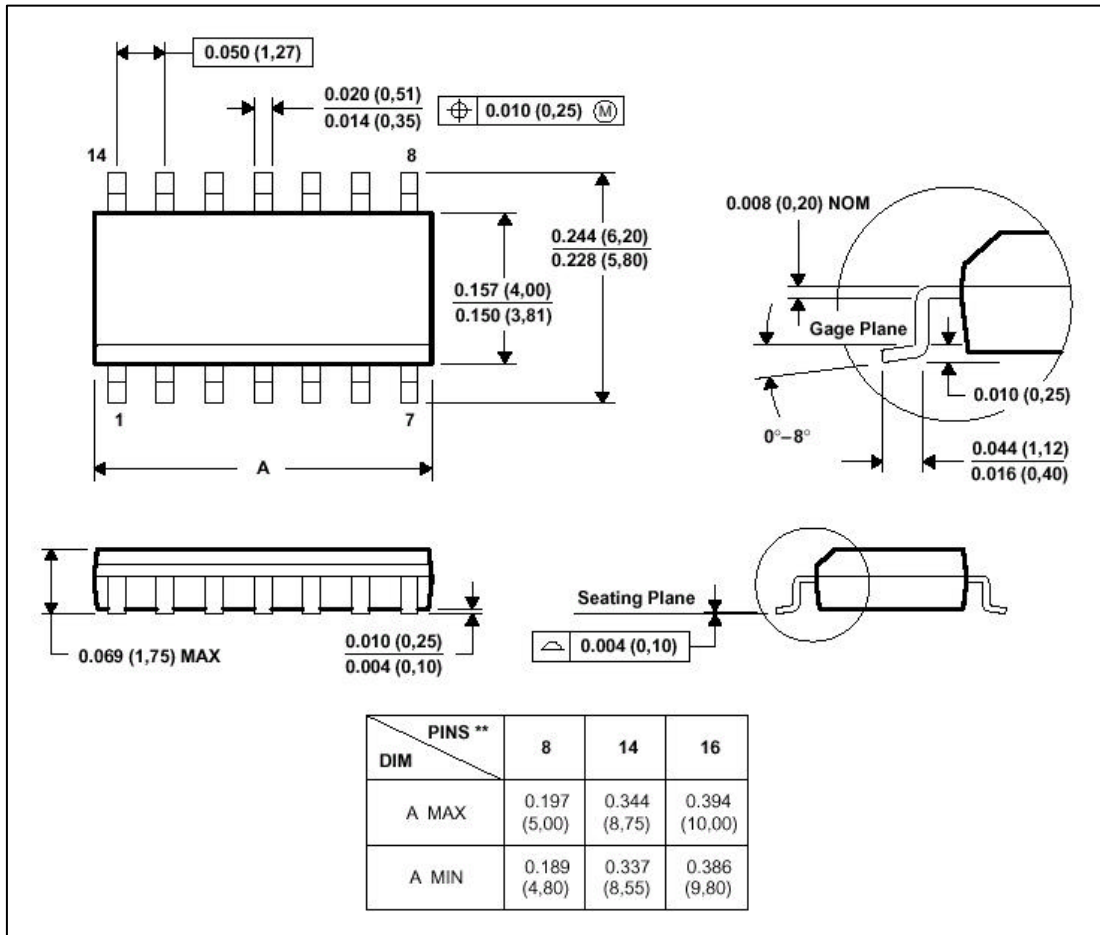


NOTE 1 : All linear dimensions are in inches (millimeters) .

NOTE 2 : This drawing is subject to change without notice.

NOTE 3 : Falls within JEDEC MS-001

PLASTIC SMALL-OUTLINE PACKAGE



NOTE 1 : All linear dimensions are in inches (millimeters) .

NOTE 2 : This drawing is subject to change without notice.

NOTE 3 : Falls within JEDEC MS-012