Sequencing Power Supplies in Multiple Voltage Rail Environments

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ABSTRACT

Designers must consider timing and voltage differences during power up and power down in systems where multiple power rails are involved. A simple example would be a single DSP with its core and I/O voltages, requiring power supply sequencing. The possibility for a latch-up failure or excessive current draw exists when power supply sequencing is not designed properly. The trigger for latch-up may occur if power supplies are applied at different potentials of the core and I/O interfaces. This paper addresses some of the more common sequencing requirements of digital signal processing (DSPs), field programmable gate arrays (FPGAs), application-specific integrated circuits (ASICs) and microprocessors, and proposes a variety of practical solutions implemented with power management devices. These techniques take advantage of the reset, power good, enable and soft-start features available on many types of power management devices ranging from low drop out (LDO) regulators to plug-in power modules.

I. INTRODUCTION

High-performance signal processing devices, such as FPGAs, ASICs, PLDs and DSPs require multiple power supplies that generate different voltages for the core and I/O voltages. The order in which these voltages power up and power down can prove critical to device operation and long term reliability. This paper addresses some of the reasons devices require the different types of power supply sequencing and offers examples of practical supply sequencing solutions.

II. WHY SEQUENCE POWER SUPPLIES?

Designing a system without proper power supply sequencing may introduce potential risks, including compromised reliability and immediate faults. Long term reliability is sacrificed when an out-of-bounds condition persists on a multi-supply device for extended periods of time. The risk comes when there is an active power supply rail and an inactive supply on a device for long time periods. This condition can stress electrostatic discharge (ESD) protection and other internal circuits that interface between the different voltages. The amount of time the device can be stressed before potential damage occurs under these conditions may be measured in months, but it is the cumulative exposure to these conditions that determines the usable life of the product. While a few poorly controlled power-up and power-down cycles are unlikely to damage a device, a system that is power cycled time after time without proper power supply sequencing can eventually fall victim to this failure mode.

Another risk of improper power supply sequencing in a system can cause immediate damage to a device. This failure is often a result of excessive current flow into a pin or excessive voltage differential across pins that stress internal components. The causes of these immediate failures are similar to those of the reliability failures. The difference is how the device is affected by the stresses.

A. Latch-Up

Since most multi-supply devices are fabricated in CMOS technology, the devices are susceptible to an electrical failure mode called latch-up. Latch-up can occur when voltage and current levels beyond the normal operating level stress pins of a powered device. When latch-up occurs, the device draws unusually high supply current which may render the device inoperable and/or cause permanent damage to the device.

Fig. 1 depicts a cross section of a CMOS inverter with the parasitic bipolar transistors overlaying the illustration.[1][2] The source of the N-channel MOS device serves as emitter, the N-well as collector, and substrate as base of the parasitic bipolar NPN transistor. Similarly, the source of the P-channel MOS device serves as emitter, the N-well as base, and the substrate as collector of the parasitic bipolar PNP. These parasitic bipolar transistors comprise a PNPN structure commonly known as a silicon-controlled rectifier (SCR). The PN junctions of the parasitic transistors are normally reverse-biased. However, a PN junction of the parasitic SCR may become forward-biased due to electrical disturbances resulting in SCR conduction which may result in device failure. Among electrical disturbances which may cause latch-up are voltages on pins beyond the supply voltage rails, large DC currents in the substrate or N-well, and displacement currents in the substrate or N-well resulting from fast-transitioning internal nodes.

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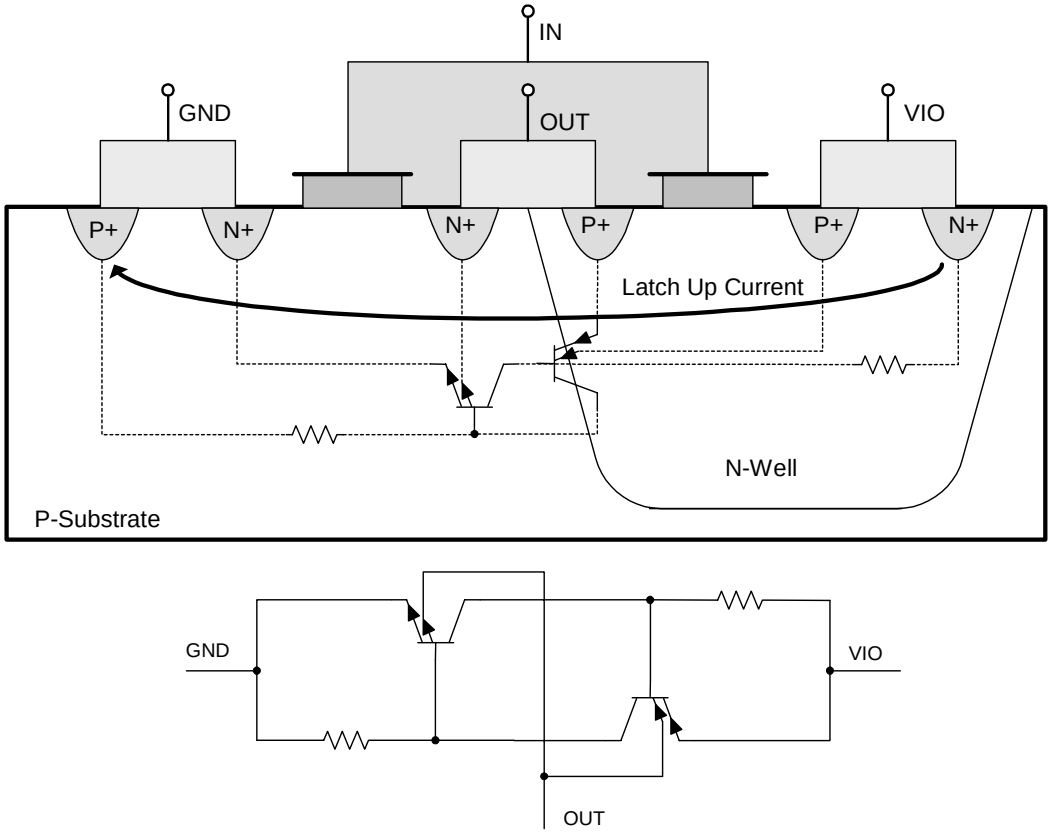


Fig. 1. Cross-section of CMOS inverter.

Fig. 2 represents the architecture of a multi-voltage device, such as a programmable logic device (PLD), interfacing to an external driver.[3] To illustrate some of the problems with sequencing power supplies, the system consists of three power supplies: V_{CORE}, V_{IO}, and V_{EXT} at 5 V, 3.3 V and 3.3 V, respectively.

Consider the following scenario: V_{IO} supply is active, V_{CORE} is inactive, and the driver input is not initialized. Since the driver is not in a known state, Q1 could be biased on, sourcing current through ESD diode D1. The magnitude of the current depends on the impedance of Q1, D1 and the inactive supply. Latch-up may occur as current flows through the ESD diode when the core supply ramps up. Whether this current causes a catastrophic latch-up failure, latent reliability issue, or neither, depends on robustness of the device design. In other words, damage may not occur if magnitude of the current is sufficiently low that the silicon can conduct the current without compromising reliability.

A potential latch-up issue arises when peripheral devices, such as data converters and memory, are coupled to the I/O pins of a multi-supply device and powered from a different supply that is ramping. Fig. 2 shows an external driver coupled to the I/O pin that has a "sneak path" through the anti-parallel body diode of Q3 when the V_{EXT} pin voltage is lower than V_{IO}. This issue can easily be resolved by connecting the V_{EXT} and V_{IO} pins to the same power supply. When V_{EXT} is active and the external driver sources current into the pin when V_{CORE} or V_{IO} is ramping, the potential for latch-up in the multi-supply device exists.

Trends in the semiconductor industry include increasing device speed, including more features, reducing power consumption, and reducing device size, all the while shortening product development cycle times. To meet these goals, design teams pack more components into a smaller area by using smaller device geometries, thinner well structures, and lighter substrate and well concentrations. Unfortunately, these design techniques increase the ohmic resistance and gain (or "beta") of the parasitic PNP and NPN transistors which, in turn, increases the likelihood of latch-up. Design techniques to prevent latch-up include using protection circuits and "guard rings". Protection circuits are used on input and output pads to safely shunt current and guard rings are used around wells to provide low-resistance. Both these prevention techniques come at the penalty of device size and cost.

The device's core voltage, susceptibility to latch-up, and supply sequencing order are, all too often, determined after pre-production silicon is available and device characterization and qualification are performed. With the emphasis on meeting cost and customer timetables for the latest product, if only minor issues are found with a device (such as a preference for supply sequencing), the issues are documented and the device released to market.

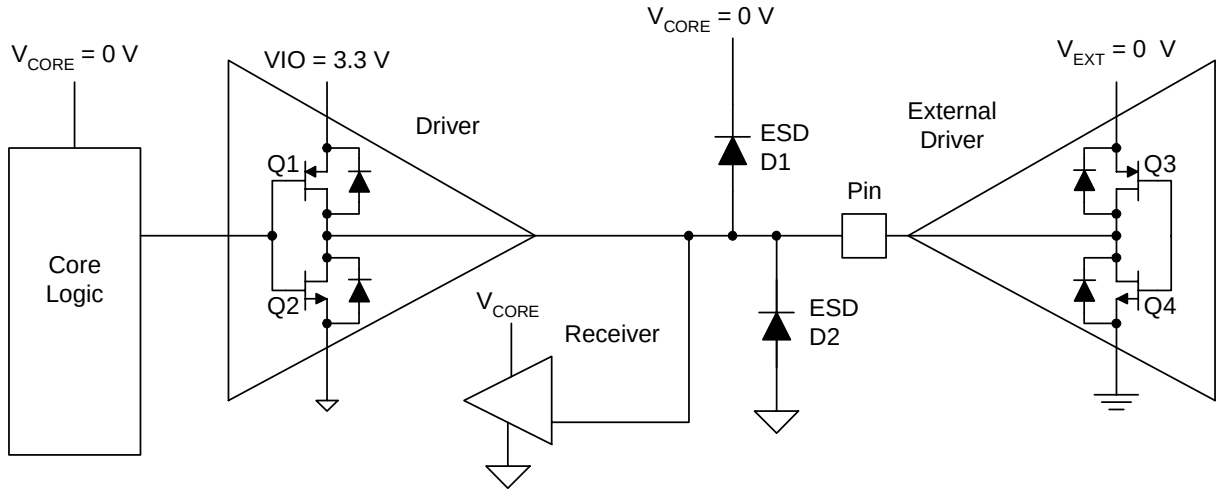


Fig. 2. Close-up of a multi-voltage device.

B. System-Level Bus Contention

Power supply sequencing may be required to prevent system-level bus contention, in which the bidirectional I/O pins of a DSP and external peripheral device oppose each other. Since the bus control logic originates in the core section of the DSP, powering I/O prior to the core may result in both the DSP and peripheral simultaneously configured as outputs. If the data values on each side are opposing, then the output drivers contend for control, as shown in Fig. 3.

Excessive current flows in one of the paths shown, depending on the opposing data-out patterns. The outputs contend for control and excessive current flows when the data values are opposing. This excessive current may damage the bidirectional I/O ports. Following the recommendation to power the core at the same time or before the I/O prevents undefined logic states on the bus control signals. [4]

III. SEQUENCING SCHEMES

There are three distinct schemes to power-up and power-down multi-rail power supplies: sequential, ratio-metric, and simultaneous [5]. The appropriate sequencing scheme is dependent on device requirements. The manufacturer's data sheet does not explicitly name which power sequencing scheme to implement, but rather outlines voltage and timing conditions that cannot be exceeded on power supply pins. Note that some devices allow out-of-bounds conditions for a short period of time. Using the pin conditions and the waveforms in the following section, a sequencing methodology can be chosen to meet the processor requirements.

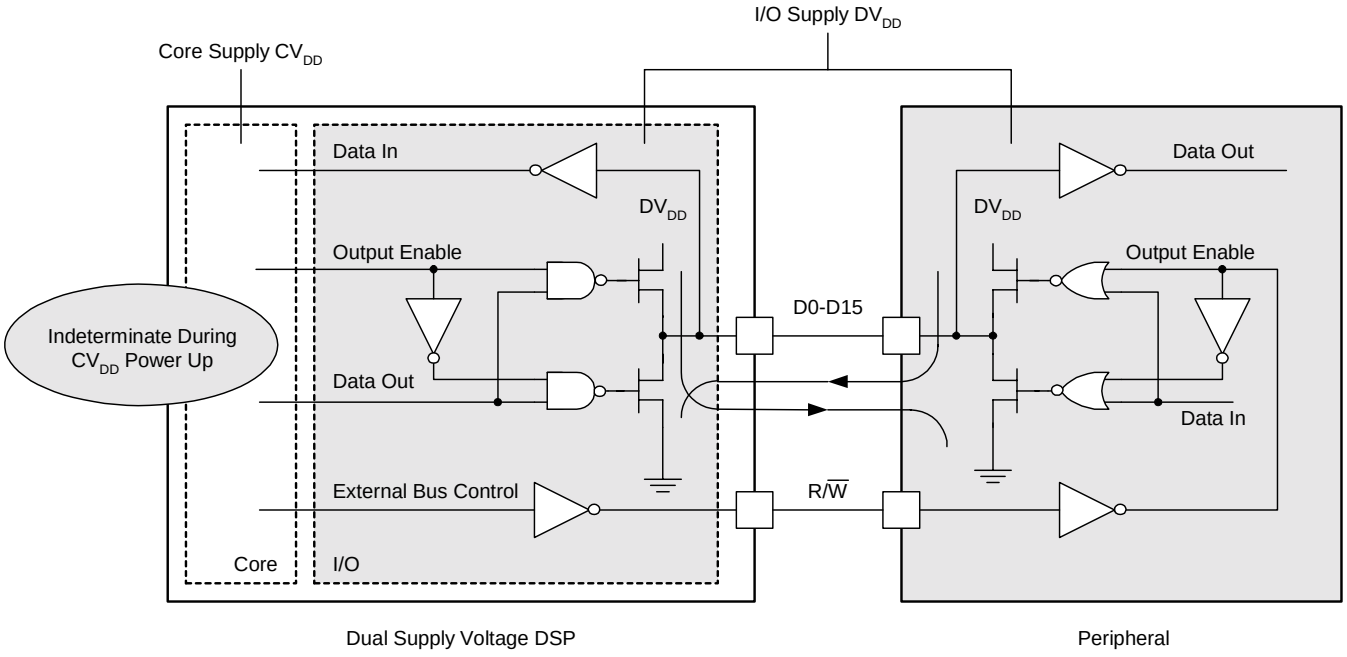


Fig. 3. System-level bus contention.

A. Sequential Sequencing

The sequential scheme of power supply sequencing is best described as one power supply ramping and settling to its final regulation voltage and then the second power supply ramping after a time delay. This method is used to initialize certain circuitry to a known state before activating another supply rail. An example applying the core supply rail prior to the I/O supply starting is shown in Fig. 4a.

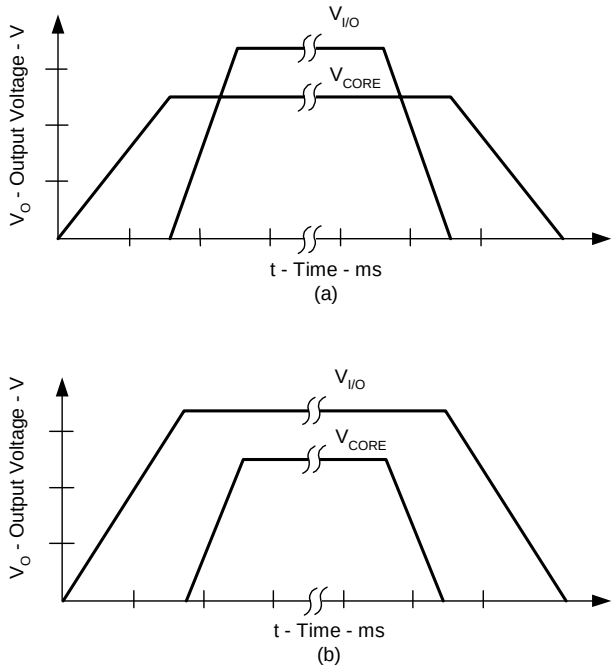


Fig. 4. Sequential sequencing schemes.

The following is an excerpt from a footnote in a device specification with recommendations best suited to using sequential power supply sequencing:

"System-level concerns such as bus contention may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as or prior to the I/O buffers and then powered down after the I/O buffers." [6]

An alternative power supply sequence order would call for the I/O supply to power up first and the core supply to start after the I/O power supply reaches regulation, see Fig. 4b. In the particular example [7], this method meets the recommended power sequencing for the device as long as the delay time for the start up of the core supply is less than 100 ms. As presented later in this topic, a typical hardware implementation employs an output voltage monitor to develop a power good (PG) signal for the first power supply, which then connects to the enable (EN) function of the second power supply.

B. Ratio-Metric Sequencing

For a dual power supply implementing ratio-metric sequencing, both power supply outputs ramp at the same time *and in proportion* until regulation is reached. Fig. 5a illustrates ratio-metric power sequencing where the core and I/O supply reach regulation at approximately the same instant. During power-up the core supply is a percentage of the I/O supply until regulation is reached. Similarly, during power-down the core is a specific percentage of the I/O supply voltage. Another example of ratio-metric sequencing may find the core supply voltage slightly greater than the I/O supply during the power-up and down, see Fig. 5b. In this particular case, to ensure the I/O buffers have valid inputs, the core rail is powered slightly before the I/O rail to eliminate problems with bus contention. [8]

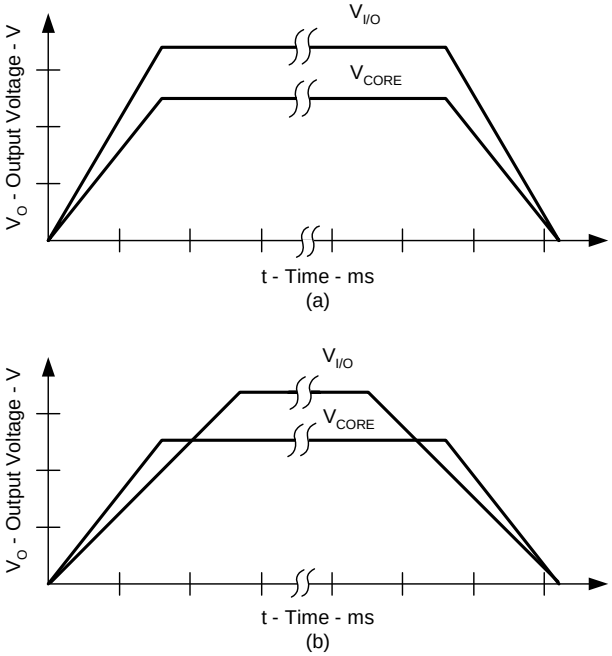


Fig. 5. Ratio-metric sequencing.

C. Simultaneous Sequencing

The simultaneous power sequencing method is similar to ratio-metric sequencing in that both power supply outputs ramp at the same time. However, in simultaneous sequencing, the objective is to minimize the voltage difference between the two supply rails during power up and down, as shown in Fig. 6, until regulation is reached for the core supply. This sequencing method is useful for devices that have "sneak paths" between supply pins or draw excessive current during startup if internal logic has not transitioned to a stable state. Reference [9] recommends simultaneous sequencing to minimize transient start-up currents.

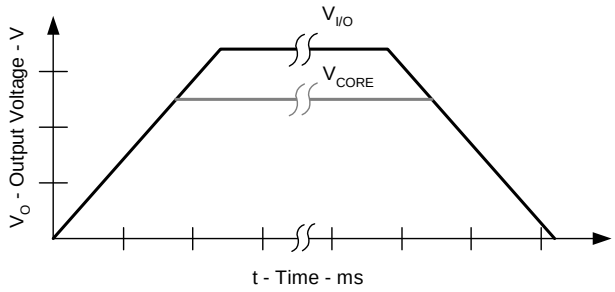


Fig. 6. Simultaneous sequencing.

The following sections show many examples of power sequencing implemented with:

- Diodes
- Low-dropout (LDO) linear regulators
- Supply voltage supervisors (SVS)
- Power distribution switches
- Hot-swap controllers
- Microcontrollers
- Switch-mode controllers (power FETs external)
- Switch-mode converters (power FETs internal)
- Plug-in power modules

IV. Sequencing Implementations Illustrated with LDOs

A. Diodes

Diodes are often used to facilitate sequencing requirements. Though diodes alone cannot achieve true sequential, ratio-metric or simultaneous sequencing, they can help maintain proper relation between various supply voltages.

Fig. 7 illustrates use of a Schottky diode to limit voltage differential between the core and I/O rail. The Schottky diode further reduces potential stress on devices by bootstrapping the I/O supply and shortening the delay between supply ramps. [5]

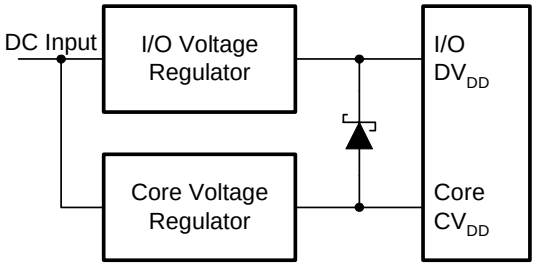


Fig. 7. Schottky diode limits voltage differential.

Fig. 8 shows rectifiers in combination to help meet these microprocessor requirements:

- *"V_{IN} must not exceed V_{DDH} by more than 2.5 V at any time, including during power-on reset.*
- *V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 1.6 V at any time, including during power-on reset.*
- *V_{DD}/V_{CCSYN} must not exceed V_{DDH} by more than 0.4 V at any time, including during power-on reset."* [17]

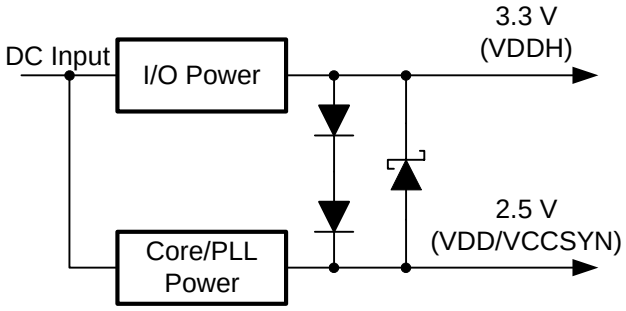


Fig. 8. Combination of diodes limits voltage differential.

"Note: There are internal diodes connected serially between VDDH and VDD, and vice-versa for ESD protection. If one of the voltages (VDD or VDDH) is applied and the other power pins are not driven, then the internal diodes pull up these pins. However, a problem could occur if one of the voltages (VDD or VDDH) is applied and the other voltage is forced to GND. In this case, the ESD diodes might be destroyed." [17]

To achieve *true* sequential, ratio-metric or simultaneous sequencing, enlist the capabilities of a wide range of active devices, as discussed in the following sections.

B. LDO Enable Via Supply Voltage Supervisor (SVS)

Sequential Sequencing

Fig. 9 shows an implementation of a supply voltage supervisor (SVS) to realize a sequential sequencing scenario. The load of this power supply is an FPGA which requires sequential sequencing. The power solution shown employs a 5-V input supply voltage rail. The core voltage is powered up first and, once the core voltage has ramped, the I/O voltage rail is enabled. Advantages of a linear regulator over a switch-mode approach typically include lower noise, reduced board space and cost. A key disadvantage is lower efficiency and, as a result, increased power dissipation.

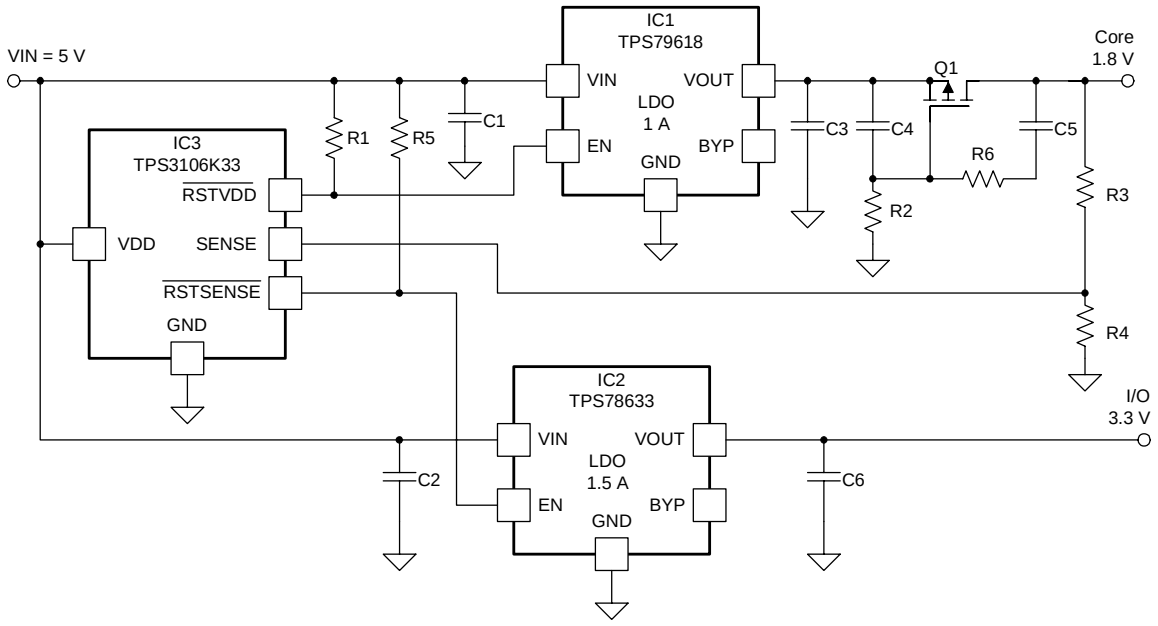


Fig. 9. Sequential sequencing using SVS.

This solution is based on two LDOs, IC1 to supply core voltage and IC2 for the I/O voltage rail, along with an SVS, IC3. The dual SVS, with trip point threshold voltage of 2.941 V (typical), monitors the input voltage rail. Once the input voltage rail has reached the threshold of 2.941 V, the SVS reset output transitions from low to high impedance state after a delay of 130 ms, enabling LDO IC1. Once LDO IC1 is enabled, the core voltage ramps up towards its final value of 1.8 V. To ensure that the input voltage rail does not drop due to the high inrush current demand of the capacitor bank and the FPGA, a current-limiting circuit has been implemented. Without this current-limit circuit, the input voltage could potentially droop during the switch-on cycle. This current-limit circuitry, consisting of Q1, C4, R2, R6 and C5, provides smooth charging of the load during power-up.

Core voltage is monitored via a comparator incorporated in SVS IC3. Voltage divider R3 and R4 adjusts the threshold voltage to the particular needs of the application. In this case, it has been adjusted to a threshold voltage of 1.7 V. Once the core voltage reaches the threshold voltage, IC3 enables LDO IC2, which provides the I/O voltage to the system, and the I/O voltage ramps to its final value of 3.3 V.

The power-up and power-down waveforms of this implementation appear in Fig. 10.

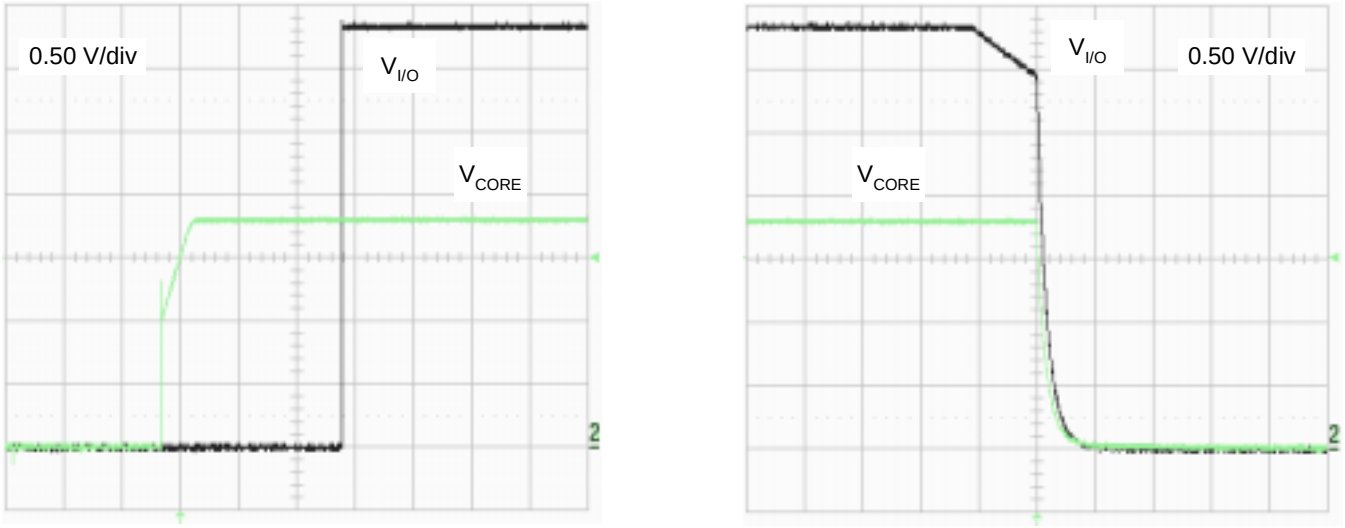


Fig. 10. Ramp-up (a) and ramp-down (b) waveforms for circuit of Fig. 9.

Simultaneous Sequencing

Some applications require either a specific slew rate or a maximum inrush current during power-up and power-down, which can be realized with the circuit in Fig. 11.

The power-up and power-down sequencing circuit employs network R3 and C2 to generate a ramp-up slope. This network is the slew rate reference for the output of the LDO during power-up and power-down. The operational amplifier compares the output voltage at its non-inverting input with the voltage applied to its inverting input. It then adjusts the output voltage to match the slew rate determined by the RC network. When $\overline{\text{ENABLE}}$ transitions low, Q1 is switched off, and R3 starts to charge C2 to the input voltage rail level. When V_{OUT} reaches 2.5 V, set by R1 and R2, the voltage at the operational amplifier inverting input continues to rise, causing the operational amplifier output to decrease. This reverse-biases D1, thereby removing the power-up and power-down sequencing circuit from the feedback loop. R4 and C1 ensure a smooth voltage rise during power-up.

In this example, the output voltage set point can be calculated as follows:

$$R1 = R2 \times \left[\left(\frac{V_{OUT}}{V_{REF}} \right) - 1 \right]$$

where V_{REF} = 1.224 V for the LDO shown.

Fig. 12 features simultaneous sequencing circuitry that programs a required slew rate during power-up and power-down using IC2 as a tracking LDO.

The power-up and power-down sequencing circuit is using the same basic circuit as described above with programmable slope. In this example, the core voltage must track the I/O voltage during power-up and power-down. Additionally, the I/O voltage must be within 600 mV of the core voltage during power-up and power-down. If these conditions are violated, the processor could be damage due to forward-biasing of the substrate diode.

During power-up and power-down, IC4 provides active tracking to ensure that the voltage difference between I/O and core voltage is far less than the required 600 mV. Schottky diode D3 provides an additional level of protection.

During power-up, IC1's output voltage increases with the applied slope ramp at the inverting node of IC3. Operational amplifier IC4 derives the ramp-up and ramp-down slope from the 2.5-V I/O output voltage rail. During power-up, the I/O voltage slowly increases, and this voltage is applied to the inverting node of IC4. The non-inverting node detects the core voltage, which is the output of linear regulator IC2. When the core voltage reaches 1.5 V, set by R5 and R6, the inverting input of operational amplifier IC4 continues to rise, causing the operational amplifier output to decrease. This reverse biases D2, removing the tracking circuit from the feedback loop. Fig. 13 displays power-up and power-down waveforms, respectively.

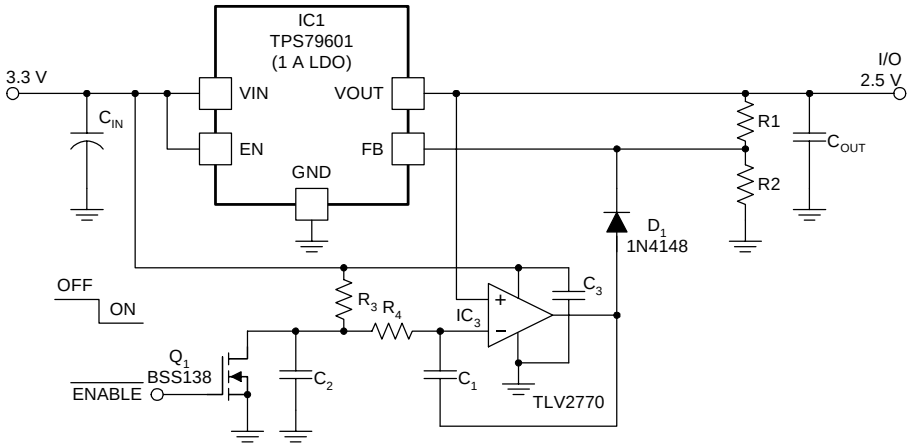


Fig. 11. Capacitor-programmable slew rate circuit.

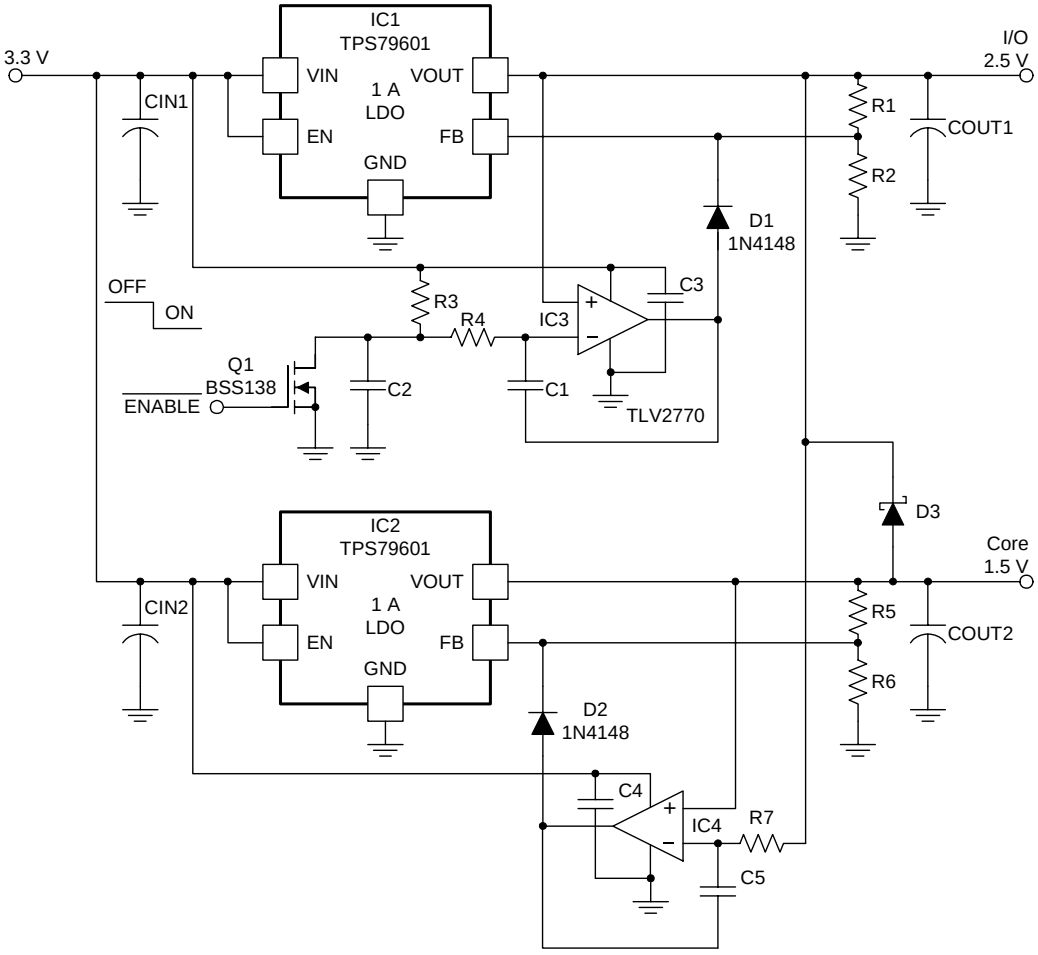


Fig. 12. Simultaneous sequencing with capacitor-programmable slew rate circuit.

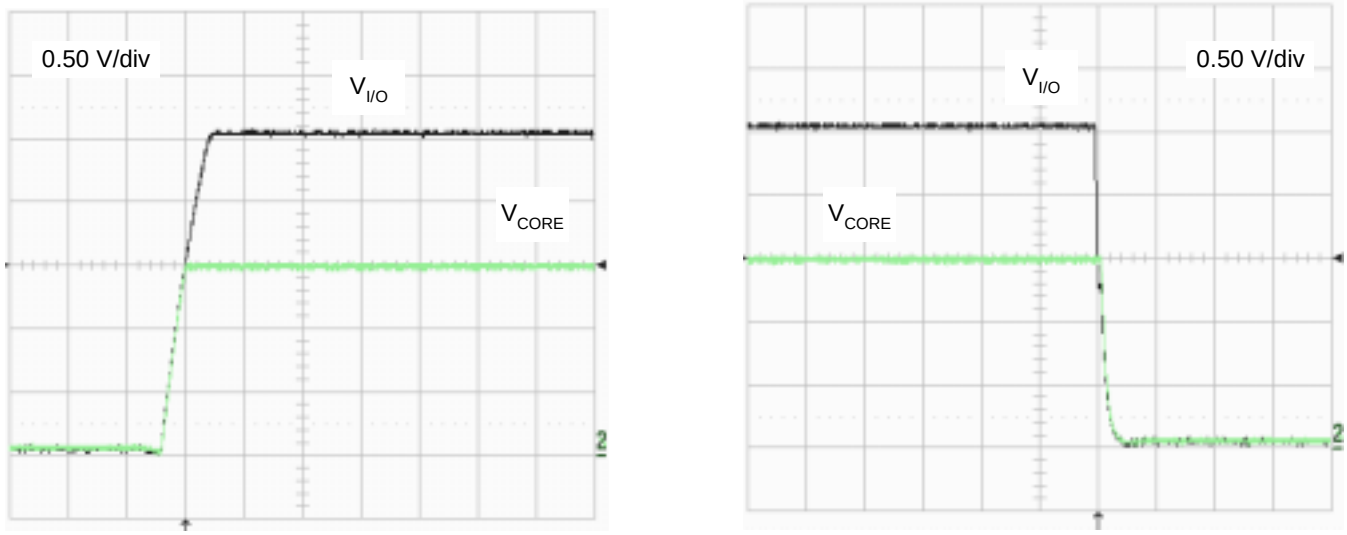


Fig. 13. Power-up (a) and power-down (b) waveforms for circuit of Fig. 12.

C. LDO and Power Distribution Switch

Sequential Sequencing

Some applications challenge the designer to apply core voltage prior to I/O voltage, even though the input source voltage is already at the I/O voltage level. A high-side power distribution switch can be used to disable the I/O supply until the core voltage is powered up and stable. Fig. 14 shows a sequential power supply sequencing implementation using the TPS2150, which integrates a high-side power switch with an LDO.

The TPS2150 uses the power good function of the LDO to enable the power switch, resulting in the power-up waveforms of Fig. 15a. The power switch and LDO feature pull down MOSFETs to discharge the bulk capacitance when the devices are disabled (Fig. 15b).

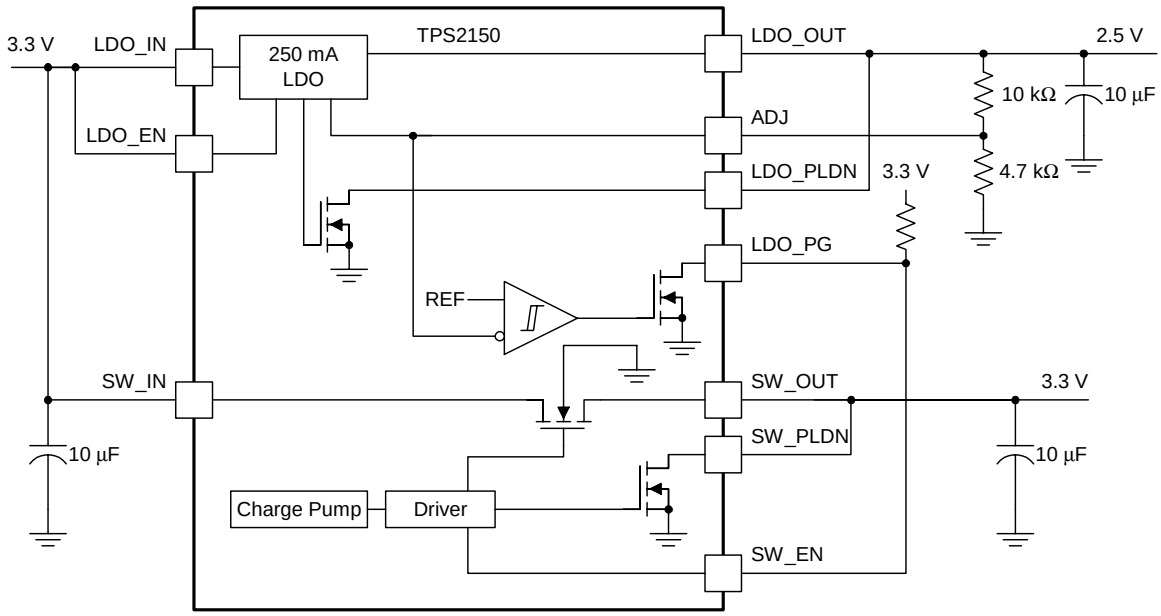


Fig. 14. Sequencing with combination LDO/high-side switch (core then I/O).

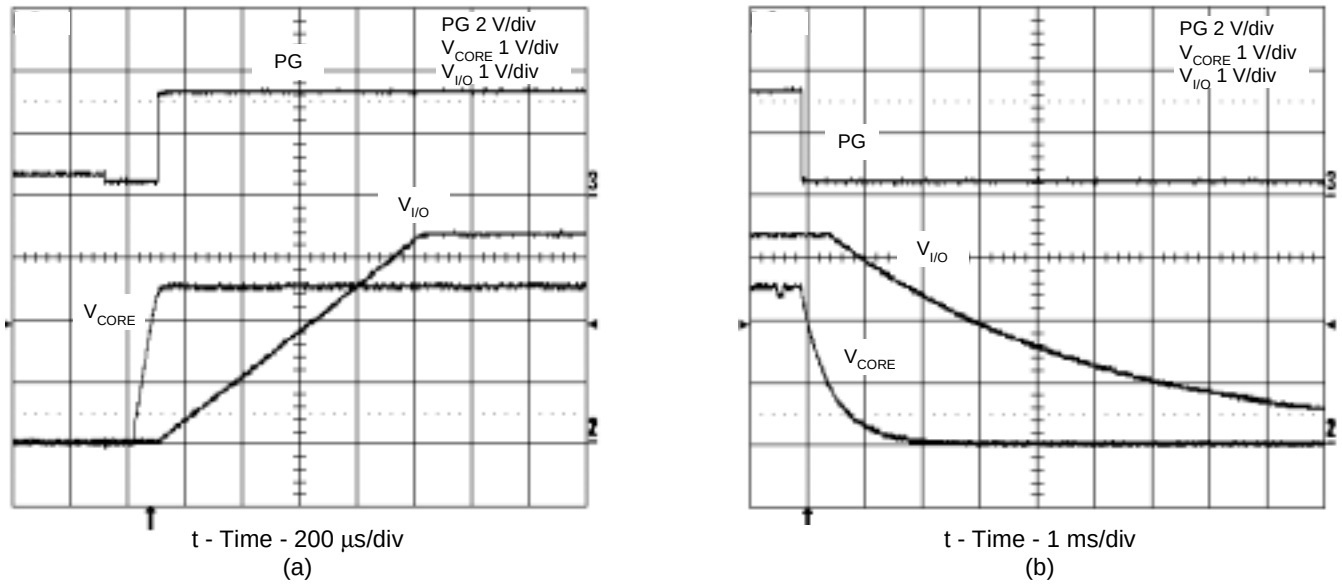


Fig. 15. Power-up (a) and power-down (b) of circuit in Fig. 14.

Fig. 16 implements the opposite configuration, in which the I/O voltage is applied before the core at turn-on. Corresponding waveforms are shown in Fig. 17.

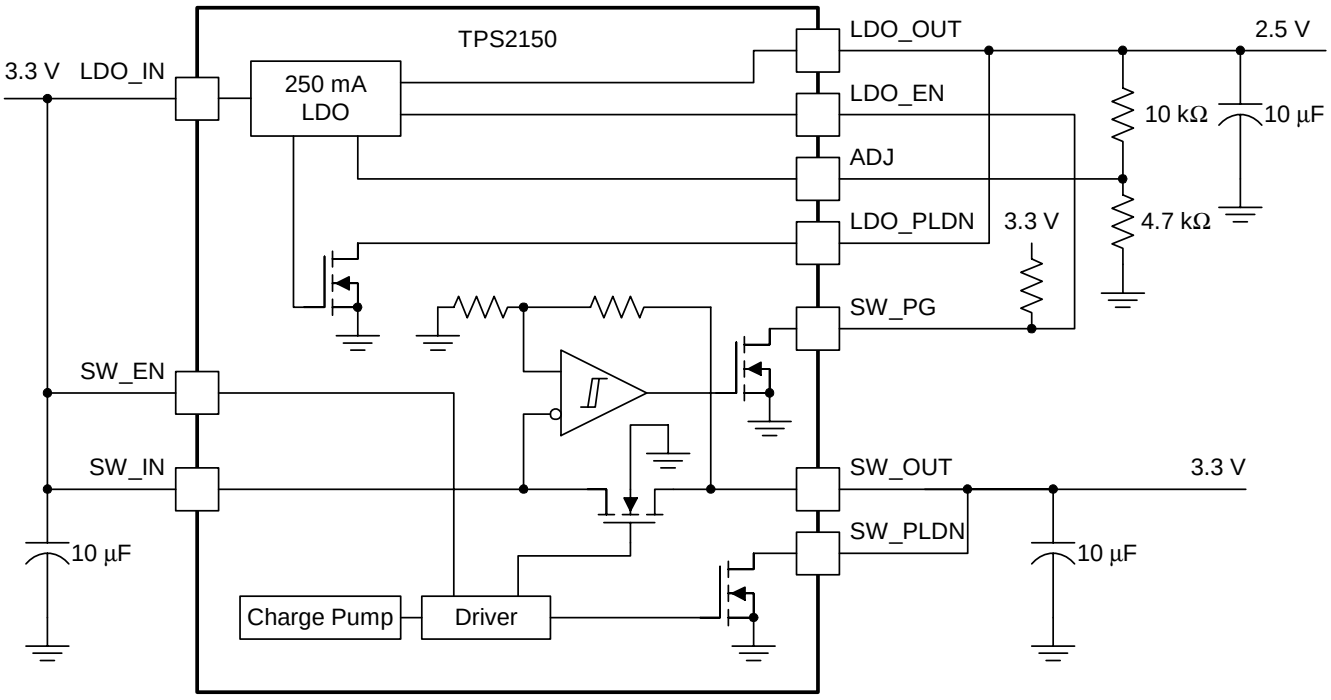


Fig. 16. Sequential sequencing (I/O then core).

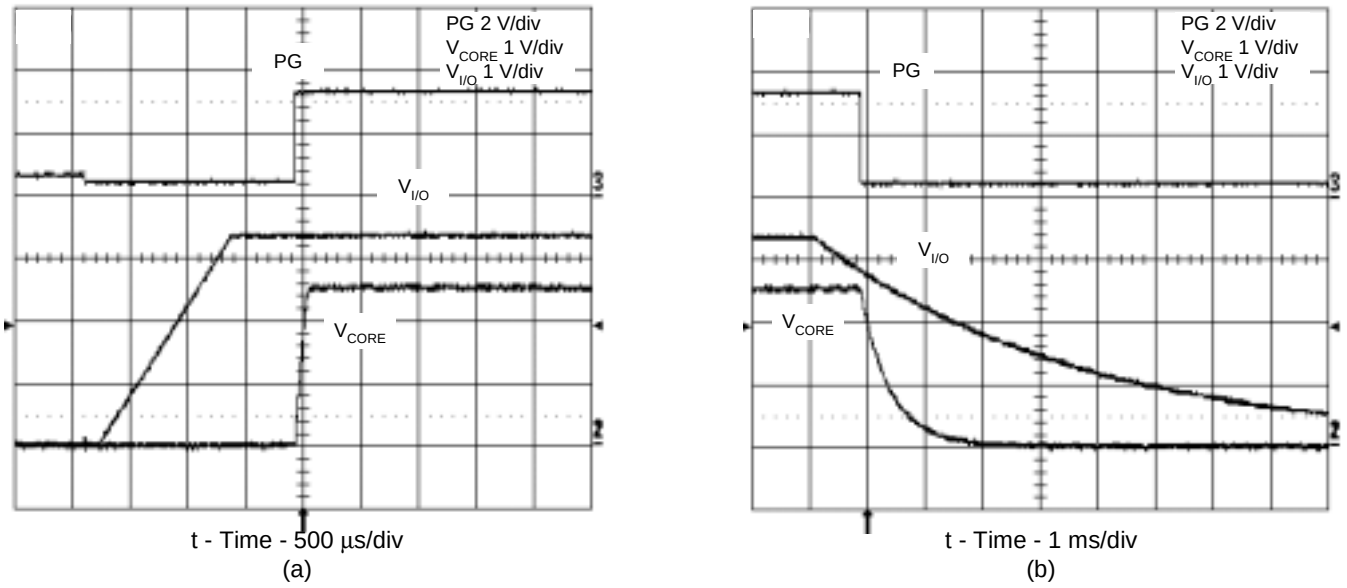


Fig. 17. Power-up (a) and power-down (b) waveforms for circuit of Fig. 16.

D. Hot-Swap Control

Simultaneous Sequencing

Another method to power-up and power-down with minimum voltage difference between the power supply rails is to use MOSFETs between the supply and load. Fig. 18 shows a simplified schematic using two MOSFETs and a TPS2331 hot swap controller to provide simultaneous start-up sequencing. By driving the gates of the MOSFETs with the same gate driver, the power supply rails effectively ramp together (Fig. 19a). The TPS2331 features an integrated pull-down transistor to discharge the bulk output capacitors, see Fig. 19b. The Schottky diode clamps the core supply during power-down.

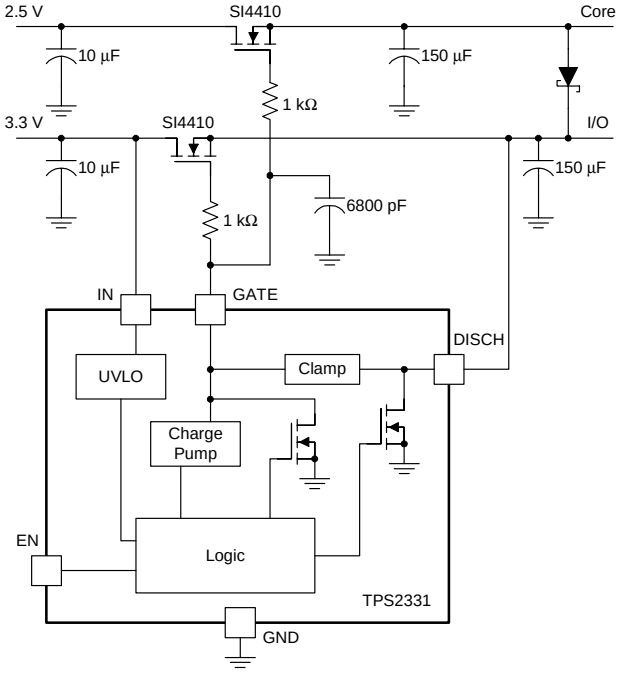
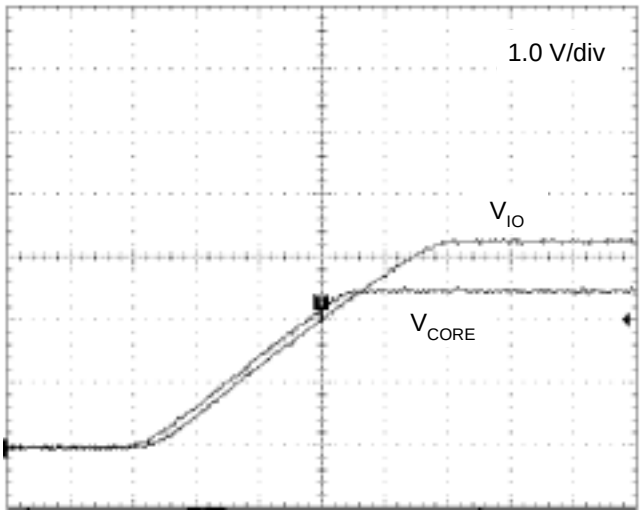
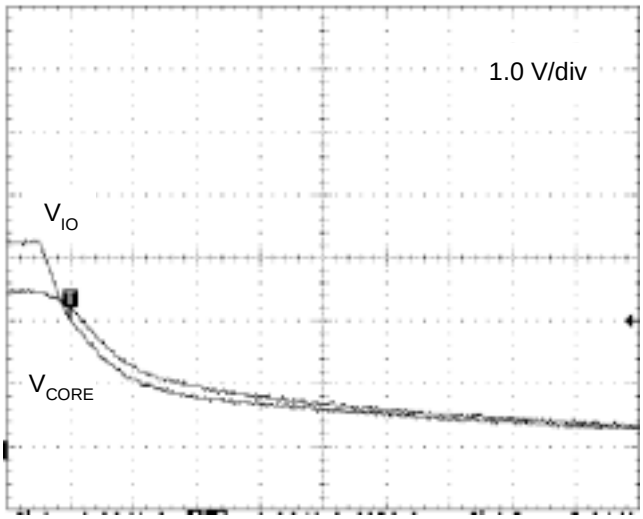


Fig. 18. Simultaneous sequencing with hot-swap controller.



t - Time - 500 µs/div
(a)



t - Time - 20 ms/div
(b)

Fig. 19. Power-up (a) and power-down (b) waveforms for circuit of Fig. 18.

E. Microcontroller

Microcontrollers are among the most versatile devices available for sequencing. If the power supplies to be controlled feature enable pins, then controlling them is a simple matter of using general purpose input and output (GPIO) lines. If the enable function is not available, an in-line MOSFET or power distribution switch can be used to control the power supply, either with a GPIO or PWM signal.

Use of a microcontroller is illustrated with the MSP430, a 16-bit RISC processor featuring several analog peripherals and a JTAG interface. The circuit of Fig. 20 uses the TPS725xx family of LDOs to provide 3.3 V, 2.5 V and 1.8 V from an input DC source. These LDOs have an enable pin and reset function. This circuit can easily be expanded to any number of voltage rails. The MSP430 monitors a control variable to determine when each rail should be activated. For power sequencing applications, the two most commonly controlled variables are time and voltage.

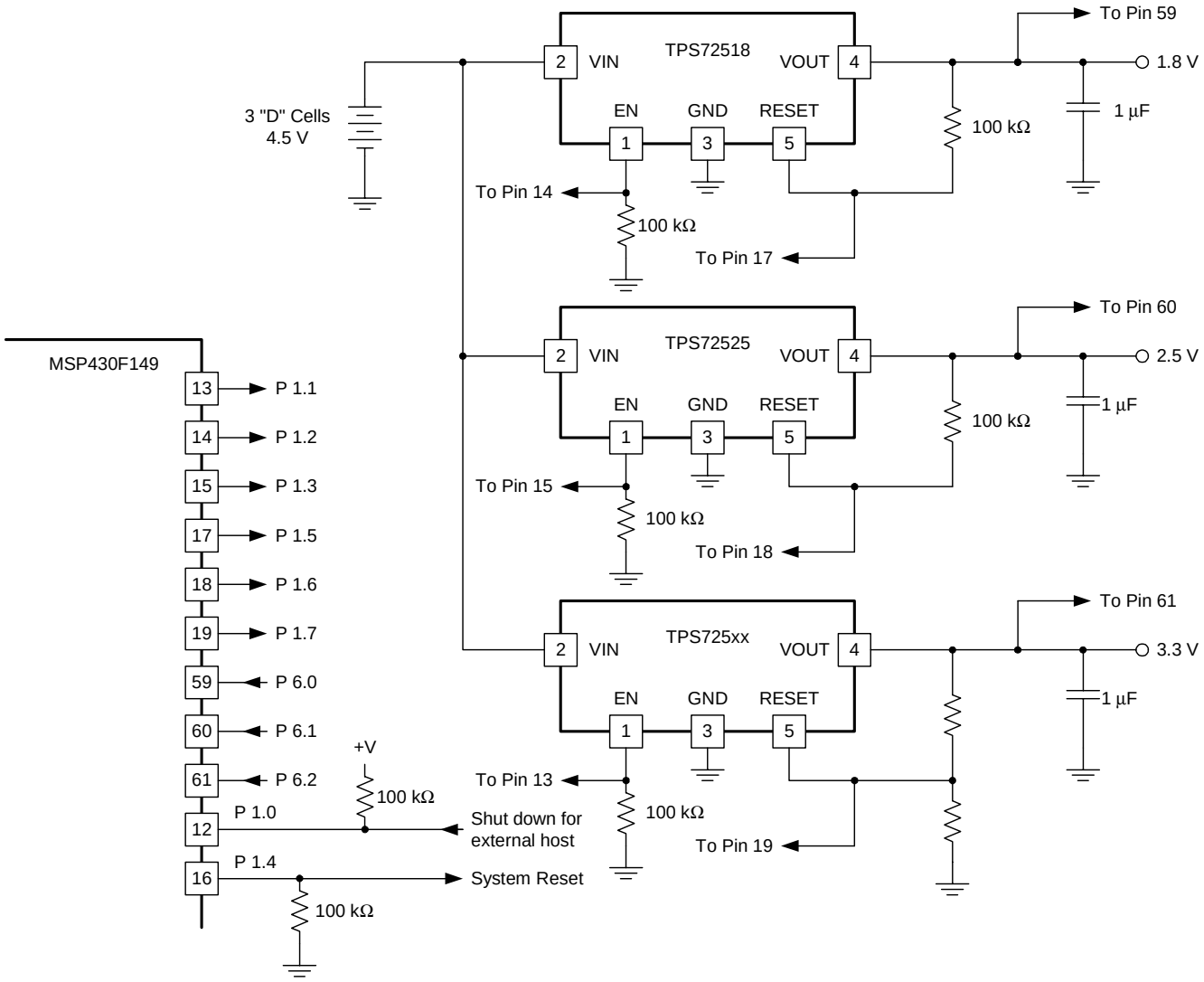


Fig. 20. Sequencing implemented with the MSP430 microcontroller.

Sequential Sequencing

When time is the control variable the first rail is enabled then, at a specific time thereafter, the next rail is enabled. Some time after that the next rail is enabled and so on, until all rails have been enabled. The MSP430 provides the timing sequence and the control signals to turn on the power supplies (Fig. 21).

If voltage is the control variable, then the first voltage rail is activated and its rise is monitored via an analog-to-digital converter (ADC). When the first voltage rail has reached a specific voltage level, the next voltage rail is enabled and its rise is monitored until it has reached a specified voltage level, at which point the next voltage rail is enabled and monitored. This continues until all voltage rails have been enabled (Fig. 22). When using voltage as the control variable, either a GPIO or PWM signal can be used as the enable signal, depending on whether rail tracking is required. Of course, a combination of voltage and timing control can also be used.

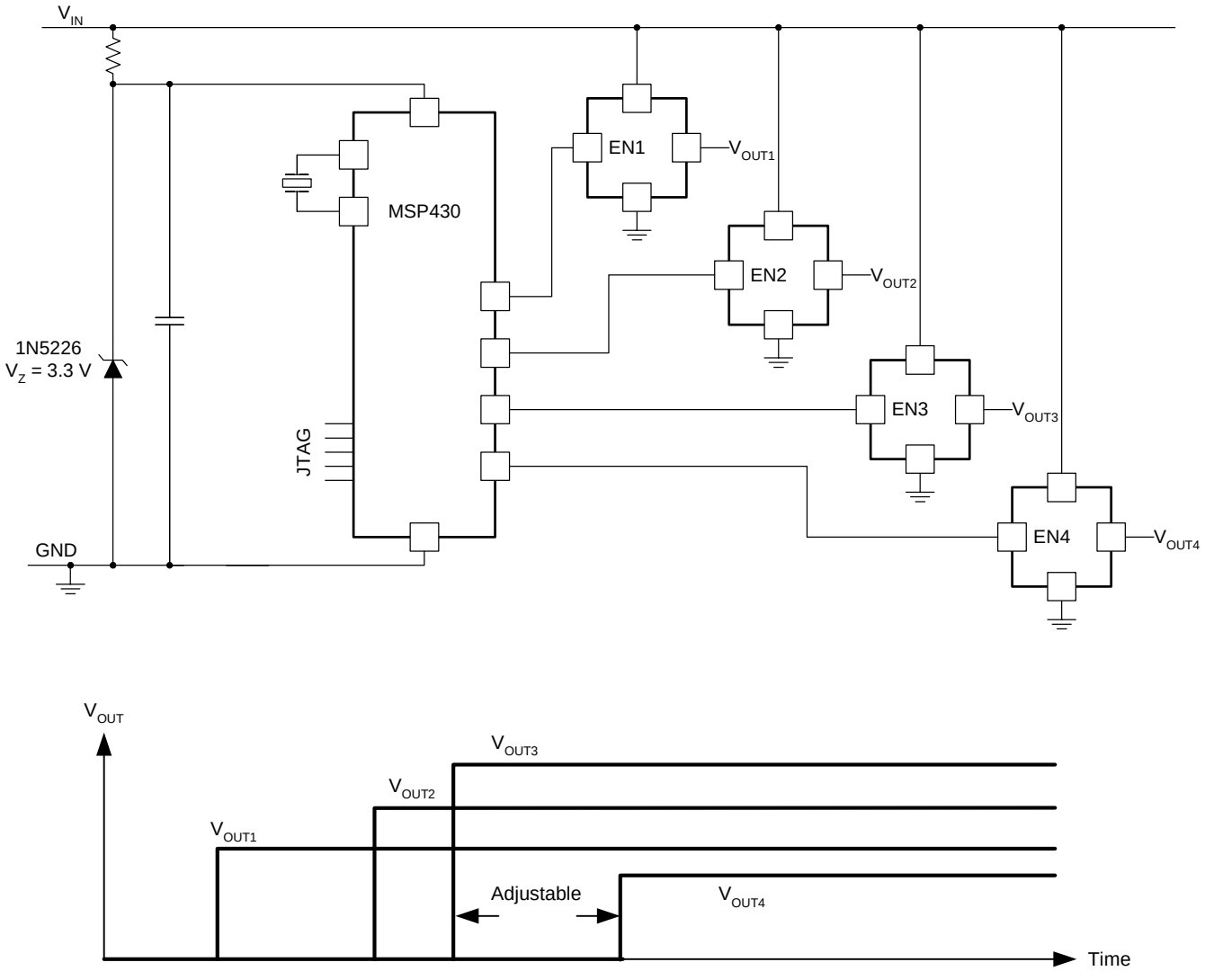


Fig. 21. Sequential sequencing with microcontroller (time as the control variable).

Once the MSP430 has turned on all the voltage rails and applied the system reset, it enters the monitor mode. It continually checks the output voltages, via the reset or output pins, depending on whether time or voltage is the control variable. If a fault occurs, the MSP430 enters an error routine. The most obvious fault would be the loss of a voltage rail, but other faults such as over- or under-voltage could also be monitored. The actions taken in the error routine are completely application-dependent. The simplest action is to power down all rails, but programmability offers the user complete control.

Power-down sequencing can be just the opposite of the power up sequence, or any sequence required to meet system demands. One addition to the power-down sequence could be turning on dummy loads to discharge the output filter capacitors. [16]

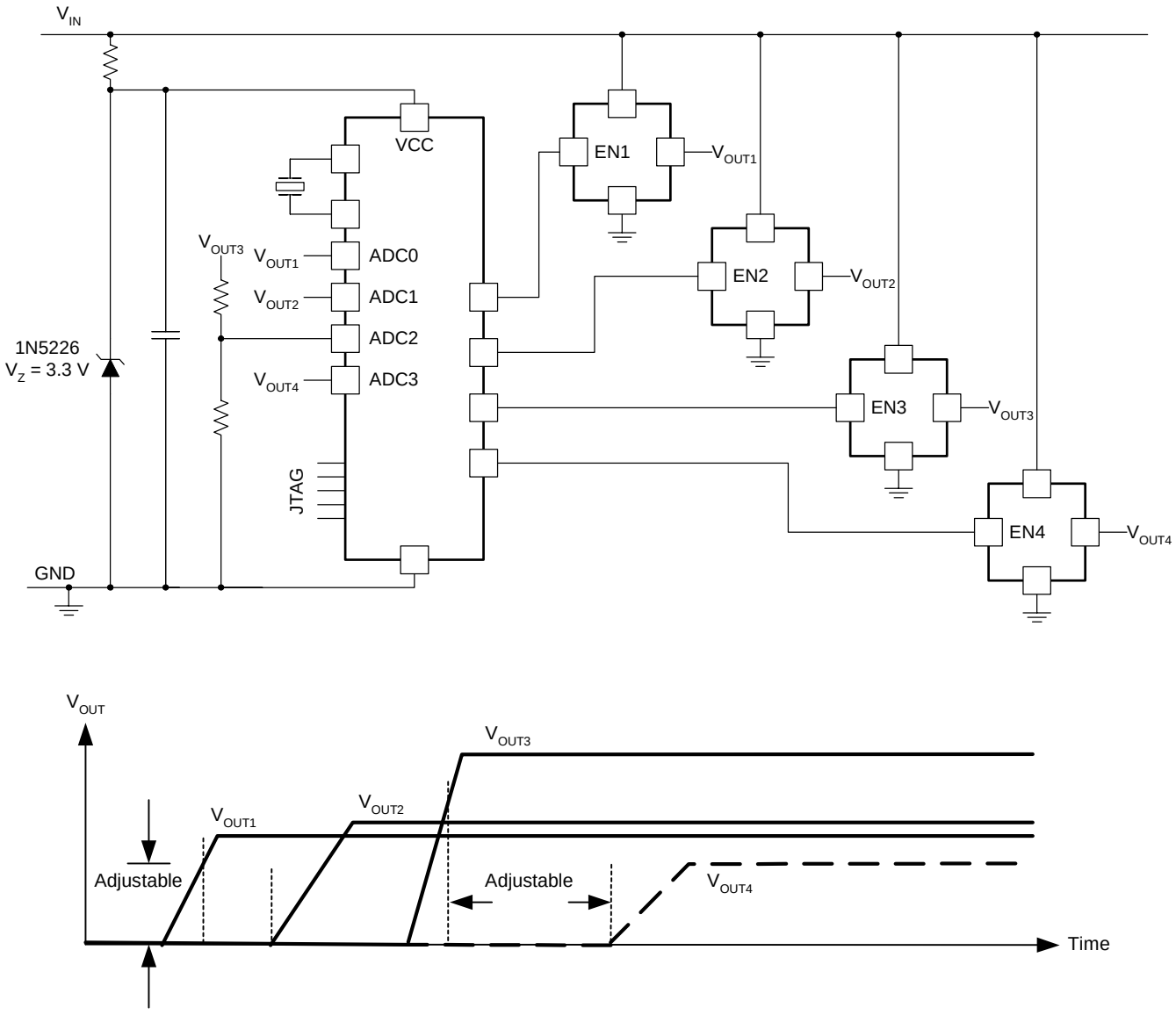


Fig. 22. Sequential sequencing with microcontroller with voltage as the control variable.

V. SEQUENCING WITH SWITCH-MODE CONTROLLERS, CONVERTERS AND MODULES

A. Pre-Bias Start-Up and Synchronous Rectifier

Many switch-mode power stages employ synchronous rectification to improve efficiency, as illustrated by the simplified synchronous buck converter shown in Fig. 23. In this example, VIO comes up first, and applies core voltage through the series diodes before the core's converter is enabled. Defining this as a pre-bias condition, in which voltage is applied at the converter output before the converter is enabled. When the converter's PWM controller is enabled, it soft-starts the high-side FET, and its duty cycle (D) ramps gradually from zero to that required for regulation. However, if during soft-start the synchronous rectifier (SR) FET is on when the high-side FET is off (SR FET duty cycle = 1-D), the SR sinks current from the output (through the inductor), tending to cause both the core and I/O voltages to drop. It is for this reason that PWM controllers with pre-bias start-up have been introduced, which disable SR drive during start-up. Until drive to the SR is enabled, inductor current flows through the parasitic body diode of the SR FET rather than through the channel. Once the soft-start time is complete, drive to the SR is enabled.

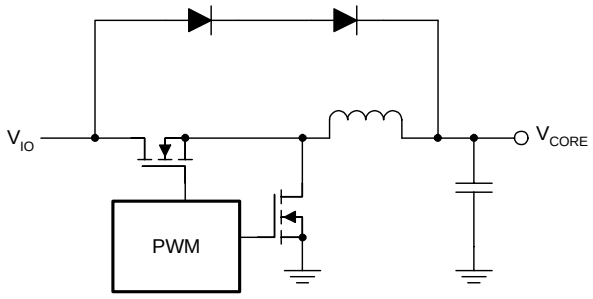


Fig. 23. Example of pre-bias condition.

The need for synchronous converters with pre-bias start-up also arises when using a sequential power-up technique with some ASICs, in which a leakage path within the device causes some I/O voltage to appear on the core voltage before the core converter is enabled. Fig. 24 uses a PTH series power module for illustration. The PTH power modules incorporate synchronous rectification, so can sink current under normal operating conditions, but the 3.3-V and 5-V input versions do not do so during power-up, or whenever the module is turned off via the Inhibit pin. In Fig. 24, module U1 (PTH05020W) produces 2.5 V for the core.

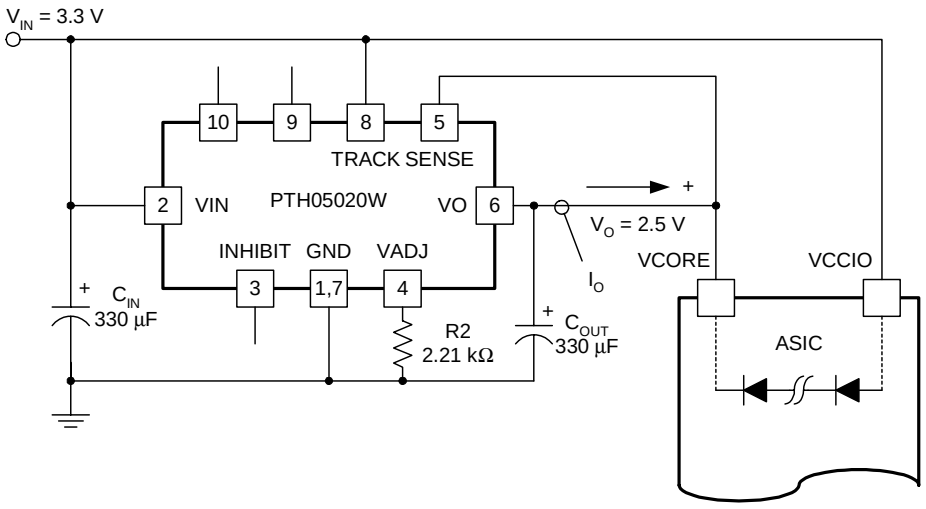


Fig. 24. Pre-bias example with PTH power module.

Fig. 25 shows the waveforms of the circuit after input power is applied. It shows V_O rising along with VIN once VIN forward-biases the leakage path within the ASIC. Note that output current (I_O) is negligible until V_O rises above the pre-bias voltage (point A). From hereon, the waveform of I_O exhibits a positive output current. [19]

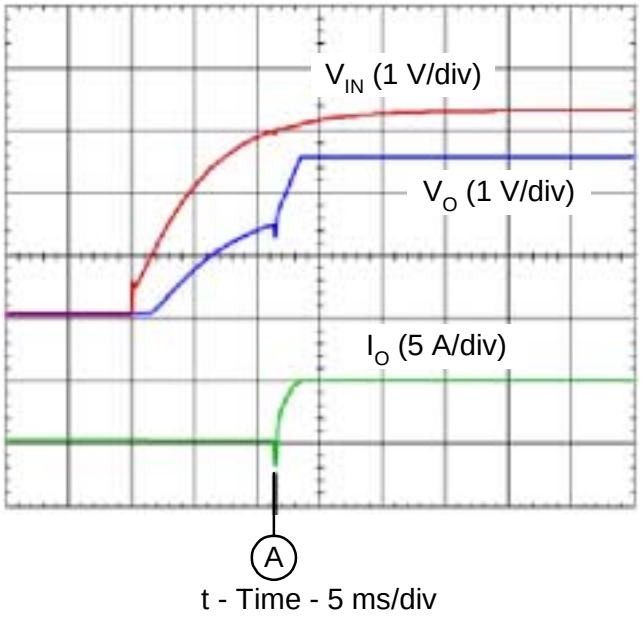


Fig. 25. Power-up waveforms with pre-bias.

B. DC-DC Controllers

Ratio-Metric Sequencing

In ratio-metric sequencing, multiple output power rails start ramping at the same time and in proportion. This function can be accomplished with multiple controllers sharing a common soft-start capacitor. The solution in Fig. 26 (waveforms in Fig. 27) is based on two TPS40051 synchronous buck controllers with a wide input voltage range of 8 V to 40 V. These controllers drive synchronous rectifiers and feature feed-forward voltage-mode control. In this example, I/O voltage is 3.3 V and core voltage is 1.8 V.

Soft-start is programmed by charging external capacitor C2 via an incorporated current source of 2.3 µA. The voltage rise on C2 is then fed into a separate non-inverting input to the error amplifier (in addition to the feedback voltage and the 700-mV reference voltage). Once voltage on C2 exceeds 700 mV, the internal reference voltage is used to establish regulation. To ensure a controlled ramp of the output voltage, the soft-start time should be greater than the output inductor and output capacitor time constant.

So, in this example,

$$t_{START} \geq 2\pi\sqrt{L1 \times C13} \quad \text{(seconds)}$$

and the soft-start capacitance calculates as:

$$C2 = 2 \times \left(\frac{2.3\ \mu A}{0.7\ V} \right) \times t_{START} \text{ (Farads),}$$

since the current feeding the soft-start capacitor is 2.3 µA per controller. [20]

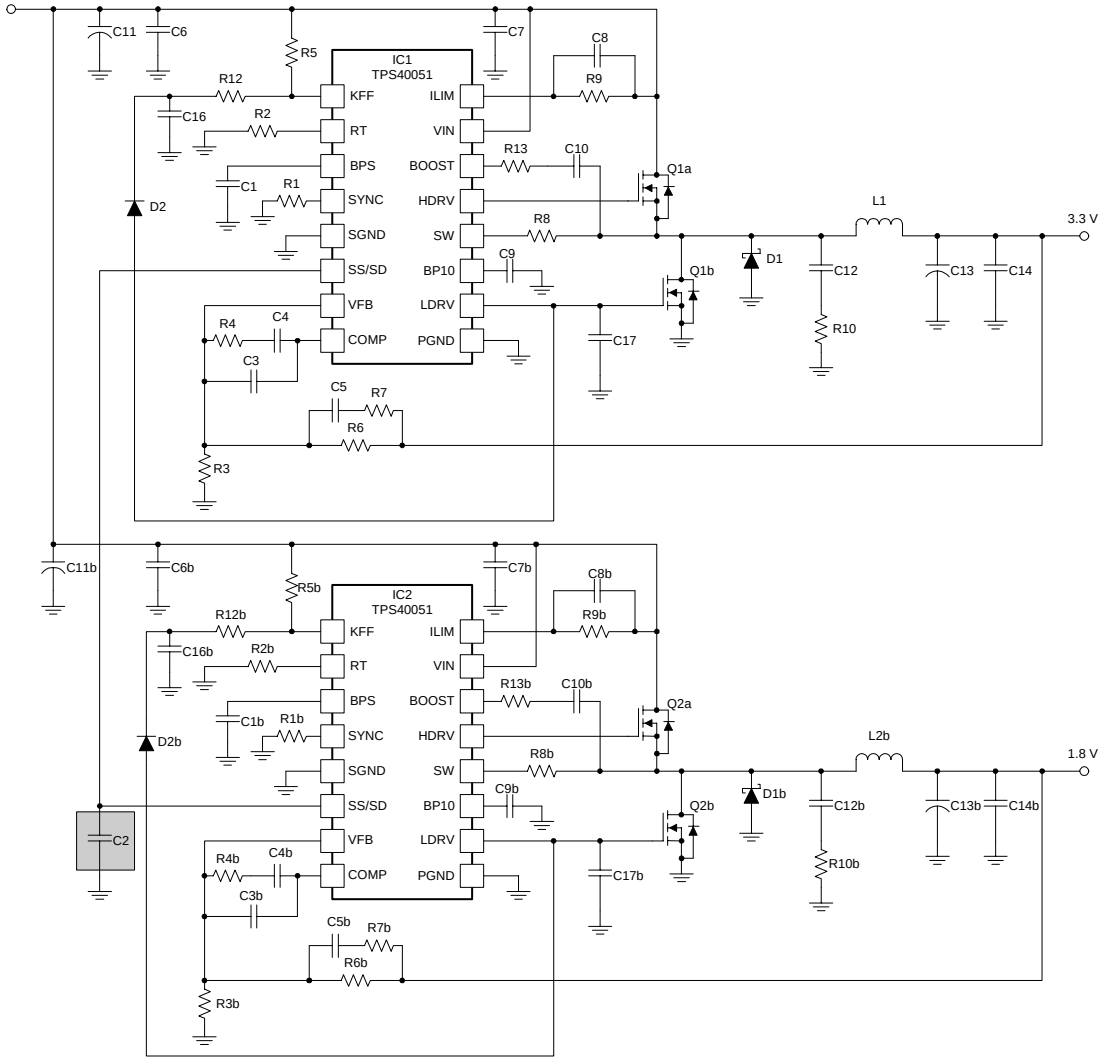


Fig. 26. Ratio-metric sequencing with common soft-start capacitor.

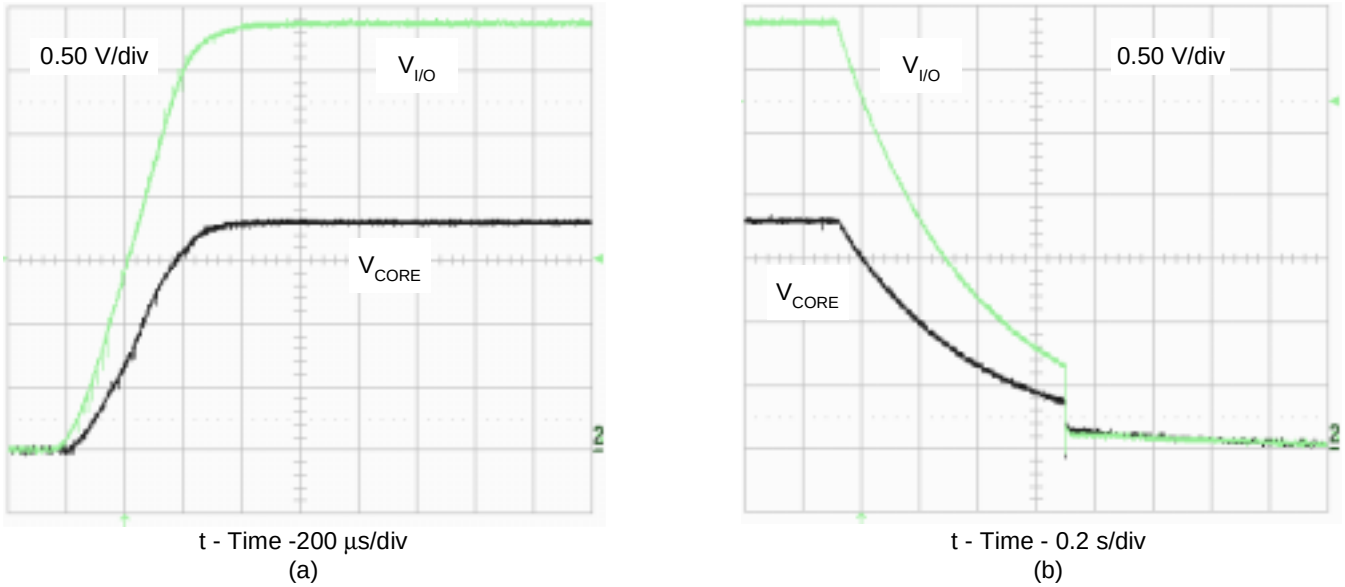


Fig. 27. Power-up (a) and power-down (b) waveforms for Fig. 26.

C. DC-DC Converters

Simultaneous Sequencing

As previously mentioned, the objective of simultaneous sequencing is to minimize the potential difference between voltage rails as they ramp. Fig. 28 illustrates such an implementation using switcher with integrated FET (SWIFT) converters that integrate both high-side and synchronous rectifier FETs. IC1 provides I/O voltage of 3.3 V, while IC2 provides core voltage of 1.5 V. The converters share one soft-start capacitor (C14) to ensure the outputs ramp at the same slope. Note that these are voltage-mode controlled converters. IC2 acts as master controller. Its output voltage is programmed at 1.5 V via voltage divider R14 and R12. Additionally, its power-good (PGOOD) comparator is used as a master flag to release the voltage divider of IC1.

During power up (Fig. 29a), both converter output voltages rise with the ramp of the soft-start capacitor to an output voltage of 1.5 V. This is due to voltage dividers R14 and R12 at IC2, and R8 and R3 at IC1. During power-up, the power good (PGOOD) pin of IC2 is active low, holding Q1 off so that the output voltages track during power up until IC2 reaches 90% of its final value. Once IC2 detects an output voltage level of 90% or greater, PGOOD goes high impedance, and pull-up resistor R4 drives the gate of Q1 on via RC network R5 and C11. Once the gate threshold voltage of Q1 reaches 1.6V (typical), it starts to conduct and switches R6 in parallel to R3. This parallel combination changes the output voltage set point of IC1 to program 3.3-V output.

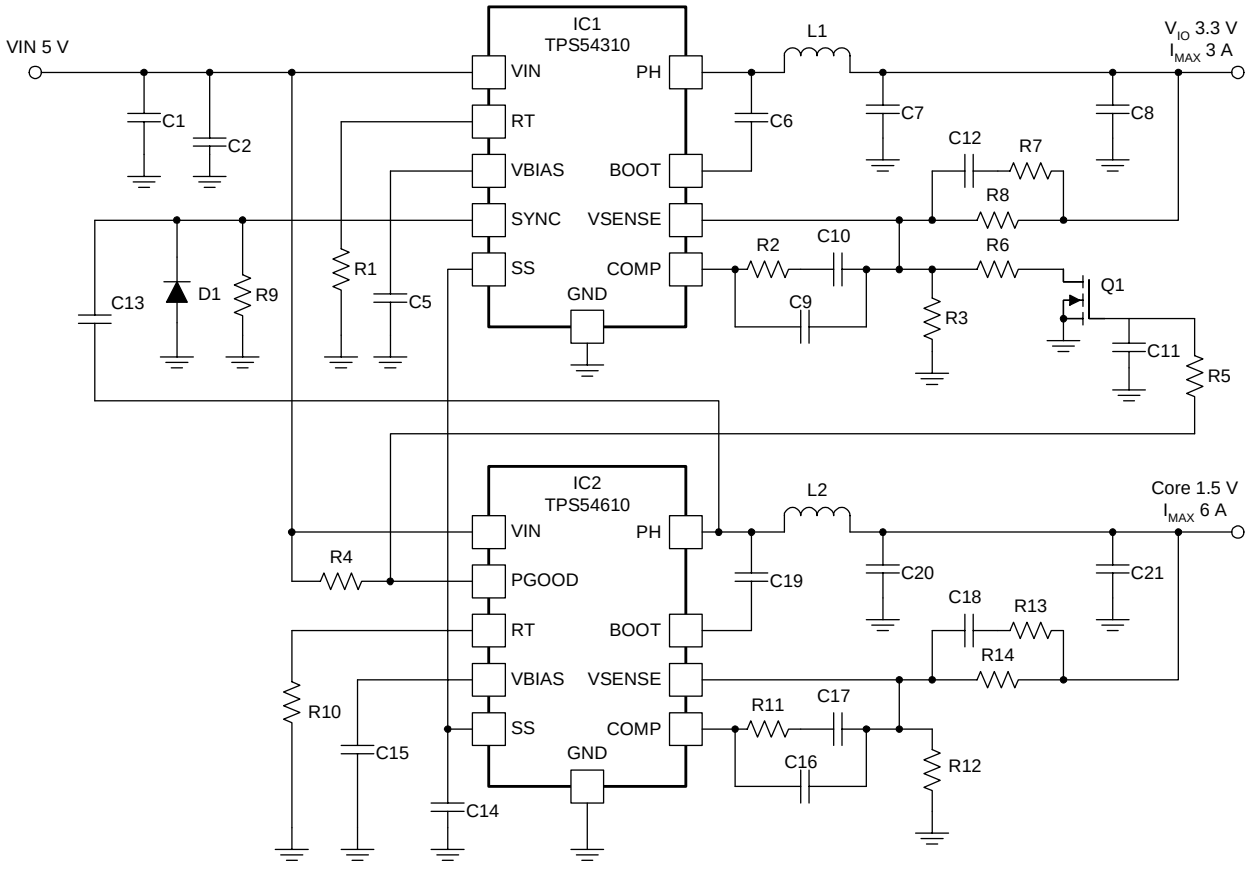


Fig. 28. SWIFT converters configured for simultaneous sequencing.

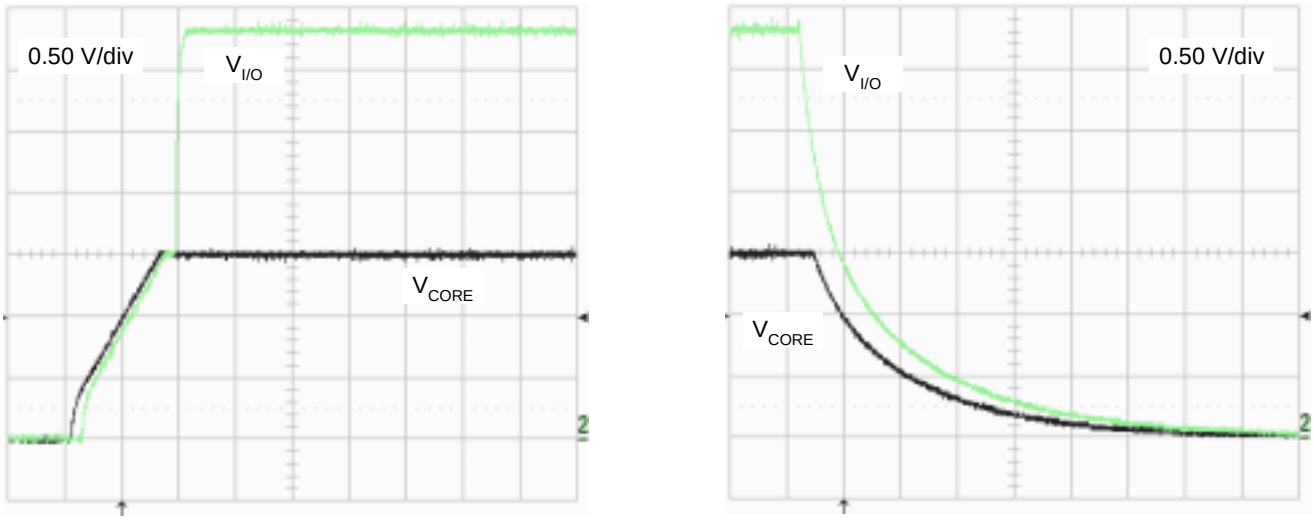


Fig. 29. Power-up (a) and power-down (b) waveforms for Fig. 28.

In this implementation, a general purpose BSS138 FET is used with a typical threshold voltage of V_{GSth} = 1.6 V. This FET features $R_{DS(on)} < 10\ \Omega$ (negligible compared to the values of R3 and R6), so does not affect the calculated output voltage set point value.

The set point resistor values can be calculated as follows:

A. Equation for V_{CORE}

$$R3 = \frac{V_{REF} \times R8}{V_{CORE} - V_{REF}}$$

V_{CORE} = 1.5 V, V_{REF} = 0.891 V

Choose R8 = 27.4 kΩ

then R3 = 40.2 kΩ

B. Equation for $V_{I/O}$

$$R_X = \frac{V_{REF} \times R_8}{V_{I/O} - V_{REF}}$$

where R_X is $R_3 \parallel R_6$

$V_{I/O}$ = 3.3 V

so R_X = 10.22 kΩ

C. Equation for R6

$$1/R_X = 1/R3 + 1/R6$$

$$\text{so, } R6 = \frac{1}{1/R_X - 1/R3}$$

R6 = 13.7 kΩ

PGOOD of IC2 transitions low when V_{CORE} falls under 90% of its initial value during power-down (Fig. 29b). This discharges C11 and the gate of Q1 via R5. Once the gate of Q1 falls below its threshold voltage level (1.6 V typical), R6 is removed from the feedback divider. Thus IC1's output voltage set point drops to 1.5 V and the I/O voltage ramps down along with the core voltage. Note during power-down the voltages do not track each other due to differing output capacitor energy storage and load levels. The tracking version of the SWIFT converters can be used to address this issue.

A noteworthy feature of this implementation is that the converters are running at the same switching frequency. IC2 is the master device programmed to a switching frequency of 700 kHz. IC1 starts at a lower initial switching frequency of roughly 630 kHz, 10% below the switching frequency of IC2. Once IC2 begins to operate, it synchronizes IC1 via the SYNC pin. Diode D1 limits negative voltage spike amplitude at the SYNC input.

Sequential Sequencing

Fig. 30 shows a dual power supply design with sequential power-up using the TPS54350 dc/dc converter. The circuit uses the power good function of the I/O supply to activate the enable of the core supply. Once the I/O supply is up and stable, the power good pin (PWRGD) transitions from active low to high impedance (see Fig. 31). The TPS54350 has an internal pull-up current source on the enable (ENA) pin, so an external pull-up resistor is not required to enable the core supply. As discussed in the last section, the challenge with using this power good and enable technique is the power-down sequence. It is preferred to power down the supply rails in the reverse order of power up. Because of supply loading and the disabling of the I/O supply and core supply at the same time, this order is not guaranteed.

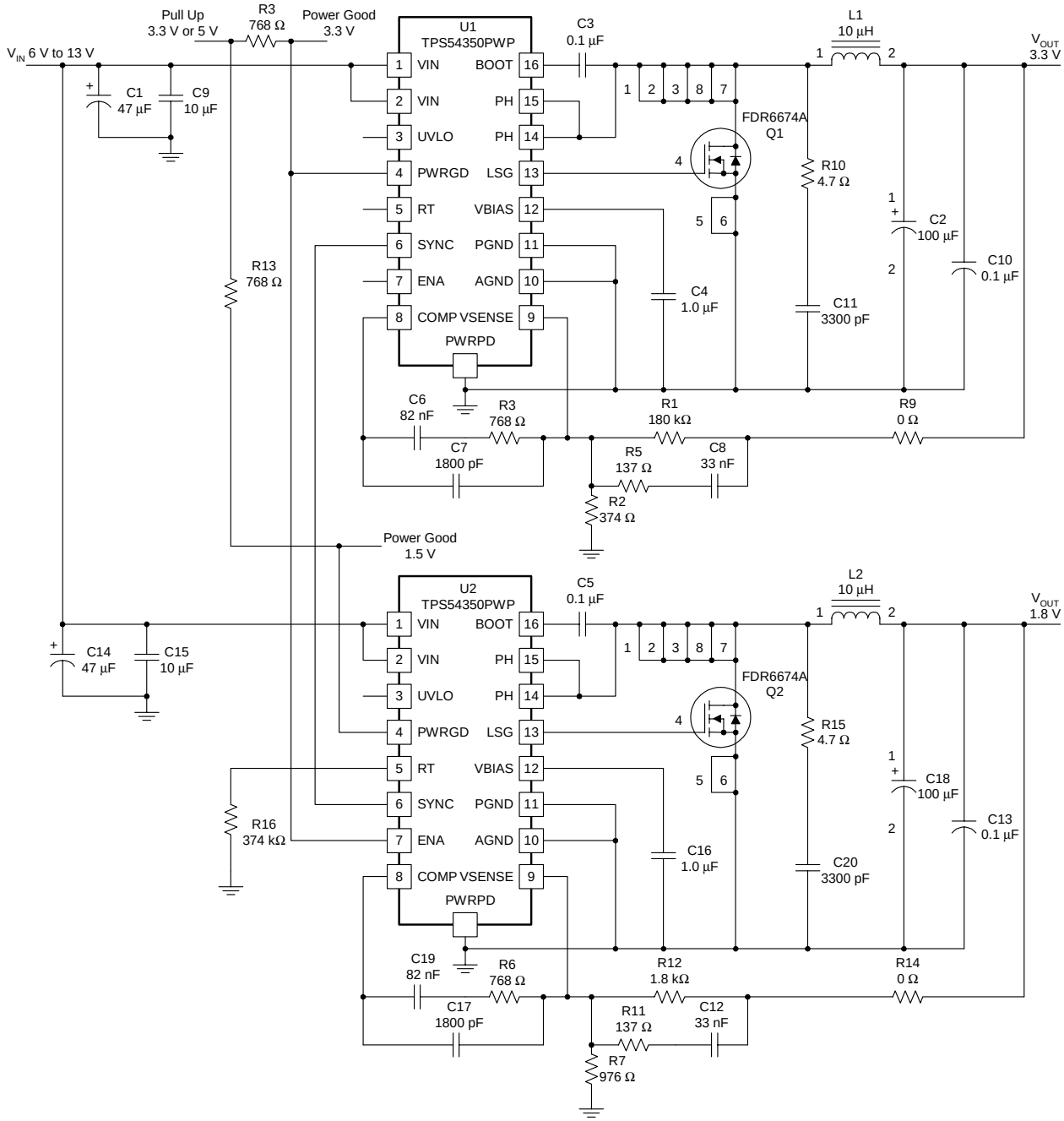


Fig. 30. Sequential sequencing with TPS54350 converters.

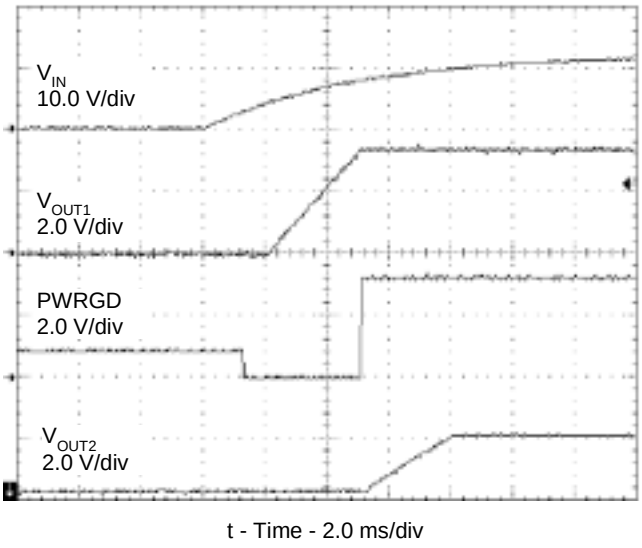


Fig. 31. Power-up waveforms of Fig. 30.

Another technique to implement sequential sequencing is implemented by connecting the power good function to the TRACKIN pin of a TPS54680 Sequencing SWIFT converter using resistors and a capacitor (Fig. 32) [10]. The TPS54680 was designed for applications that have critical power supply sequencing requirements. The device has a TRACKIN pin to facilitate the various sequencing methods. The TRACKIN pin is the input to an analog multiplexer that compares a 0.891-V internal voltage reference to the voltage on the TRACKIN pin, and connects the lower of the voltages to the non-inverting node of the error amplifier. When the TRACKIN pin voltage is lower than the internal voltage reference, the TRACKIN pin voltage is effectively the reference for the power supply. The power-up and power-down waveforms are shown Fig. 33.

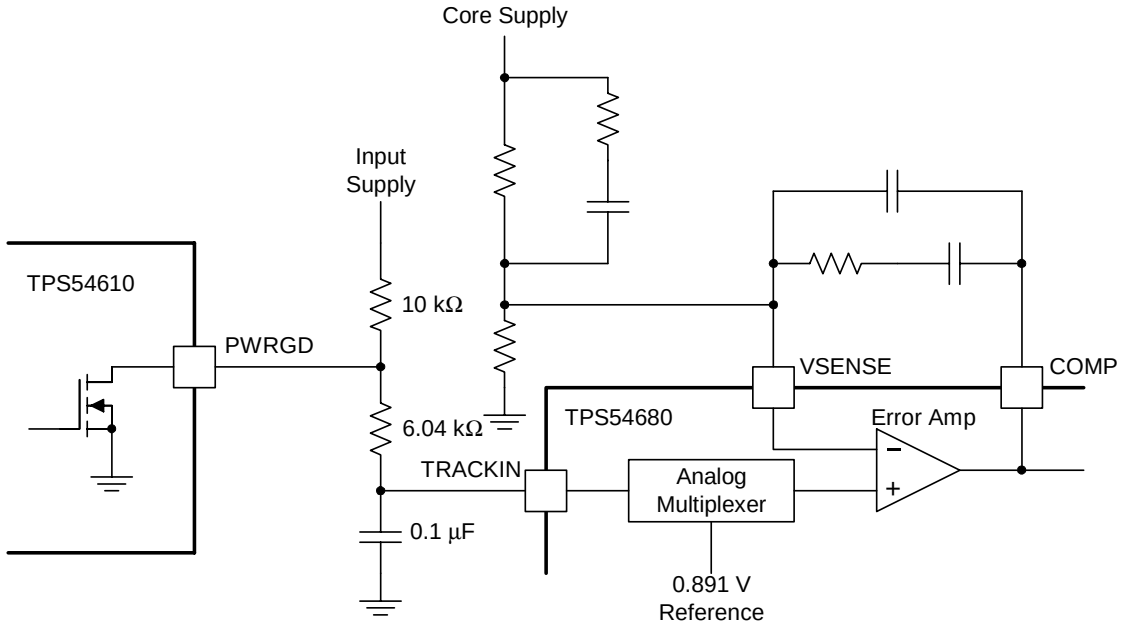
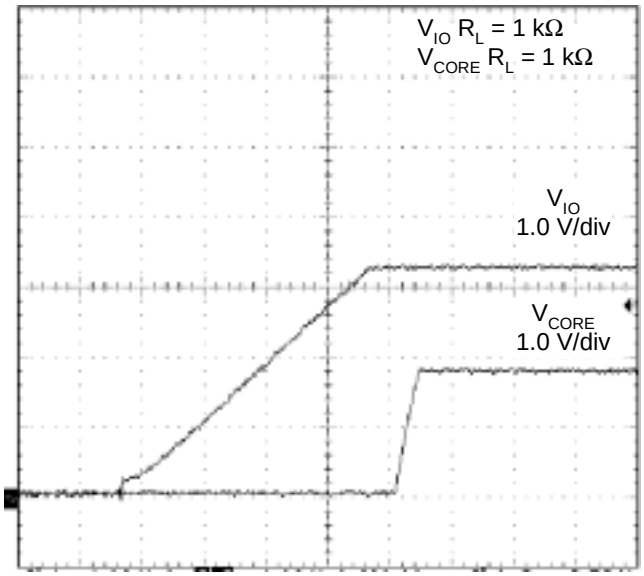


Fig. 32. Sequential sequencing with TPS54680 track input.



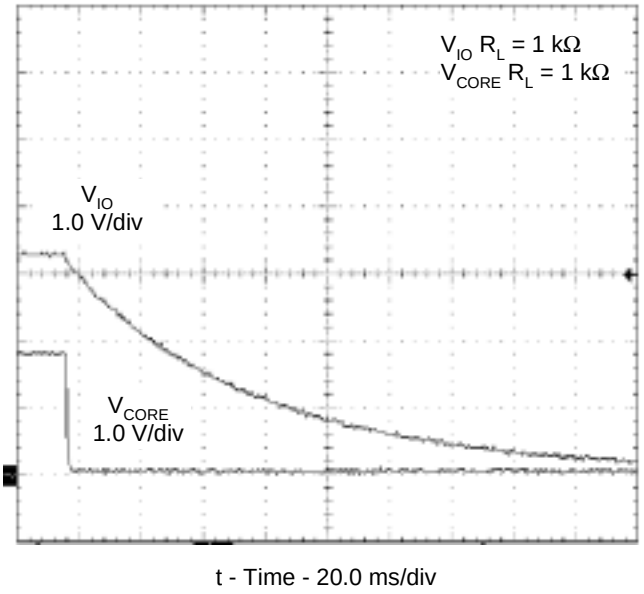


Fig. 33. Power-up (a) and power-down (b) waveforms of Fig. 32.

As shown in Fig. 33a, the 3.3-V I/O supply ramps first. When the I/O supply reaches its final 3.3-V steady state value, the open drain output of the PWRGD pin releases the TRACKIN pin, and the core supply rises at the rate of the RC time constant. The 0.1-µF capacitor is used to minimize the inrush current during startup of the core supply. The PWRGD pin asserts, pulling the TRACKIN pin low, when the SSENA pin is pulled low on the TPS54610 or when the I/O voltage is below 90% of the desired regulated voltage. Ideally, the I/O and core supplies power down in opposite order of power-up. If there is no load or a light load on the core when the I/O rail powers down, the TPS54680 device has the ability to sink current and transfers the energy stored in the output capacitor to the input capacitor. Fig. 33b shows power-down with 1-kΩ loads on both outputs.

Ratio-Metric Sequencing

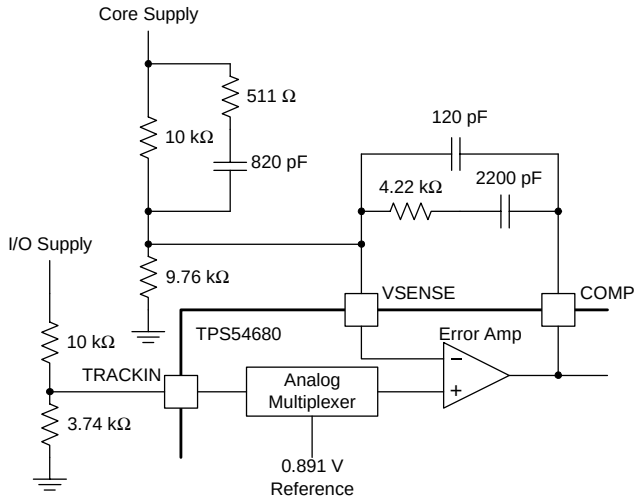
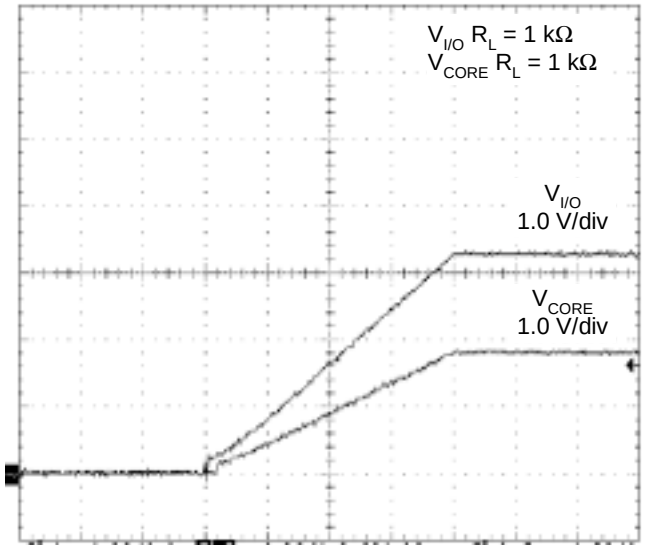
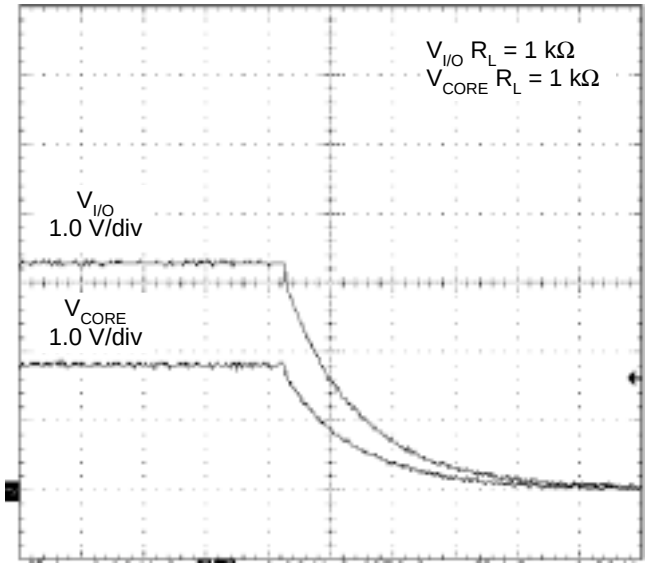


Fig. 34 Ratio-metric sequencing with TPS54680 track input.

The analog multiplexer on the TPS54680 can also provide ratio-metric power sequencing by setting the divider ratio on the TRACKIN pin to a different value than that of the feedback compensation. Fig. 34 shows a simplified schematic with the TRACKIN voltage divider set to program lower voltage than the feedback divider, resulting in the core powering-up and down in proportion to the I/O voltage. The waveforms for the core and I/O supplies are shown in Fig. 35a and 35b.



t - Time - 1.0 ms/div
(a)



t - Time - 50.0 ms/div
(b)

Fig. 35. Power-up (a) and power-down (b) waveforms of Fig. 34.

If the core supply must power up slightly before the I/O supply, the TRACKIN voltage divider ratio should be set to program higher voltage than that of the feedback divider (sample schematic and waveforms in Fig. 36 and 37). For an equation on the selection of the TRACKIN resistors see reference [10].

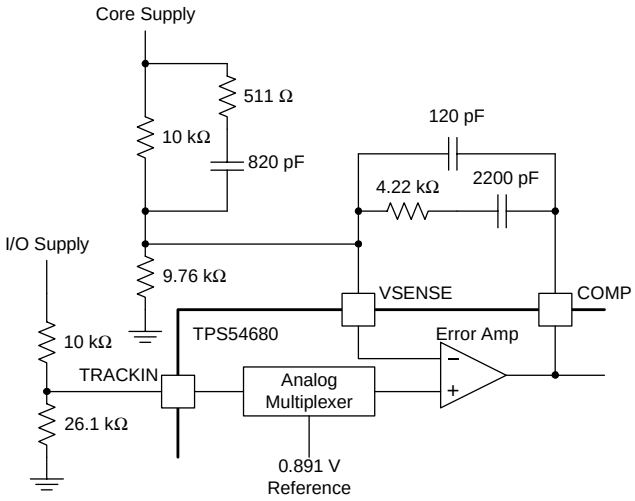


Fig. 36. Ratio-metric sequencing (core up first).

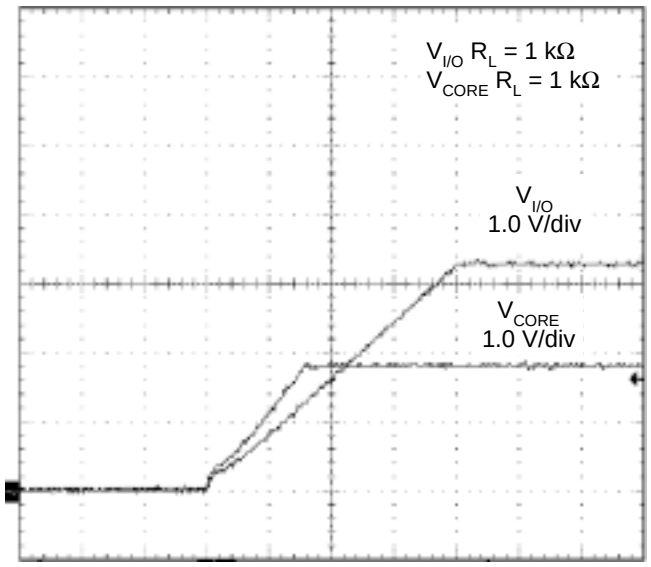


Fig. 37. Power-up (a) and power-down (b) waveforms of Fig. 36.

Simultaneous Sequencing

To minimize voltage differences between supply rails during power-up and down, the TPS54680 can be configured for simultaneous sequencing as shown in Fig. 38. By selecting the TRACKIN voltage divider to have the same ratio as the voltage divider in the feedback compensation loop, the core and I/O supplies power up and down with waveforms similar to Fig. 39. As before, the outputs of the regulators are loaded with 1-kΩ resistors. It can be observed from the waveforms that the voltage difference between the rails is minimal during power down. If the I/O supply is heavily loaded and the core supply is lightly loaded during power down, there may be a voltage difference between the rails. This is because the core supply cannot sink current as fast as the I/O supply is falling. This can be countered by adding more bulk capacitance on the I/O output.

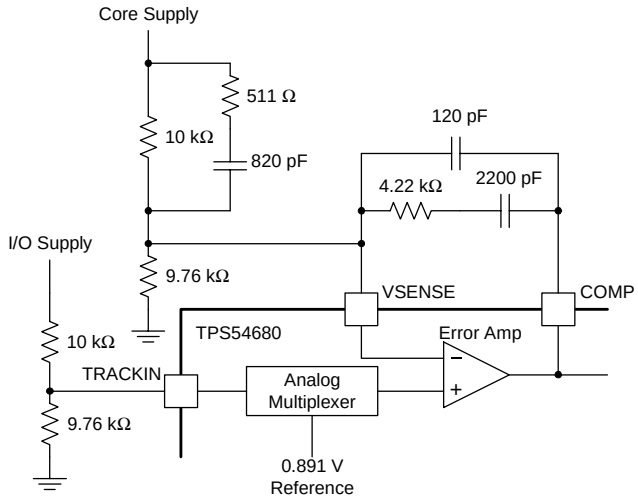


Fig. 38. Simultaneous sequencing with TPS54680 track input.

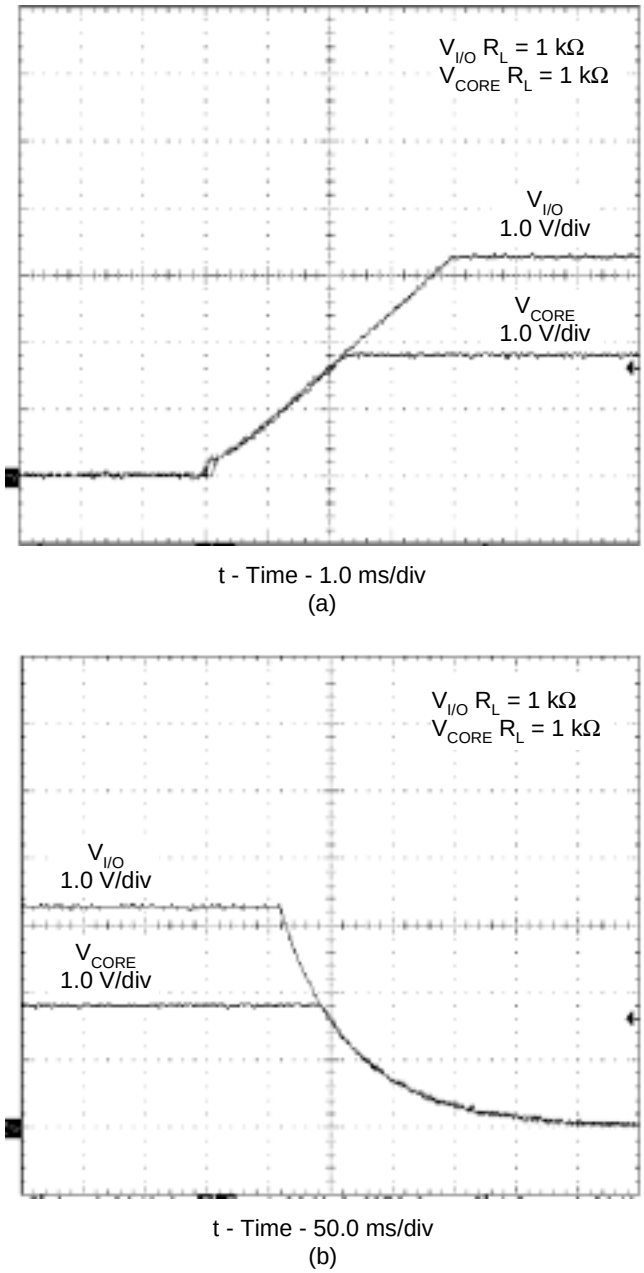


Fig. 39. Power-up (a) and power-down (b) waveforms of Fig. 38.

VI. Summary

Design of a multi-rail power system often involves much more than simply converting input voltages to output voltages and currents. As has been discussed, the power-up and power-down sequencing of these voltages can significantly impact proper system operation and reliability. Three distinct power sequencing schemes have been defined (sequential, ratio-metric and simultaneous) and implementations have been illustrated with a breadth of power devices, ranging from LDOs to PWM controllers and converters to power modules. We've also enlisted control and monitoring devices including supply voltage supervisors and a microcontroller. Of course, these devices can be applied in combination as needed to meet the power sequencing requirements of any given system.

VII. Acknowledgements

The authors wish to thank Joe DiBartolomeo and Chris Thornton for their generous contributions to this work.

REFERENCES

[1] Gray, Paul and Meyer, Robert *Analysis and Design of Analog Integrated Circuits* third edition, John Wiley & Sons, Inc., New York, 1993, Chapter 2

[2] O'Connor, Chris and Weiss, Gary, *Looking for Latch-up?*, Test & Measurement World, pages 31-34, September 2003

[3] *XC9500 CPLD Power Sequencing*, Application Note, (XAPP110) Version 1.0, February 16, 1998 Xilinx

[4] *Power Supply Sequencing Solutions for Dual Supply Voltage DSPs*, (SLVA073A), Texas Instruments

[5] Rush, Brian, *Power Supply Sequencing for Low Voltage Processors*, EDN, September 1, 2000, pp. 115-118

[6] TMS320VC5402 Data Sheet, (SPRS079E), Texas Instruments

[7] MPC8260EC/D (HiP3) Hardware Specification, Motorola, page 5, May 5, 2002

[8] TMS320VC6203B Data Sheet, (SPRS086K), Texas Instruments

[9] *Power Up Behavior of ProASIC 500 kΩ Devices*, Application Note, Actel Corporation

[10] *Sequencing with TPS54x80 and TPS54x73 DC/DC Converters*, (SLVA007), Texas Instruments

[11] TPS2140 Data Sheet, Texas Instruments (SLVS399)

[12] C.S. Mittlere, *Active Inrush Current Limiting Using MOSFETs*, Application Note, (AN1542), Motorola

[13] Power Management Reference Guide for Xilinx®, Texas Instruments (SLPB008)

[14] *Wide Range Input TPS40051 Converter Delivers 5 V at 2 Amps*, Application Note, (SLUU163), Texas Instruments

[15] *Circuit Manages Power-Up Sequencing*, Martin Galinski, Micrel Semiconductor, EDN October 2002

[16] DiBartolomeo, Joe, *Microcontroller Directs Supply Sequencing and Control*, EDN, May 29, 2003, pp. 73-74

[17] *Minimum MPC8260 PowerQUICC II System Configuration*, (AN1819), Motorola.

[18] Chris Thornton, *Auto-Track™ Voltage Sequencing Simplifies Power-Up and Power-Down*, Analog Applications Journal, (SLYT047A), Texas Instruments

[19] Chris Thornton, *New Power Modules Include Supply Voltage Sequencing and Margin Test Capabilities*, ChipCenter's Analog Avenue September 1, 2003

[20] TPS40051 Data Sheet, (SLUS540), Texas Instruments

APPENDIX A
LIST OF MATERIALS FOR FIG. 9.

Reference	Count	Description	Manufacturer	Part Number
IC1	1	LDO, 1.80 V, 1.0 A	TI	TPS79618KTT
IC2	1	LDO, 3.3 V, 1.5 A	TI	TPS78633KTT
IC3	1	SVS	TI	TPS3106K33
C1, C2	2	Capacitor, POSCAP, 100 µF, 10 V, 55 mΩ, 20%, 7343	Sanyo	10TPB100M
C3, C6	2	Capacitor, ceramic, 10 µF, 6.3 V, X5R, 20%, 1210	MuRata	GRM31CR60J106KC01
C4	1	Capacitor, ceramic, 100 nF	Std	Std
C5	1	Capacitor, ceramic, 0.47 µF	Std	Std
R1, R5	2	Resistor, chip, 100 kΩ, 1/16 W, 1%, 805	Std	Std
R2	1	Resistor, chip, 7.5 Ω, 1/16 W, 1%, 805	Std	Std
R3	1	Resistor, chip, 23.2 kΩ, 1/16 W, 1%, 805	Std	Std
R4	1	Resistor, chip, 11 kΩ, 1/16 W, 1%, 805	Std	Std
R6	1	Resistor, chip, 100 Ω, 1/16 W, 1%, 805	Std	Std
Q1	1	P-channel, FET, -12 V, -3 A, SOT-23.	Vishay	Si2333DS

APPENDIX B
LIST OF MATERIALS FOR FIG. 12.

Reference	Count	Description	Manufacturer	Part Number
IC1, IC2	2	IC, LDO Regulator, Available in 1.80-V, 2.5-V, 2.8-V, 3-V, 3.3-V and Adjustable , 1 A, ultralow noise, high PSRR, T0-263	TI	TPS79601KTT
IC3, IC4	2	Single 2.7-V High-Slew-Rate Rail-to-Rail Output Operational Amplifier w/Shutdown , SOT-23	TI	TLV2770CDGKR
CIN1, CIN2	2	Capacitor, POSCAP, 100 µF, 10 V, 55 mΩ, 20%, 805	Murata	GRM21BR60J225KC01
COUT1, COUT2	2	Capacitor, ceramic, 10 µF, 6.3 V, X5R, 20%, 805	Murata	GRM21BR60J225KC01
Q1	1	BSS 138, N-channel enhancement, SOT-23	Fairchild Semiconductor	BSS128
D2	2	Small signal diode, LL-34	Fairchild Semiconductor	1N4148
D3	1	Shottky barrier rectifiers, DPAK	On Semi-conductor	MBRD320-D
C1, C2, C3, C4, C5	5	Capacitor, ceramic, 100 nF, X7R, 10%	Std	Std
R1, R5	2	Resistor, chip, 31.6 kΩ, 1/16 W, 1%, 805	Std	Std
R2	1	Resistor, chip, 30.1 kΩ, 1/16 W, 1%, 805	Std	Std
R3	1	Resistor, chip, 300 kΩ, 1/16 W, 1%, 805	Std	Std
R4, R7	2	Resistor, chip, 4.99 kΩ, 1/16 W, 1%, 805	Std	Std
R6	1	Resistor, chip, 140 kΩ, 1/16 W, 1%, 805	Std	Std

APPENDIX C
LIST OF MATERIALS FOR FIG. 26.

Reference	Count	Description	Manufacturer	Part Number
C1, C7, C10, C1b, C7b, C10b	6	Capacitor, ceramic, 0.1 µF, 25 V, X7R, 10%, 805	Vishay	VJ0805Y104KXXAT
C11, C11b	2	Capacitor, aluminum, 100 µF, 63 V, 20%	Panasonic	EEVFK1J101P
C13, C13b	2	Capacitor, POSCAP, 330 µF, 6.3 V, 10 mΩ, 20%, 7343D	Sanyo	6TPD330M
C14, C14b	2	Capacitor, ceramic, 1 µF, 16 V, X5R, 20%, 805	TDK	C2012X5R1C105KT
C16, C16b	2	Capacitor, ceramic, 470 pF, 50 V, X5R, 20%, 805	Vishay	VJ0805Y471KXAAT
C2, C12, C17, C2b, C12b, C17b	6	Capacitor, ceramic, 2.2 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y222KXAAT
C3, C3b	2	Capacitor, ceramic, 82 pF, 50 V, NPO, 5%, 805	Panasonic	VJ0805A820KXAAT
C4, C4b	2	Capacitor, ceramic, 2.7 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y272KXAAT
C5, C5b	2	Capacitor, ceramic, 10 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y103KXAAT
C6, C6b	2	Capacitor, ceramic, 1.5 µF, 50 V, X7R, 10%, 1210	TDK	C3225X7R1H155KT
C8, C8b	2	Capacitor, ceramic, 100 pF, 50 V, X7R, 10%, 805	Vishay	VJ0805A101KXAAT
C9, C9b	2	Capacitor, ceramic, 1 µF, 16 V, X7R, 10%, 805	Vishay	C2012X5R1C105KT
D1, D1b	2	Diode, schottky, 1 A, 60 V, 45600	IR	10BQ060
D2, D2b	2	Diode, switching, 10 mA, 85 V, 350 mW, SOT-23	Vishay-Liteon	BAS16
L1, L2b	2	Inductor, SMT, 22 µH, 4.5 A, 34 mΩ, 0.85 ξ 0.59	Coiltronics	UP4B-220
Q1, Q2	2	MOSFET, dual N-channel, 60 V, 3.8 A, 55 mΩ, SO-8	Siliconix	Si946EY
R1, R1b	2	Resistor, chip, 1 kΩ, 1/10 W, 1%, 805	Std	Std
R10, R10b	2	Resistor, chip, 4.7 Ω, 1 W, 5%, 2512	Std	Std
R11, R11b	2	Resistor, chip, 20 Ω, 1/10 W, 1%, 805	Std	Std
R12, R12b	2	Resistor, chip, 243 kΩ, 1/10 W, 1%, 805	Std	Std
R13, R13b	2	Resistor, chip, 8.2 Ω, 1/10 W, 5%, 805	Std	Std
R2, R2b	2	Resistor, chip, 165 kΩ, 1/10 W, 1%, 805	Std	Std
R3	1	Resistor, chip, 2.1 kΩ, 1/10 W, 1%, 805	Std	Std
R3b	1	Resistor, chip, 4.99 kΩ, 1/10 W, 1%, 805	Std	Std
R4, R4b	2	Resistor, chip, 30.1 kΩ, 1/10 W, 1%, 805	Std	Std
R5, R5b	2	Resistor, chip, 71.5 kΩ, 1/10 W, 1%, 805	Std	Std
R6, R6b	2	Resistor, chip, 7.87 kΩ, 1/10 W, 1%, 805	Std	Std
R7, R7b	2	Resistor, chip, 100 Ω, 1/10 W, 1%, 805	Std	Std
R8, R8b	2	Resistor, chip, 3.3 Ω, 1/10 W, 5%, 805	Std	Std
R9, R9b	2	Resistor, chip, 20 kΩ, 1/10 W, 1%, 805	Std	Std
IC1, IC2	2	Wide Input Synchronous Buck Controller	TI	TPS40051PWP

APPENDIX D
LIST OF MATERIALS FOR FIG. 28

References	Count	Description	Manufacturer	Part Number
C1	1	Capacitor, aluminum, 470 µF, 6.3 V, 20%, 140CLH series, 1010	BC Components	2222 140 95301
C2, C4	2	Capacitor, ceramic, 10 µF, 6.3 V, X5R, 20%, 1206	muRata	GRM319 R6 0J 106K
C7, C8, C20, C21	4	Capacitor, ceramic, 47 µF, 6.3 V, X5R, 20%, 1210	muRata	GRM42-2 X5R 476K
C3, C14	2	Capacitor, ceramic, 39 nF, X7R, 10%, 603	Std	Std
C6, C19	2	Capacitor, ceramic, 47 nF, X7R, 10%, 603	Std	Std
C9, C11	2	Capacitor, ceramic, 470 pF, X7R, 10%, 603	Std	Std
C10	1	Capacitor, ceramic, 6.8 nF, X7R, 10%, 603	Std	Std
C12	1	Capacitor, ceramic, 1.8 nF, X7R, 10%, 603	Std	Std
C13	1	Capacitor, ceramic, 56 pF, X7R, 10%, 603	Std	Std
C5, C15	2	Capacitor, ceramic, 100 nF, X7R, 10%, 603	Std	Std
C16	1	Capacitor, ceramic, 1.5 nF, X7R, 10%, 603	Std	Std
C17	1	Capacitor, ceramic, 18 nF, X7R, 10%, 603	Std	Std
C18	1	Capacitor, ceramic, 5.6 nF, X7R, 10%, 603	Std	Std
R1	1	Resistor, chip, 76.8 kΩ, 1/16 W, 1%, 603	Std	Std
R2	1	Resistor, chip, 3.83 kΩ, 1/16 W, 1%, 603	Std	Std
R3	1	Resistor, chip, 40.2 kΩ, 1/16 W, 1%, 603	Std	Std
R4, R5	2	Resistor, chip, 330 kΩ, 1/16 W, 1%, 603	Std	Std
R6	1	Resistor, chip, 13.7 kΩ, 1/16 W, 1%, 603	Std	Std
R7	1	Resistor, chip, 105 Ω, 1/16 W, 1%, 603	Std	Std
R8	1	Resistor, chip, 27.4 kΩ, 1/16 W, 1%, 603	Std	Std
R9	1	Resistor, chip, 1 kΩ, 1/16 W, 1%, 603	Std	Std
R10	1	Resistor, chip, 71.5 kΩ, 1/16 W, 1%, 603	Std	Std
R11	1	Resistor, chip, 1.43 kΩ, 1/16 W, 1%, 603	Std	Std
R12	1	Resistor, chip, 14.7 kΩ, 1/16 W, 1%, 603	Std	Std
R13	1	Resistor, chip, 33.2 Ω, 1/16 W, 1%, 603	Std	Std
R14	1	Resistor, chip, 10 kΩ, 1/16 W, 1%, 603	Std	Std
IC1	1	Low Input Voltage 3-A Buck Converter, PWP	TI	TPS54310PWP
IC2	1	Low Input Voltage 6-A Buck Converter, PWP	TI	TPS54610PWP
Q1	1	Bipolar Small Signal, NPN, 50 V, 22 mA, 3.5 Ω, SOT-23	Infineon	BSS138
D1	1	Diode, 100 V, 200 mA, SOT-23	Fairchild	MMBD4148
L1, L2	2	Inductor, CEP125, 7.2 µH, 7.8 A, 14 mΩ, 12.5x12.5 mm	Sumida	CEP125-H-7R2

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