Thermal Considerations for Surface Mount Layouts

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ABSTRACT

The focus of this paper is to present the techniques that are effective in removing the heat from the surface mounted power ICs and transferring it to the cooler surroundings. In the past the thermal design was as simple as adding the theta values (°C/W) of the power component, the pad and the heat sink together and multiplying by the power dissipated in that component to arrive at the temperature rise between the ambient and the junction of the IC. Today, with surface mount technology and ICs with power pads the Printed Circuit Board (PCB) has become an integral part for removing the heat. Every PCB is different and the task of mathematically deriving a temperature profile for the PCB and each power component is beyond the scope of this paper. However the basic concepts of what makes a good thermally conductive PCB, some first order modeling examples and evaluations of an existing EVM will help the designer understand the techniques in producing a good thermally conductive PCB.

There are three basic methods to move heat away from the source, conduction, convection and radiation heat transfer. Conduction is moving the heat through a material (PCB) typically from copper to FR4 to copper and so on. Convection is for removing the heat off the surface material to the air. Radiation is for moving the heat from one surface material to another through air.

I. HEAT TRANSFER BY CONDUCTION

Conduction is important because it is the surface area that eventually dissipates the heat and only through conduction does the heat spread out to the required surface area. The trend is to migrate toward smaller packages believing that the design area can be reduced. The reality is that a smaller footprint, with the same power dissipation, requires a better PCB conduction design and a similar amount of surface area, for a given temperature rise.

Heat conduction is better through some materials (Copper) than others (FR4). Table 1 shows the thermal conductivity factor K for different materials. These common materials have significant different thermal conductivity factors. The units are Watts per meter-Kelvin (W/m°K) or Watts per meter-Celcius (W/m°C). Since the temperature is a temperature rise (dT) the 273.15 offset between K and C drops out.

TABLE 1 THERMAL CONDUCTIVITY FACTORS

Materials	K (W/m°K)	K (W/in°C)
Copper	355	9
Aluminum	175	4.44
FR4	0.25	0.0064
Solder 63/67	39	1
Air	0.0275	0.0007

At first glance at the units, it appears that one would multiply the Thermal Conductivity Factor by the thermal path length to get W/°C (1/θ), but this is not correct since this would indicate the longer the thermal path the larger the heat transfer factor. The correct method is to divide K by the thermal path length which results in the units, W/in^2°C. Next multiplying by the cross sectional surface area of the thermal path yields W/°C or 1/θ.

A. *Formulas For Conduction*

1. *General Conduction Formula*

The general conduction formula for thermal impedance for a given material is:

$$\theta = \frac{L}{K \bullet A_{CS}} \quad (1)$$

Where

- K is the Thermal Conductivity Factor
- L is the thermal path length
- A_{CS} is the cross sectional area where the heat is being applied

A low theta is desired since this is the temperature rise in °C per Watt of heat dissipated.

2. *Lateral Conduction Heat Flow Formula*

Fig. 1 shows the lateral conduction heat flow along a plane. The thermal impedance for the lateral heat flow is given by

$$\theta = \frac{L}{K \bullet W \bullet t} = \frac{L}{K \bullet A_{CS}} \quad (2)$$

where

- L is the path length of the heat flow
- W is the width and t is the thickness
- $W \bullet t = A_{CS}$, area-cross section of heat flow,

$$\theta = \frac{1}{K \bullet t} \quad (3)$$

where

- for a square area L=W

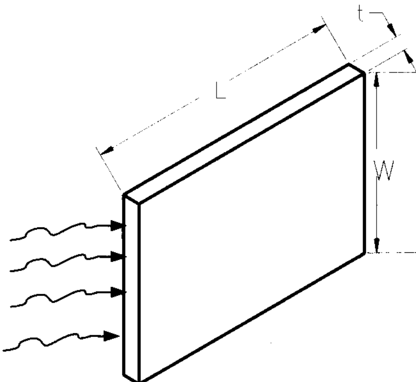


Fig. 1. Lateral conduction heat flow along the length of a plane.

- Thermal Impedance, θ, for lateral conduction, for a square of 1–oz. Cu is:

$$\theta_{sq-1oz-Cu} = \frac{1}{9W/(in-C) \cdot 0.0014 in} = 79.4°C/W \quad (4)$$

"1-oz. Cu" is 1 ounce of copper spread over 1 square ft of area. (1 oz. is the equivalent to 1.14 mil thickness of Copper: which is also eqivalent 310 grams of Copper per square meter.

- Thermal Impedance, θ, for lateral conduction, for a square of 0.06" thick FR4 is:

$$\theta_{sq-0.060-FR4} = \frac{1}{0.0064 W/(in-C) \cdot 0.060 in} = 2620°C/W \quad (5)$$

It shows that the copper plane has much better thermal impedance than FR4.

3. *Perpendicular Conduction Heat Flow Formulas*

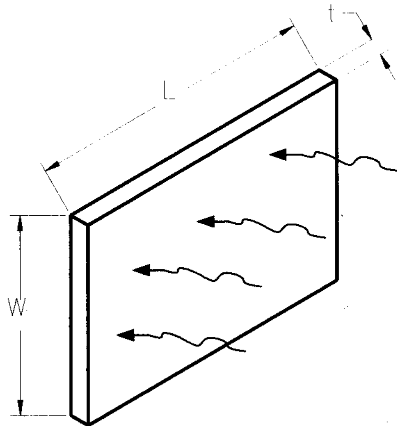


Fig. 2. Perpendicular conduction heat flow through a plane.

Fig. 2 shows the perpendicular conduction heat flow through a plane. The thermal impedance is given by:

$$\theta = \frac{t}{K \bullet W \bullet L} = \frac{t}{K \bullet A_{CS}} \tag{6}$$

where

- t is the path of heat flow (the heat flows through the thickness of the material)
- W•L is the cross sectional area where the heat is being applied, A_{CS}
- Thermal Impedance, θ, for perpendicular conduction, for a 1 in^2 of copper, 2 oz, is:

$$\theta_{2oz_Cu_1in^2} = \frac{0.0028 in}{9W/(in-C) \bullet 1 in^2} = 0.0003^{o} C/W \tag{7}$$

- Thermal Impedance, θ, for perpendicular conduction, for a 1 in^2 of FR4, 60m, is:

$$\theta_{0.06in-FR4_1in^2} = \frac{0.060\ in}{0.0064\ W/(in-C) \bullet 1\ in^2} = 9.4°C/W \tag{8}$$

4. *Heat Flow Through a Via Formula*

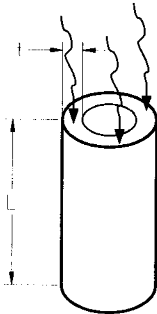


Fig. 3. Vertical conduction heat flow through a via.

Fig. 3 shows the vertical conduction heat flow through a cylinder via. Its thermal impedance is given by

$$\theta_{Cu-Via} = \frac{L}{K \bullet A_{CS}} = \frac{L}{K \bullet \pi \bullet \frac{(D_0^2 - D_1^2)}{4}} \tag{9}$$

where

- L is the length of the via (the heat flows through the length of the cylinder)
- $\pi \bullet \frac{(D_0^2 - D_1^2)}{4}$ is the cross sectional area,

Substituting L=0.06 in., K=9 W/(in-C), D_0=0.016 in., and D_1=0.013 in into the above equation yields 97.6°C/W for a copper via.

For a solder filled via, the thermal impedance for the "solder plug" is given

$$\theta_{Solder-via} = \frac{L}{K \bullet A_{CS}} = \frac{L}{K \bullet \pi \bullet \frac{D_1^2}{4}} \tag{10}$$

Substituting L=0.06 in, K=1 W/(in-C), and D_1=0.013 in provides 452°C/W.

5. *Conduction Through Solder Mask Formula*

$$\theta_{Solder-Mask} = \frac{L}{K \bullet A_{CS}} \tag{11}$$

Where K= 0.0075 W/in- C and L=1 mil.

The very thin sheet along with a large area result in a 0.133 C/W rise for 1 $in.^2$ of surface area. This small temperature change is typically ignored.

B. *Thermal Conduction Concepts*

1. *Concept 1: A Shorter Thermal Path Has a Lower Theta*

For a given material the shorter the thermal path the better. It is more efficient to conduct heat through the plane's thickness rather than along its length.

An example of short and long heat transfer paths using FR4 is shown below.

Example: Heat transfer through FR4, thickness 0.060 in:

$$\theta_{0.06in-FR4} \bullet Acs = \frac{t}{K} = \frac{0.060\, in}{0.0064\, W/(in-C)} \approx 10^{o} C \bullet in^2 / W \tag{12}$$

This implies that a 10°C drop over 1 in^2 conducts 1 W)

Example: Heat transfer along 1 in of 0.060in FR4 layer:

$$\theta_{1in-FR4} \bullet Acs = \frac{L}{K} = \frac{1\,in}{0.0064W/(in-C)} = 156°C \bullet in^2 / W \quad (13)$$

This implies that it conducts only 3.8 mW with 10°C rise for a 1 in. wide by 0.060 in. thick FR4

a. Conclusion – Short Thermal Path, FR4

FR4 is a fairly good thermal conductor (relative to air) through thin layers (perpendicular conduction) but not along the length of the plane's layer (lateral conduction).

An example of short and long heat transfer paths using Copper is shown below.

Example: Heat transfer through 2 oz. Cu (t=2.8 mils):

$$\theta_{2oz-Cu} \bullet Acs = \frac{t}{K} = \frac{0.0028\,in}{9W/(in-C)} = 0.000311°C \bullet in^2 / W \quad (14)$$

can assume perfect heat transfer.

Example: Heat transfer along 1 in of 2-oz. Cu

$$\theta_{1in-Cu} \bullet Acs = \frac{L}{K} = \frac{1\,in}{9W/(in-C)} = 0.11°C \bullet in^2 / W \quad (15)$$

This implies that for a 10°C drop over 1-in. wide and 0.0028-in thick conducts 25 mW.

b. Conclusion – Short Thermal Path, Cu

Copper is an excellent thermal conductor through the 2-oz. thick layer and is a good thermal conductor along its length for a large cross-section, (W•t). At least one full copper layer is needed to spread the heat.

2. Concept 2: A Larger Connection (Area / Perimeter) Between IC & PCB Has a Lower theta

The larger the perimeter of the power pad (circumference), the greater the cross-sectional thermal conduction area, the lower the PCB's Theta and the cooler the PCB and IC.

As A_{CS} (circumference around the power pad times copper thickness) decreases the Theta increases. Therefore selecting a smaller part decreases the circumference and results in a higher Theta. To compensate for this change one can increase the copper thickness, which increases the cross-sectional thermal conduction area and reduces the Theta.

An analogy to heat flow is water flow. Consider a pump which outputs a constant water flow rate (5 gal/min), through a ½-in diameter, 1-ft pipe with a ¾-in coupler on the end. A ½-in diameter garden hose is connected to the ¾-in coupler and the pressure dropped is observed across the coupler. Since two ½-in pipes are connected together with a ¾-in connection, there is no measurable pressure drop observed.

The ¾-in coupler is replaced with a ¼-in coupler and the pressure drop observed. As one could imagine, the pump had to dramatically increase its output pressure to get the same flow through the smaller coupler connection. This change in pressure is analogist to the temperature change, and where the constant flow rate is analogist to the constant power dissipation.

One can see that a better connection (larger A_{CS}) to a source, the better the flow from the source.

$$\theta = \frac{L}{K \bullet W \bullet t} = \frac{L}{K \bullet A_{CS}} \quad (16)$$

3. Concept 3: Use Thick Copper and Thin FR4 Layers

Heat conducts through a FR4 layer more efficiently than through air, so FR4 is still relatively a good heat conductor; therefore to maximize heat flow through FR4, minimize the thickness if possible.

Copper is 9/0.0064≈1400 times the thermal conductor as FR4. For copper, a thicker layer helps the heat conduction along the length of the plane but the does not significantly impede the heat transferred through the thickness of the copper layer. Therefore use a thick layer of copper to maximize the heat flow along the copper sheet (2 oz. is great for most power designs).

4. *Concept 4: Use Multiple Vias to lower the Theta through the PCB (FR4)*

Copper is nine times better thermal conductor than 63/37 solder, and solder is 157 times better than FR4. Consider the effects of using multiple solder filled vias.

Example: Heat Transfer through 60m - FR4, under IC (Pad Area, 0.08"x0.12"), with no Vias

$$\theta_{60m-FR4-IC} = \frac{9.4°C/W - in^2}{A_{CS}} = \frac{9.4°C/W - in^2}{2mm \times 3mm}\left(\frac{mm}{0.040in}\right)^2 = 979°C/W \quad (17)$$

Example: Heat transfer through a Cu thermal via, D=0.016", D0=0.013", L=0.06"

$$\theta_{Cu} = \frac{L}{K \bullet A_{CS}} = \frac{L}{K \cdot \pi \cdot \frac{D_0^2 - D_1^2}{4}} = \frac{0.06in}{9W/(in-C) \bullet \pi \bullet \frac{(0.016in)^2 \bullet (0.013in)^2}{4}} = 97.6°C/W \quad (18)$$

Example: Heat transfer through solder portion of via,

$$\theta_{Solder} = \frac{t}{K \bullet \pi \bullet \frac{D^2}{4}} = \frac{0.06in}{\frac{1W}{in-C} \bullet \pi \bullet \frac{0.013^2}{4} in^2} = 452°C/W \quad (19)$$

Example: Heat Transfer for Solder Filled Vias

$$\theta_{Cu-Solder} = \frac{1}{\frac{1}{\theta_{Cu}} + \frac{1}{\theta_{Solder}}} = 80.3°C/W \quad (20)$$

Combined they result in θ Cu/solder = 80.3°C/W.

a. *Conclusion – Use Multiple Vias*

Solder and copper greatly enhance thermal performance of the FR4. Solder is less conductive but often has a larger cross sectional area so it can improve thermal conductivity significantly. Multiple vias further lower the Theta value.

II. HEAT TRANSFER BY CONVECTION

Convection is the method of moving heat from the surface of a material to the air. The temperature rise is a function of the power dissipated and inversely proportional to the surface area and the heat transfer coefficient, h. The heat transfer coefficient, h, is a function of air speed and temperature difference. The range is 7.8 (10°C rise) to 9.1 mW/(in2-C) (60°C rise), for no air flow. A conservative value for h is 7.5 mW/(in2-C) for no air flow.

A. *Convection Formulas*

1. *The temperature rise through convection is given by*

$$dT = \frac{P}{h \bullet A} = 133\frac{P}{A} \quad (21)$$

where

- P is in Watts
- h is 0.0075 W/(in^2-C)
- A is surface area, in^2.

So the thermal impedance is given by

2. *The Theta for Convection is given by*

$$\theta_{Surface-area} = \frac{1}{A \bullet h} = \frac{133(°C - in^2/W)}{A(in^2)} \quad (22)$$

3. *Minimum PCB Surface Area need for a given temperature rise, from TAMB to TPCB-MIN.*

$$A = \frac{P}{h \bullet dT} = 133\frac{P}{dT} \quad (23)$$

4. Junction Temperature is given by

$$T_J = T_{AMB} + dT_{PCB-Conv} + dT_{PCB-Cond} + dT_{JC_IC} \quad (24)$$

B. Convection Concepts

1. Concept 5: Convection is a Function of ΔT and Area, not the Material

The heat transfer off of a surface is related to the temperature difference between the ambient air and the surface of the material and the air flow, but not the material itself. This at first seems like an error because Copper is a better conductor than FR4. Copper is a better conductor than FR4, but both have the same heat dissipation factor for Convection.

<u>*Example :*</u> <u>Convection vs Conduction</u>

Consider a sheet of copper and a sheet of FR4 with the same dimensions (10 in × 10 in × 1 in). Each sheet is placed on top of a perfectly insulated box (sides and bottom) with a 10W heat source placed in each box. The ambient temperature is 25°C and the lid (top sheet) is allowed to reach its steady state temperature.

The top surface temperature, by convection, of each material (FR4 or Copper) is:

$$T_{EXT_SURFACE}$$
$$= 25°C + 133°C/W - in^2 \times 10W \times 100\, in^2 \quad (25)$$
$$= 38.3°C$$

Both external surfaces are the same temperature and dissipate the same amount of heat.

For conduction, the thermal conductivity factor is different for different materials and the temperature change for given shape and power dissipation will be different.

The temperature change from the external surface to internal surface, due to conduction, is:

$$T_{Rise-Cu} = \frac{10W}{\left(100\text{ in}^2 \times 9\text{ W/in}^2\right)\text{-}°\text{C}} \quad (26)$$
$$= 0.011°\text{C}$$

$$T_{Rise-FR4} = \frac{10W}{\left(100\text{ in}^2 \times 0.0064\text{ W/in}^2\right)\text{-}°\text{C}} \quad (27)$$
$$= 15.6°\text{C}$$

The interior surface temperatures are:

$$T_{INT-Cu} = T_{RISE-Cu} + T_{EXT-SURFACE}$$
$$= 0.011°C + 38.3°C \quad (28)$$
$$= 38.311°C$$

$$T_{INT-FR4} = T_{RISE-FR4} + T_{EXT-SURFACE}$$
$$= 15.6°C + 38.3°C \quad (29)$$
$$= 53.9°C$$

The concept of having the same external surface temperature, for Copper and FR4, is more easily accepted knowing the internal surface temperature of the FR4 is much higher than that of the copper, for a given power dissipation.

With 1.5 ft/sec of air flow, h can double and lower the temperature rise due to convection by half. Calculating h for the non linear air flow patterns is complex and not explored in this paper. For Portable Power, often the PCB are enclosed and in an environment where there is no air flow.

C. PCB Area Estimate for Typical Design

How much board surface area is needed for a design? A typical example is a power component (θ_{JC} of 7°C/W, T_J-125°C) dissipating 2 W with a maximum ambient of 50°C. How much area is needed to keep the junction temperature from exceeding it maximum temperature? Start with the maximum junction temperature and subtract off the temperature rise across the IC, PCB and maximum ambient temperature, the remainder is the allowable temperature rise allowed due to convection.

The temperature rise across the IC-θ_{JC} is

$$T_{JC(\max)} = P_{DISS} \times \theta_{JC}$$
$$= 2W \bullet 7°C/W = 14°C \quad (30)$$

A conservative estimate for theta, due to conduction, across the PCB is 20°C/W. The temperature rise across the PCB is

$$T_{PCB(\max)} = P_{DISS} \times \theta_{PCB-Cond}$$
$$= 2W \bullet 20°C/W = 40°C \quad (31)$$

The dT between ambient and the PCB surface is:

$$dT_{PCB-Conv(\max)}$$
$$= T_{J(\max)} - T_{JC(\max)} - T_{PCB(\max)} - T_{AMB(\max)} \quad (32)$$
$$= 125°C - 14°C - 40°C - 50°C = 21°C$$

The surface area needed is:

$$A = \frac{133P}{dT} = 133 in^2\,°C/W \bullet \frac{2W}{21°C} = 12.7\ in^2 \quad (33)$$

A 2.5 in. by 2.5 in. PCB gives 12.7 in^2 of surface area.

III. Heat Transfer By Thermal Radiation

Thermal Radiation is the transfer of heat from one surface to another. It is based off of the Stefan-Boltzman Law of Radiation equation and is given by

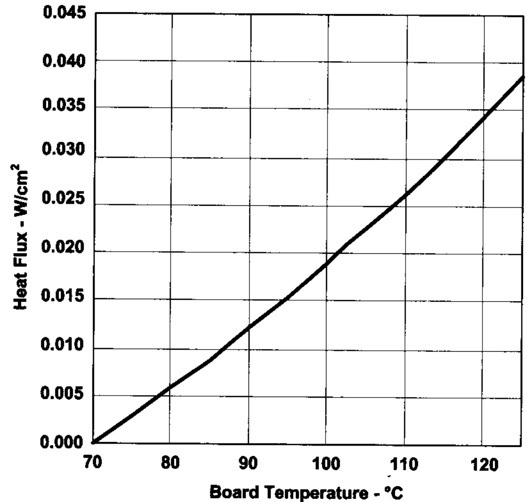
$$H = e\sigma A T_1^4 - T_2^4 \quad (34)$$

where

- e = emissivity (0-1).
- $T_{°K}$ = Kelvin temperature
- σ=Stefan-Boltzmann constant (see Equation 17)

$$5.67 \bullet 10^{-8} \bullet \frac{J}{\left(s - m^2 \bullet K^4\right)} \quad (35)$$

Plots were generated based on the thermal radiation, in Watts/area, versus surface temperature, of the radiator, and are shown in Fig. 4.



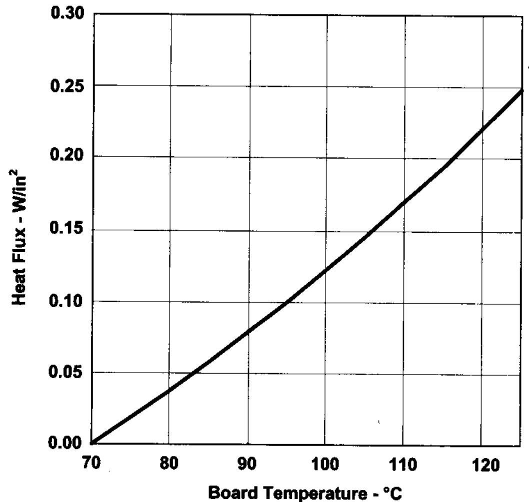


Fig. 4. Thermal Surface Radiation

The plots are fairly linear due to the small change in surface temperature compared to the large temperature values in °K. It turns out that the heat transfer due to radiation, assuming that the radiating surface temperature is greater than the ambient temperature, is approximately ½ the amount of heat transferred by convection. The heat transfer contribution by Thermal Radiation is often ignored in any analysis, due to its added complexity, but may be considered as a margin of safety in the thermal design.

IV. Is There An Easy Modeling Approach?

Modeling can be very complex since no two PCB designs are exactly the same. The temperature and power dissipation gradients are non linear and is beyond the scope of this article to create and integrate a formula to accurately predict temperature rise, for power dissipation of multiple ICs. However a generic model has been created with a matrix of series and parallel resistors to simulate temperature rise through and along the PCB layers for various size boards for a single power IC. The resistor values are determined from the conduction and convection formulas and represent the theta values for small circular rings, 0.1 in. wide for both Copper and FR4. The radius of each consecutive ring is 0.1 in. larger The larger the radius the longer the circumference and the more 0.1 in. squares there are per ring, thus lowering the theta.

The theta value for conduction through 2-oz. thick copper is assumed zero where the theta value along the length of the FR4 plane is assumed infinite. The heat transfer is restricted or limited by the PCB materials (theta values) represented by resistors, the heat flow (Watts) is modeled by the current and voltage drops represent change in temperature (dT).

Fig. 5 is the thermal model for a 2-layer, 1-oz., 60-mil PCB with an IC that dissipates 3 W. The 3-A current source represents the 3 W power dissipation of the IC. The two horizontal rows of resistors represent the top and bottom copper planes. Each resistor, from left to right, represents the conduction horizontally along the copper layer, starting at the IC's perimeter, for a 0.1 in. radius, and heading outward in a circular pattern. As the 0.1-in, "band", circular rings get further from the IC, the circumference increases and so does the number of *squares* of copper. This explains the continual drop in theta values as the radius increases from the IC.

This model has 20 horizontal resistors representing 20, 0.1-in. circular rings (or a radius of 2 in. from the heat source (power IC)). The center row of vertical resistors (circular rings) represent the thermal resistance through the FR4 (PCB) from one Copper surface to the other. The top and bottom row of vertical resistor represent the theta values for the convection off of the surface, of the PCB, into the air. The ground potential represents the air temperature. The voltage rises from the ground toward the 3-A current source represent the temperature rises above ambient. As mentioned earlier, there is negligible temperature rise through the thickness of the copper layer, so the 0-Ω resistors are not shown. The horizontal resistors for conduction in the FR4 plane are very large and are in parallel with the small copper horizontal resistors and thus are omitted.

Table 1 is a quick reference chart for the theta value of a single via given its finished hole diameter and the board thickness. The effective theta value can be reduced by a factor of n by adding n number of vias to the PCB.

TABLE 1. THETA VALUES

	Board Thickness															
	0.03		0.04.		0.05		0.06		0.07		0.08		0.09		0.1	
Filled Vias	N	Y	N	Y	N	Y	N	Y	N	Y	N	Y	N	Y	N	Y
0.01	61.5	53.1	82.0	70.7	102.5	88.4	123.0	106.1	143.5	123.8	164.0	141.5	184.5	159.2	205.0	176.8
0.013	48.8	40.2	65.0	53.6	81.3	67.0	97.6	80.4	113.8	93.8	130.1	107.2	146.3	120.6	162.6	134.0
0.016	40.4	31.9	53.9	42.5	67.4	53.1	80.8	63.7	94.3	74.4	107.8	85.0	121.3	95.6	134.7	106.2
0.019	34.5	26.1	46.0	34.8	57.5	43.5	69.0	52.2	80.5	60.9	92.0	69.6	103.5	78.3	115.0	86.9
0.022	30.1	21.8	40.1	29.1	50.2	36.4	60.2	43.7	70.2	51.0	80.3	58.3	90.3	65.5	100.3	72.8
0.025	26.7	18.6	35.6	24.8	44.5	31.1	53.4	37.3	62.3	43.5	71.2	49.7	80.1	55.9	89.0	62.1
0.028	24.0	16.1	32.0	21.5	40.0	26.9	48.0	32.2	55.9	37.6	63.9	43.0	71.9	48.4	79.9	53.7
0.031	21.8	14.1	29.0	18.8	36.3	23.5	43.5	28.2	50.8	32.9	58.0	37.6	65.3	42.3	72.5	47.0
0.034	19.9	12.5	26.6	16.6	33.2	20.8	39.9	25.0	46.5	29.1	53.1	33.3	59.8	37.4	66.4	41.6
0.037	18.4	11.1	24.5	14.8	30.6	18.5	36.7	22.2	42.9	26.0	49.0	29.7	55.1	33.4	61.2	37.1
0.04	17.0	10.0	22.7	13.3	28.4	16.6	34.1	20.0	39.8	23.3	45.5	26.6	51.1	30.0	56.8	33.3
0.043	15.9	9.0	21.2	12.0	26.5	15.0	31.8	18.0	37.1	21.1	42.4	24.1	47.7	27.1	53.0	30.1
0.046	14.9	8.2	19.9	10.9	24.8	13.7	29.8	16.4	34.7	19.1	39.7	21.9	44.7	24.6	49.6	27.3
0.049	14.0	7.5	18.7	10.0	23.3	12.5	28.0	15.0	32.7	17.5	37.4	20.0	42.0	22.5	46.7	24.9
0.052	13.2	6.9	17.6	9.2	22.0	11.4	26.4	13.7	30.9	16.0	35.3	18.3	39.7	20.6	44.1	22.9
0.055	12.5	6.3	16.7	8.4	20.9	10.5	25.0	12.6	29.2	14.7	33.4	16.8	37.6	19.0	41.7	21.1
0.058	11.9	5.8	15.9	7.8	19.8	9.7	23.8	11.7	27.7	13.6	31.7	15.6	35.7	17.5	39.6	19.5
0.061	11.3	5.4	15.1	7.2	18.9	9.0	22.6	10.8	26.4	12.6	30.2	14.4	34.0	16.2	37.7	18.0
0.064	10.8	5.0	14.4	6.7	18.0	8.4	21.6	10.1	25.2	11.7	28.8	13.4	32.4	15.1	36.0	16.8
0.067	10.3	4.7	13.8	6.3	17.2	7.8	20.7	9.4	24.1	10.9	27.5	12.5	31.0	14.1	34.4	15.6
0.07	9.9	4.4	13.2	5.8	16.5	7.3	19.8	8.8	23.1	10.2	26.4	11.7	29.7	13.2	33.0	14.6
0.073	9.5	4.1	12.7	5.5	15.8	6.8	19.0	8.2	22.2	9.6	25.3	11.0	28.5	12.3	31.6	13.7

Fig. 6 is the temperature *RISE* profile plot for a 3-W, 2-layer, 1-oz. Cu, 60-mil FR4 PCB. There are two sets of curves. The top set is for a board that has a 1 in. radius around the part similar to a 2 in × 2 in PCB. The lower set of curves is for a radius of 2 in. or a 4 in. × 4 in. PCB. The difference between the 1-in. and 2-in. radius models is that for the 1-in. model the horizontal resistors at the 1-in. radius are made very large, effectively cutting off heat transfer to the rest of the PWB. Note that for a given power dissipation and board size that the PCB's temperature tapers to a steady state base line temperature toward the outer part of the PCB.

The smaller PCB reaches a higher "base" temperature. Notice how the temperature rises faster as the distance to the IC is reduced. The sets of curves also fan out close to the part. The curves that ramp up to a higher temperature are the ones with isolated connections on the top layer. For the totally isolated power pad the top surface temperature drops rapidly toward the average base line temperature of the PCB. This fits well with the analogy about the larger water pressure changes for smaller connections to the source. The plot also shows how the top and bottom surface layer temperatures merge as the distance from the IC increases. This is the result of the lower FR4 theta value, due to the increased material area, as the distance from the power IC is increased.

Fig. 5. Theta model for 3-W, 2-layer, 1-oz., Cu, 60 mil FR4 PCB (for Figure 2 plot)

This model is a first order effect and does not account for air flow or board orientation so in reality, for a horizontal board the thetas would be slightly lower making the top of the board 1 to 3°C cooler. Also if the board is vertical, both surfaces are a couple of degrees cooler. This model is however fairly close to an enclosed application where there is no air flow and orientation becomes less of a factor.

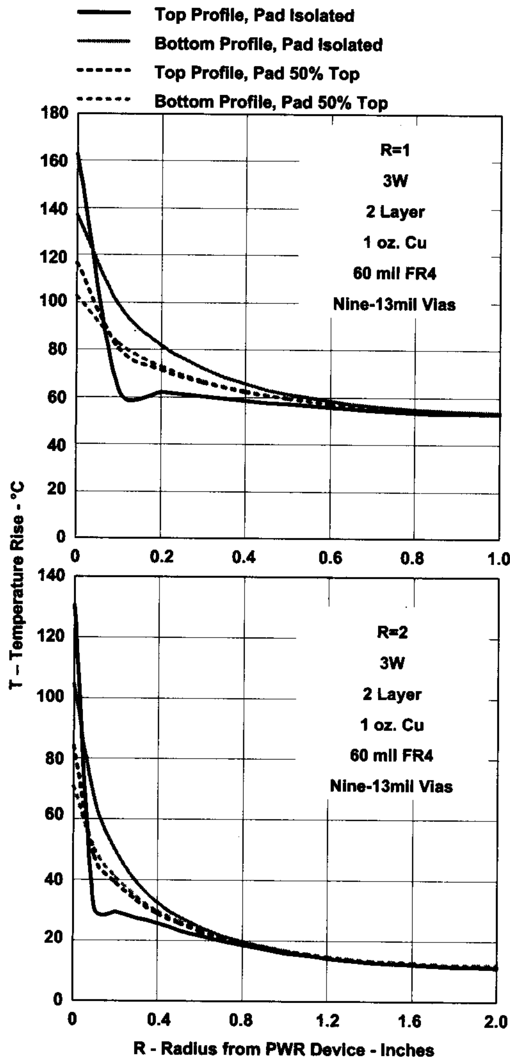


Fig. 6. PCB temperature profile, 3-W, 2-layer, 1-oz., Cu, 60 mil FR4, nine-13 mil vias.

Fig. 7 is similar to Fig. 6 except that it uses 2-oz. Copper. Note how the base line temperature is the same verifying that the temperature is a function of board area and not Copper thickness. The temperature profile close to the IC is much better for the 2-oz. case which again supports the theory that a good connection to the heat source is vital.

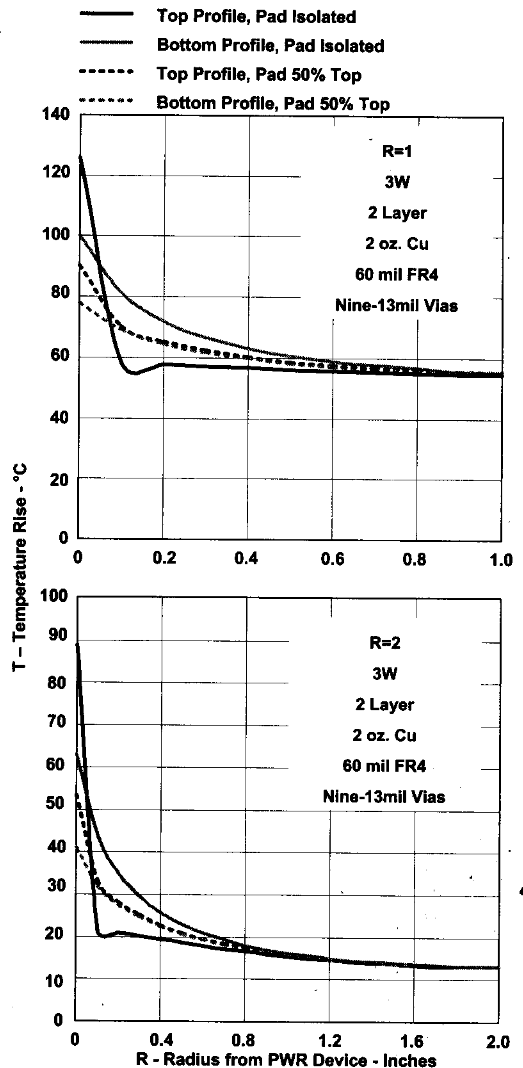


Fig 7. PCB temperature profile, 3-W, 2-layer, 2-oz., Cu, 60 mil FR4, nine-13mil vias.

The difference between Fig. 8 and Fig. 7 is that the FR4 is half as thick. Once again the base temperatures are the same and the connection between the IC and board has improved since the vias and FR4 are half the thickness and half the theta value. The result is half the temperature rise perpendicular through the PCB, near the IC.

Fig. 9 is a model of a 4 layer PCB and therefore has two extra copper layers and two extra FR4 layers. Note that when a Copper layer is isolated, from the IC, or the board radius is reduced the theta value at that location is effectively removed by placing a series of 9s in front of the value. This allows quick changes between simulations.

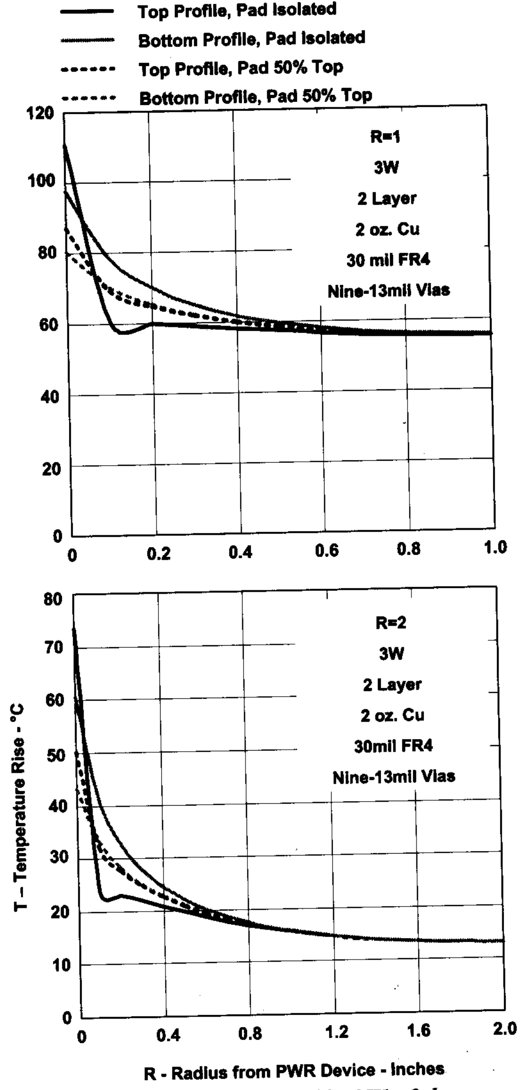


Fig. 8. PCB temperature profile-3W, 2-layer, 2-oz. Cu, 30 mil FR4, nine-13 mil vias.

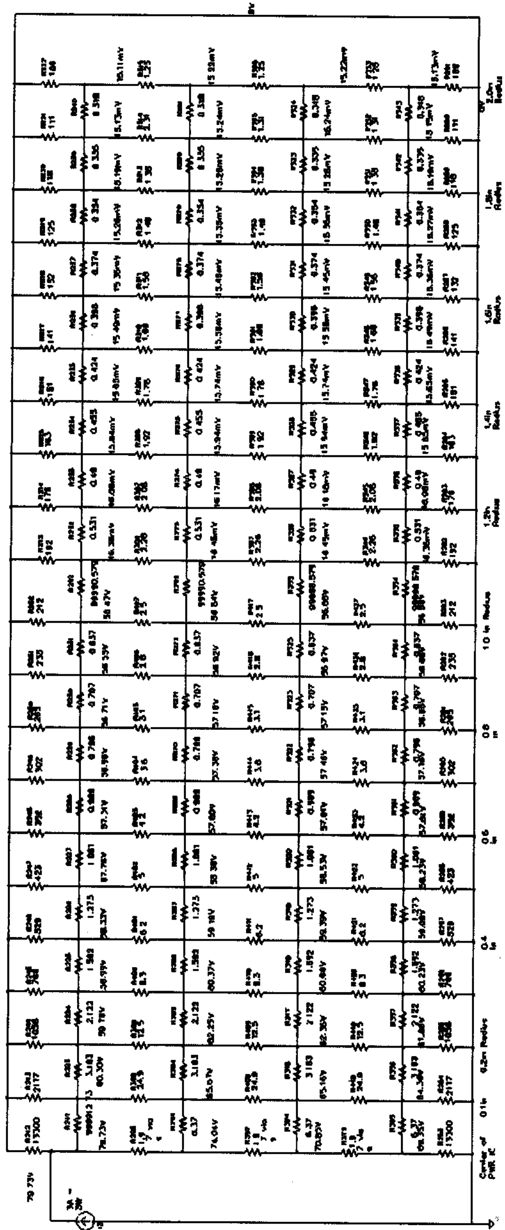


Fig. 9 Theta model for 3-W, 4-layer, 2-oz. Cu, 30 mil FR4 PCB (for Fig. 10 plot)

The difference between Fig. 10 and Fig. 8 is that Fig. 10 has four layers. Once again, the base temperatures are the same for a give surface area. Also there is at least twice the copper connection near the IC reducing the temperature rise. The extra curve to the right end of traces represents the base line temperature for the PCB ranging from approximately 1.4 in. per side to 4 in. (2 in. radius) per side. For a 3-W dissipation, a PCB smaller than 2-in. per side (1-in. radius) has a difficult time dissipating its heat and is very unlikely to keep the junction temperatures, of the IC, under its maximum rating.

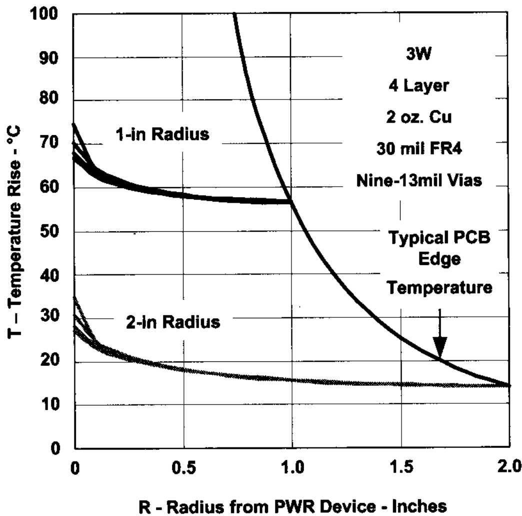


Fig. 10. PCB temperature profile-3W, 4-layer, 2-oz. Cu, 30 mil FR4, nine-13 mil vias.

Fig. 11 shows the temperature profile of an EVM and its Model Data. The ambient temperature of 25°C was added to the model data which is in °C temperature rise above ambient. The PCB of the EVM is approximately 2.1 in. × 2.3 in., has four 2-oz. copper layers, two of which connect to the IC through 6-13 m vias, one routing layer with no copper connection to the IC and the top layer that has a 60% connection to the IC's power pad.

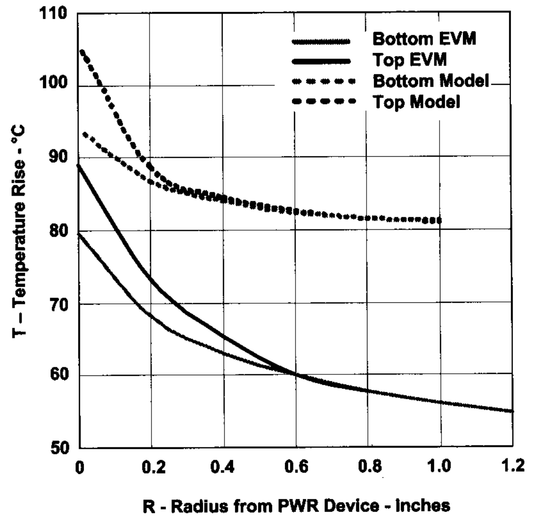


Fig. 11. Temperature profile of bq24032 EVM - RHL package dissipating 3W vs. Model Data.

The model in Fig. 9 was adjusted for these differences. The power IC is mounted approximately 0.9 in from the south and east sides of the board. The board is 0.031 in thick. The measured data was taken from the center of the IC toward the west side of the PCB.

The Model Data is higher, by about 20C, than the measure data and is explained by absence of the Radiation effect in the model. Is is estimated that up to 35% of the power dissipation is due the heat transfer by radiation. Notice how both plots have a similar temperature curve profile. The measured EVM temperature data ramps up sooner which implies a poorer thermal path than the model. This is true since the model did not take into account all the *signal* vias that break up the copper planes (similar to swiss cheese). The separation in temperatures between the top and bottom surfaces also occurs further out form the IC than the model indicates. This is explained by the signal vias reducing the FR4 effectiveness and other surface mounted components that change the thermal characteristics. The temperature spread from the top and bottom surfaces, at the IC's power pad, is similar for the model and measured data and indicates that the model and PCB are in agreement.

IV. Applying The Basic Concepts In A PCB Design

Taking what was learned about thermal convection design, the goal is to spread the heat out and at the same time get it to both top and bottom surfaces. We know that copper does the best job conducting heat, followed by solder, and then FR4. Therefore the best approach is to have a good thermal path between the power pad of the device to at least one copper plane, either directly connected to the copper plane or by vias and then let the copper plane spread the heat out. The better the copper connection to the heat source, the smaller the temperature change (rise) across the connection. As the heat, from the source, is spread out, it becomes more efficient to transfer the heat through the FR4 to the adjacent surface and then be dissipated into the air.

Consider a design using an IC, as shown in Fig. 12, that dissipates 1.5 W, has a theta of θ_{JC}= 10°C/W and will be mounted on a PCB that is 2-layer, 2-oz. Cu., with up to 9-13 mil vias, in the power pad. Assume the IC's power pad is isolated from the top copper layer.

What is the highest ambient temperature the PCB assembly should see if the $T_{J(MAX)}$ =125°C is not to be exceeded, for a 2 in. × 2 in. PCB (1-in. radius from IC)?

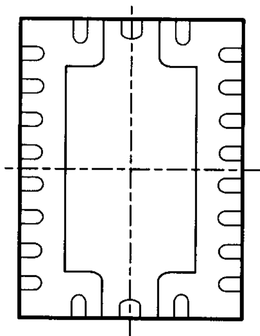


Fig. 12. Bottom view of IC showing power pad restriction by signal pins.

Since the PCB model for Fig. 8 is similar to the one in our example, we can use that data and estimate the maximum ambient temperature using the formula:

$$T_{J\text{-}MAX} = t_{AMB} + dt_{PWB} + dt_{IC}$$

or

$$t_{AMB\text{-}MAX} = T_{J\text{-}MAX} - dt_{IC} - dt_{PWB}$$

The power dissipation in this example is half the referenced model data so the temperature changes should be half. The temperature rise from ambient to the power pad, for the *isolated 1" radius* curve is 110°C. The PCB rise for this example is half of this or 55°C. The rise from the case to junction of the IC is 1.5 W•10°C/W = 15°C. The maximum ambient temperature should not exceed 55°C (125°C-15°C-55°C).

What about for a 3 in. × 3 in. (R=1.5 in.) board? Fig. 10 shows how the base line temperature of the board changes for the size of the PCB for a 3-W dissipation. The change between R=1 and R=1.5 is 32°C (57°C-25°C). For this example at half the power, the temperature change would be half of 32°C or 16°C. It is estimated that the ambient can be 16°C higher on the R=1.5 in. PCB (3 in. × 3 in.) for a maximum ambient of 71°C.

The convection temperature rise above ambient for the R=1 example above is ½•55°C=27.5°C. The temperature margin due to the Thermal Radiation contribution in parallel with the convection would result 1/3 of the calculated convection temperature rise or 9.2°C (1/3•27.5). This means that the assembly should be 9.2°C lower in temperature than estimated due to the contribution of the Thermal Radiation losses.

Understanding the electrical equivalent concept of the current (heat) flowing through the resistors (thetas) from the source (IC) to ground (ambient temperature) resulting in voltage (temperature) drops is helpful in understanding what PCB parameters one has to modify to achieve the thermal results desired.

V. Conclusion

Thermal PCB design is a critical component design that is often over looked or not understood. This article tries to break down the components of thermal design, analyze them and give examples to show what makes an effective design. The ultimate goal is to keep the junction temperature of the IC's below their maximum temperature values. The IC typically has a theta value which accounts for the temperature rise from the Power pad to the IC's junction. The board area and power dissipation determines the base line temperature of the board, assuming there is at least one copper plane connected, by copper, to the IC. The critical area of the design is the connection method close by the power IC. Multiple planes (thicker copper) with multiple ground vias helps reduce the theta values. A larger package for a given heat dissipation provides a larger initial path and less temperature rise. The maximum junction temperature can be estimated by adding the temperature rise of the PCB and the IC's temperature rise to the maximum ambient temperature. The heat loss due to Thermal Radiation is typically not considered in the analysis, but its contribution is used as the margin of safety in the design.

VI. References

Kollman, Robert, *Constructing Your Power Supply - Layout Considerations*, Texas Instruments Power Supply Design Seminar SEM-1700, 2004 (SLUP224).