



FTSM103A

OPERATIONAL AMPLIFIER

- LOW INPUT OFFSET VOLTAGE : 0.5 mV typ.
- LOW SUPPLY CURRENT : 350 μ A/op.
(@ Vcc = 5V)
- MEDIUM BANDWIDTH (unity gain) : 0.9MHz
- LARGE OUTPUT VOLTAGE SWING : 0V to (Vcc – 1.5V)
- INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND
- WIDE POWER SUPPLY RANGE : 3 to 32V \pm 1.5 to \pm 16V

VOLTAGE REFERENCE

- FIXED OUTPUT VOLTAGE REFERENCE 2.5V
- 0.4% AND 1% VOLTAGE PRECISION
- SINK CURRENT CAPABILITY : 1 to 100mA
- TYPICAL OUTPUT IMPEDANCE : 0.2 Ω

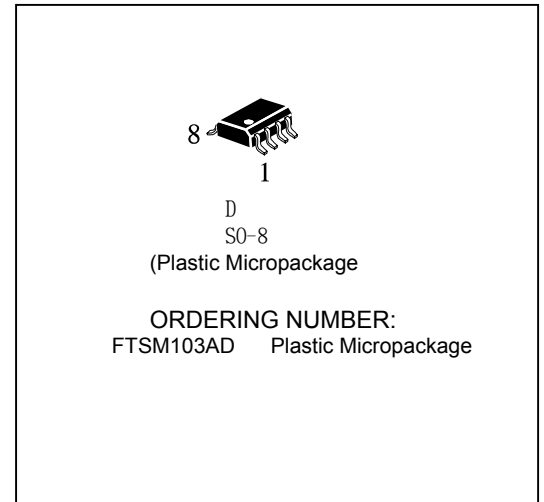
DESCRIPTION

The FTSM103A is a monolithic IC that includes one independent op-amp and another op-amp for which the non inverting input is wired to a 2.5V fixed Voltage Reference. This device is offering space and cost saving in many applications like power supply management or data acquisition systems.

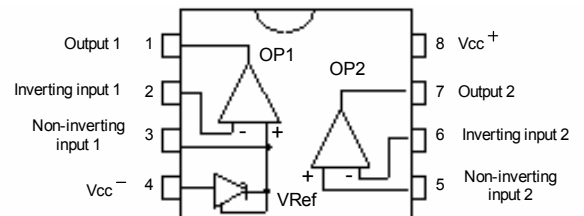
ORDER CODE

Part Number	Temperature Range	Package
		D
FTSM103A	-40°C, +105°C	•

D = Small Outline Package (SO) – also available in Tape & Reel (DT)



PIN CONNECTIONS (top view)





Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{cc}	Supply Voltage	36	V
V _{id}	Differential Input Voltage	36	V
V _i	Input Voltage	-0.3 to +36	V
T _j	Maximum Junction Temperature	150	°C

Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
I _{cc}	Total Supply Current, excluding Current in the Voltage Reference V _{cc+} = 5 V, no load T _{min} < T _{amb} < T _{max} V _{cc+} = 30 V, no load T _{min} < T _{amb} < T _{max}		0.7	1.2 2	mA



Dual Operatinal Amplifier and Voltage Reference

OPERATOR 2 (independent op-amp)

$V_{cc}^+ = +5\text{ V}$, $V_{cc} = \text{Ground}$, $V_o = 1.4\text{ V}$, $T_{amb} = 25\text{ }^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
V_{io}	Input Offset Voltage $T_{amb} = 25\text{ }^\circ\text{C}$ $T_{min.} \leq T_{amb} \leq T_{max}$		0.5	3 5	mV
DV_{io}	Input Offset Voltage Drift			7	$\mu\text{V}/^\circ\text{C}$
I_{io}	Input Offset Current $T_{min.} \leq T_{amb} \leq T_{max}$		2	30 50	nA
I_{ib}	Input Bias Current $T_{min.} \leq T_{amb} \leq T_{max}$		20	150 200	nA
A_{vd}	Large Signal Voltage Gain $V_{cc} = 15\text{ V}$, $R_L = 2\text{ k}$, $V_o = 1.4\text{ V}$ to 11.4 V $T_{min.} \leq T_{amb} \leq T_{max}$	50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio $V_{cc} = 5\text{ V}$ to 30 V	65	100		dB
V_{icm}	Input Common Mode Voltage Range $V_{cc} = +30\text{ V}$ – see note ¹⁾ $T_{min.} \leq T_{amb} \leq T_{max}$	0 0		$(V_{cc}^+) - 1.5$ $(V_{cc}^+) - 2$	V
CMR	Common Mode Rejection Ratio $T_{min.} \leq T_{amb} \leq T_{max}$	70 60	85		dB
I_{source}	Output Current Source $V_{cc} = +15\text{ V}$, $V_o = 2\text{ V}$, $V_{id} = +1\text{ V}$	20	40		mA
I_o	Short Circuit to Ground $V_{cc} = +15\text{ V}$		40	60	mA
I_{sink}	Output Current Sink $V_{id} = -1\text{ V}$, $V_{cc} = +15\text{ V}$, $V_o = 2\text{ V}$	10	20		mA
V_{OH}	High Level Output Voltage $V_{cc}^+ = 30\text{ V}$, $T_{amb} = 25\text{ }^\circ\text{C}$, $R_L = 10\text{ k}$ $T_{min.} \leq T_{amb} \leq T_{max}$	27 27	28		V
V_{OL}	Low Level Output Voltage $R_L = 10\text{ k}$ $T_{min.} \leq T_{amb} \leq T_{max}$		5	20 20	mV
SR	Slew Rate at Unity Gain $V_i = 0.5$ to 3 V , $V_{cc} = 15\text{ V}$ $R_L = 2\text{ k}$, $C_L = 100\text{ pF}$, unity gain	0.2	0.4		V/ μs
GBP	Gain Bandwidth Product $V_{cc} = 30\text{ V}$, $R_L = 2\text{ k}$, $C_L = 100\text{ pF}$ $f = 100\text{ kHz}$, $V_{in} = 10\text{ mV}$	0.5	0.9		MHz
THD	Total Harmonic Distortion $f = 1\text{ kHz}$ $A_v = 20\text{ dB}$, $R_L = 2\text{ k}$, $V_{cc} = 30\text{ V}$ $C_L = 100\text{ pF}$, $V_o = 2V_{pp}$		0.02		%

1 The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{cc}^+ - 1.5\text{ V}$. But either of both inputs can go to $+36\text{ V}$ without damage.



Dual Operatinal Amplifier and Voltage Reference

OPERATOR 1 (op-amp with non-inverting input connected to the internal Vref)
 $V_{cc}^+ = +5\text{ V}$, $V_{cc} = \text{Ground}$, $T_{amb} = 25\text{ }^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
V_{io}	Input Offset Voltage $V_{icm} = 0\text{V}$ $T_{amb} = 25\text{ }^\circ\text{C}$ $T_{min} \leq T_{amb} \leq T_{max}$		0.5	3 5	mV
DV_{io}	Input Offset Voltage Drift			7	$\mu\text{V}/^\circ\text{C}$
I_{ib}	Input Bias Current Negative input		20		nA
A_{vd}	Large Signal Voltage Gain $V_{icm} = 0\text{V}$ $V_{cc} = 15\text{V}$, $R_L = 2\text{k}$		100		V/mV
SVR	Supply Voltage Rejection Ratio $V_{icm} = 0\text{V}$ $V_{cc}^+ = 5\text{V to } 30\text{V}$	65	100		dB
I_{source}	Output Current Source $V_o = 2\text{V}$ $V_{cc} = +15\text{V}$, $V_{id} = +1\text{V}$	20	40		mA
I_o	Short Circuit to Ground $V_{cc} = +15\text{V}$		40	60	mA
I_{sink}	Output Current Sink $V_{id} = -1\text{V}$, $V_{cc} = +15\text{V}$, $V_o = 2\text{V}$	10	20		mA
V_{OH}	High Level Output Voltage $V_{cc}^+ = 30\text{V}$, $T_{amb} = 25\text{ }^\circ\text{C}$, $R_L = 10\text{k}$ $T_{min.} \leq T_{amb} \leq T_{max}$	27 27	28		V
V_{OL}	Low Level Output Voltage $R_L = 10\text{k}$ $T_{min.} \leq T_{amb} \leq T_{max}$		5	20 20	mV
SR	Slew Rate at Unity Gain $V_i = 0.5\text{ to } 2\text{V}$, $V_{cc} = 15\text{V}$ $R_L = 2\text{k}$, $C_L = 100\text{pF}$, unity gain	0.2	0.4		V/ μs
GBP	Gain Bandwidth Product $V_{cc} = 30\text{V}$, $R_L = 2\text{k}$, $C_L = 100\text{pF}$ $f = 100\text{kHz}$, $V_{in} = 10\text{mV}$	0.5	0.9		MHz
THD	Total Harmonic Distortion $f = 1\text{kHz}$ $A_V = 20\text{dB}$, $R_L = 2\text{k}$, $V_{cc} = 30\text{V}$ $C_L = 100\text{pF}$, $V_o = 2V_{pp}$		0.02		%



Dual Operatinal Amplifier and Voltage Reference

VOLTAGE REFERENCE

Symbol	Parameter	Value	Unit
I_k	Cathode Current	1 to 100	mA

Symbol	Parameter	Min	Typ	Max	Unit
V_{ref}	Reference Input Voltage $T_{amb} = 25\text{ }^\circ\text{C}$ $T_{min} \leq T_{amb} \leq T_{max}$	2.49 2.48	2.5	2.51 2.52	V
ΔV_{ref}	Reference Input Voltage Deviation Over Temperature Range $V_{KA} = V_{ref}, I_k = 10\text{mA}$ $T_{min} \leq T_{amb} \leq T_{max}$		5	24	mV
I_{min}	Minimum Cathode Current for Regulation $V_{KA} = V_{ref}$		0.5	1	mA
$ Z_{KA} $	Dynamic Impedance-note ¹⁾ $V_{KA} = V_{ref}, \Delta I_k = 1\text{ to }100\text{mA}, f < 1\text{kHz}$		0.2	0.5	Ω

¹ The Dynamic impedance is defined as $|Z_{KA}| = \Delta V_{KA} / \Delta I_k$



Typical Performance Characteristics

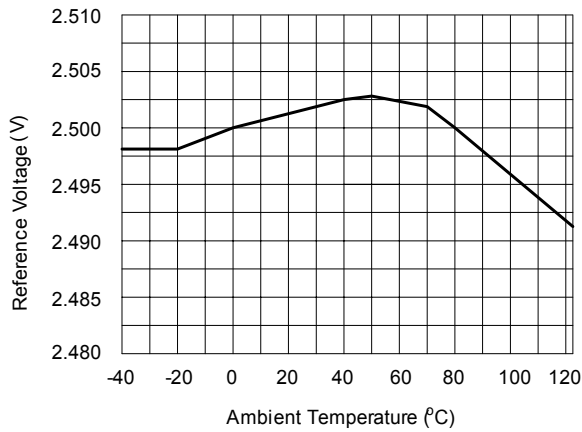


Figure 1. Reference Voltage vs. Ambient Temperature

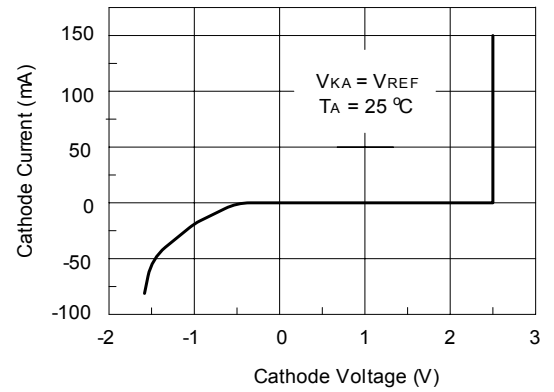


Figure 2. Cathode Current vs. Cathode Voltage

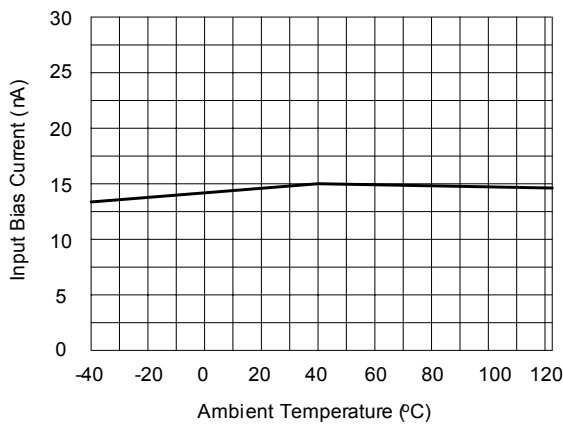


Figure 3. Input Bias Current vs. Ambient Temperature

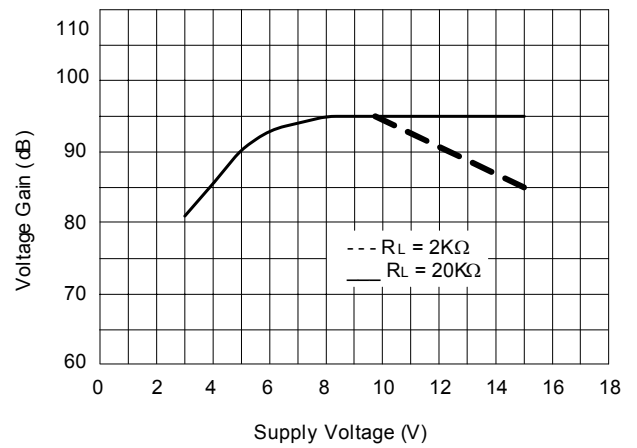
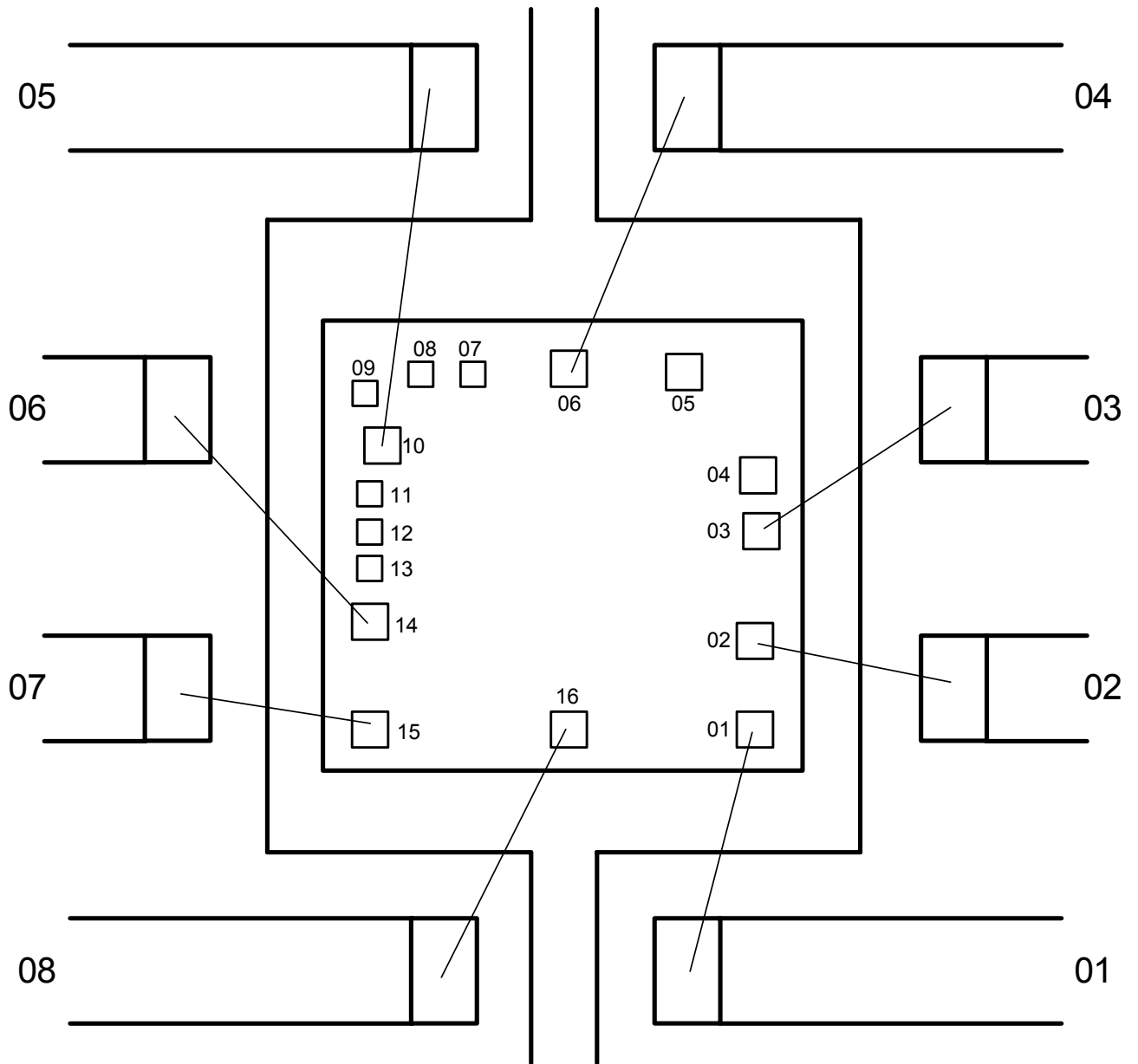
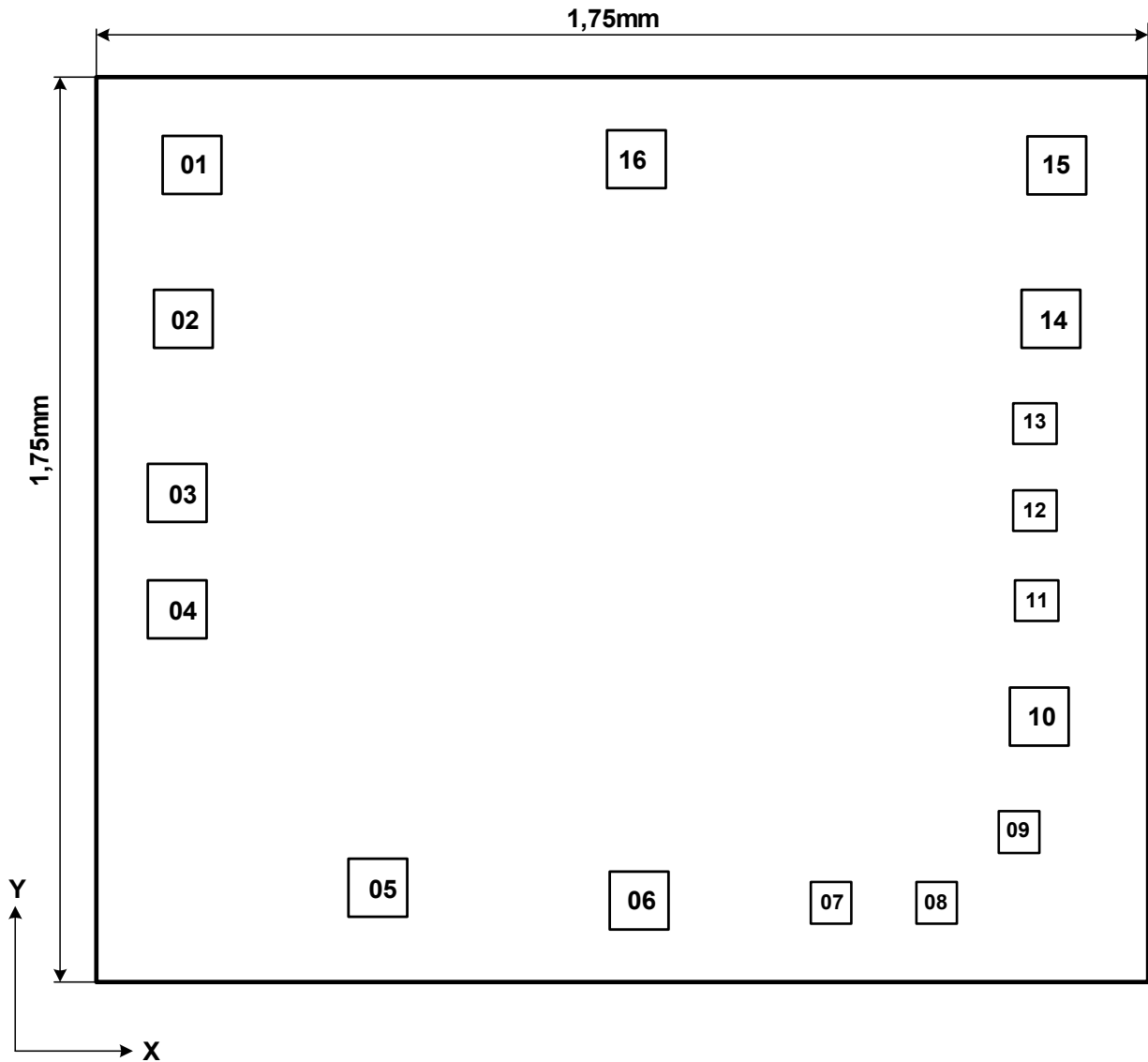


Figure 4. Operational Amplifier Voltage Gain



Bonding diagram of FTSM103A



Pad size 01, 02, 03, 06, 10, 14, 15, 16 have been bounded
Pad size 04, 05, 07, 08, 09, 11, 12, 13 have not been bounded

Pads location of FTSM103A



Dual Operatinal Amplifier and Voltage Reference

Die size $X_r=1.75\text{mm}$, $Y_r=1.75\text{mm}$ (pad size measured by layer “passivation”)
Coordinates of pads

No of pad (by layer “passivation”)	Coordinates left bottom, mkm		pad size, mkm
	X	Y	
01	157	1542	100×100
02	107	1285	100×100
03	102	996	100×100
04	103	836	100×100
05	500	153	100×100
06	827	98	100×100
07	1298	128	70×70
08	1428	128	70×70
09	1542	226	70×70
10	1549	392	100×100
11	1521	588	70×70
12	1523	776	70×70
13	1523	917	70×70
14	1543	1285	100×100
15	1493	1542	100×100
16	825	1557	100×100

No of pad	Pin	Function
01	01	Output 1
02	02	Inverting input 1
03	03	Non-inverting input 1
06	04	V_{cc}^-
10	05	Non-inverting input 2
14	06	Inverting input 2
15	07	Output 2
16	08	V_{cc}^+