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FAIRCHILD SEMICONDUCTOR™

AN9010

MOSFET Basics

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CONTENTS

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The Bipolar Power Transistor (BPT), as a switching device for power applications, had a few disadvantages. This led to the development of the power MOSFET (Metal Oxide Semiconductor Field Effect Transistor). The power MOSFET is used in many applications such as SMPS (Switched Mode Power Supplies), computer peripherals, automotive, and motor control. Continuous research and improvement have provided it with ideal characteristics for replacing the BJT (Bipolar Junction Transistor).This application note is a general description of power MOSFETs and a detailed presentation of items from FSC's data book specifications.

1. History of Power MOSFETs

The theory behind Field Effect Transistor has been known since 1920~1930, which is 20 years before the Bipolar Junction Transistor was invented. At that time, J.E. Lilienfeld of USA suggested a transistor model having two metal contacts on each side with a metallic plate (aluminum) on top of the semiconductor. The electric field at the semiconductor surface, formed by the voltage supplied at the metallic plate, enables the control of the current flow between the metal contacts. This was the initial conception of the Field Effect Transistor. But due to lack of appropriate semiconductor materials and the immature technology, the development was very slow. William Shockely introduced JFETs (Junction Field Effect Transistors) in 1952. Dacey and Ross improved on it in 1953. In JFETs, Lilienfeld's metallic field is replaced by a pn junction, the metal contacts are called source and drain, and the field effect electrode is called gate. Research in small-signal MOSFETs continued, without any significant improvements in power MOSFET design. New products were introduced in the 1970s.

In March 1986 FSC formed TFT with 9 people, and began research on power MOSFETs. And currently, Fairchild produces QFET series using planar technology and low voltage power trench products using trench technology.

2. FETs

JFET, MOSFET

1) JFET (Junction Field Effect Transistors)

There are two types of JFETs. One is an n-channel type and the other is a p-channel type. They both control the drain-to-source current by the voltage supplied to the gate. As shown in the Figure 1 (a), if the bias is not supplied at the gate, the current flows from the drain to the source, and when the bias is supplied at the gate, the depletion region begins to grow and reduces the current as shown in Figure 1 (b). The reason for the wider depletion region of the drain compared to the source depletion region is that the reverse bias of the gate and the drain $V_{DG}(=V_{GS}+V_{DS})$ is higher than the V_{GS} (bias between the gate and the source).

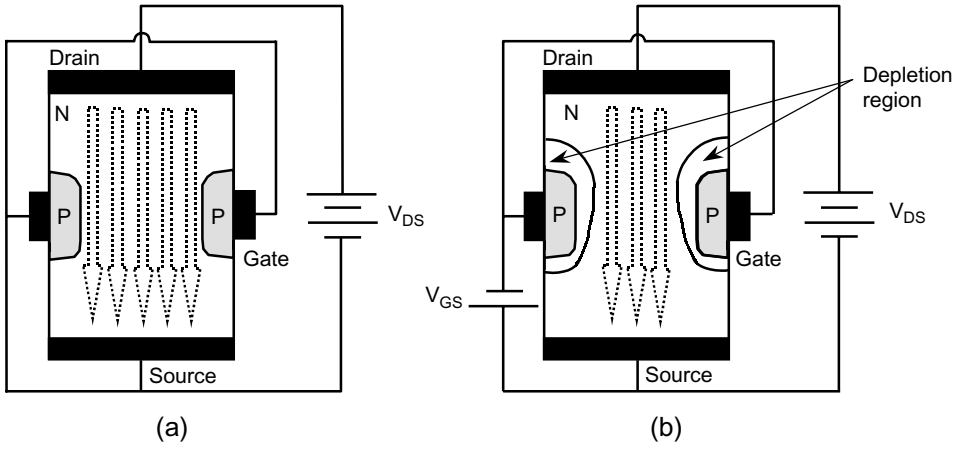

Figure 1: The Structure of a JFET and its Operation

(a) When V_{GS} (Gate-source voltage) is not supplied
(b) When V_{GS} (Gate-source voltage) is supplied

2) MOSFET (Metal Oxide Semiconductor Field Effect Transistors)

The two types of MOSFETs are the depletion type and the enhancement type, and each has a n / p – channel type. The depletion type is normally on, and operates as a JFET (refer to Figure 2). The enhancement type is normally off, which means that the drain to source current increases as the voltage at the gate increases. No current flows when no voltage is supplied at the gate (refer to Figure 3).

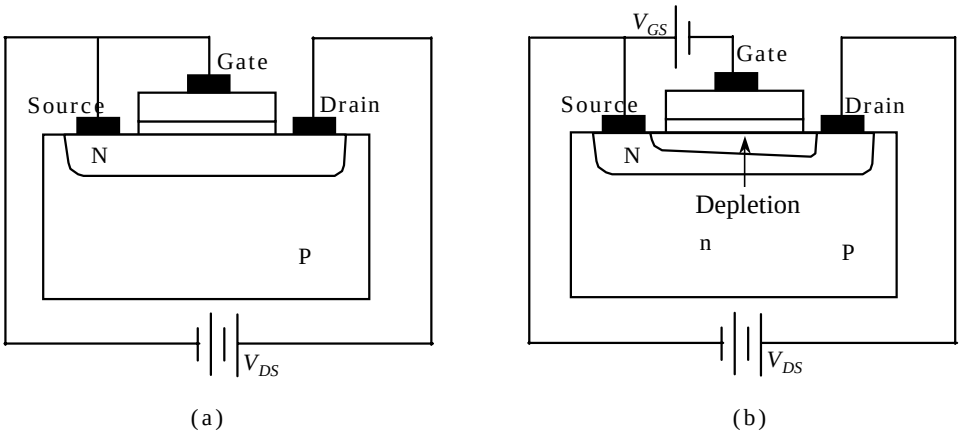

Figure 2: The Structure of a Depletion Type MOSFET and its Operation

(a) When V_{GS} (Gate-source voltage) is not supplied
(b) When V_{GS} (Gate-source voltage) is supplied

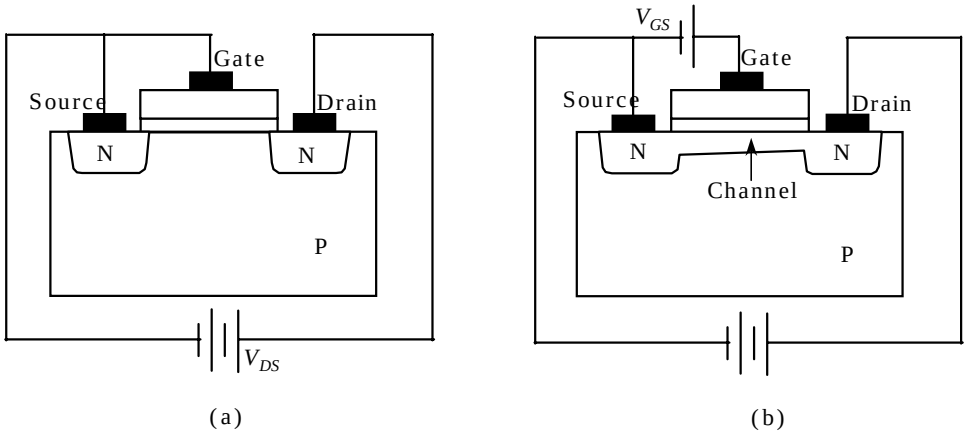

Figure 3: The Structure of an Enhancement Type MOSFET and its Operation

(a) When V_{GS} (Gate-source voltage) is not supplied
(b) When V_{GS} (Gate-source voltage) is supplied

3. The Structure of a MOSFET

1) Lateral Channel Design

The drain, gate, and source terminal are placed on the surface of a silicon wafer. This is suitable for integration but not for obtaining high power ratings since the distance between source and drain must be large to obtain better voltage blocking capability. Also, the drain-to-source current is inversely proportional to the length.

2) Vertical Channel Design

The drain and source are placed on the opposite sides of a wafer. This is suitable for a power device, as more space can be used as source. As the length between the source and drain is reduced, it is possible to increase the drain-to-source current rating, and also increase the voltage blocking capability by growing the epitaxial layer (drain drift region).

1. The VMOSFET Design
   As shown in Figure 4 (a), this design, the first to be commercialized has a V-groove at the gate region. The DMOSFETs replaced VMOSFETs as there were stability problems in manufacturing, and they also had a high electric field at the tip of the V-groove.

2. The DMOSFET Design
   As shown in Figure 4 (b), it has a double-diffusion structure with a P-base region and a N^+ source region. It is the most commercially successful design.

3. The UMOSFET Design
   As shown in Figure 4 (c), this design has a U-groove at the gate region. It has a higher channel density which reduces the on-resistance as compared to the VMOSFETs and the DMOSFETs. UMOSFET designs with the trench etching process were commercialized in the 90's.

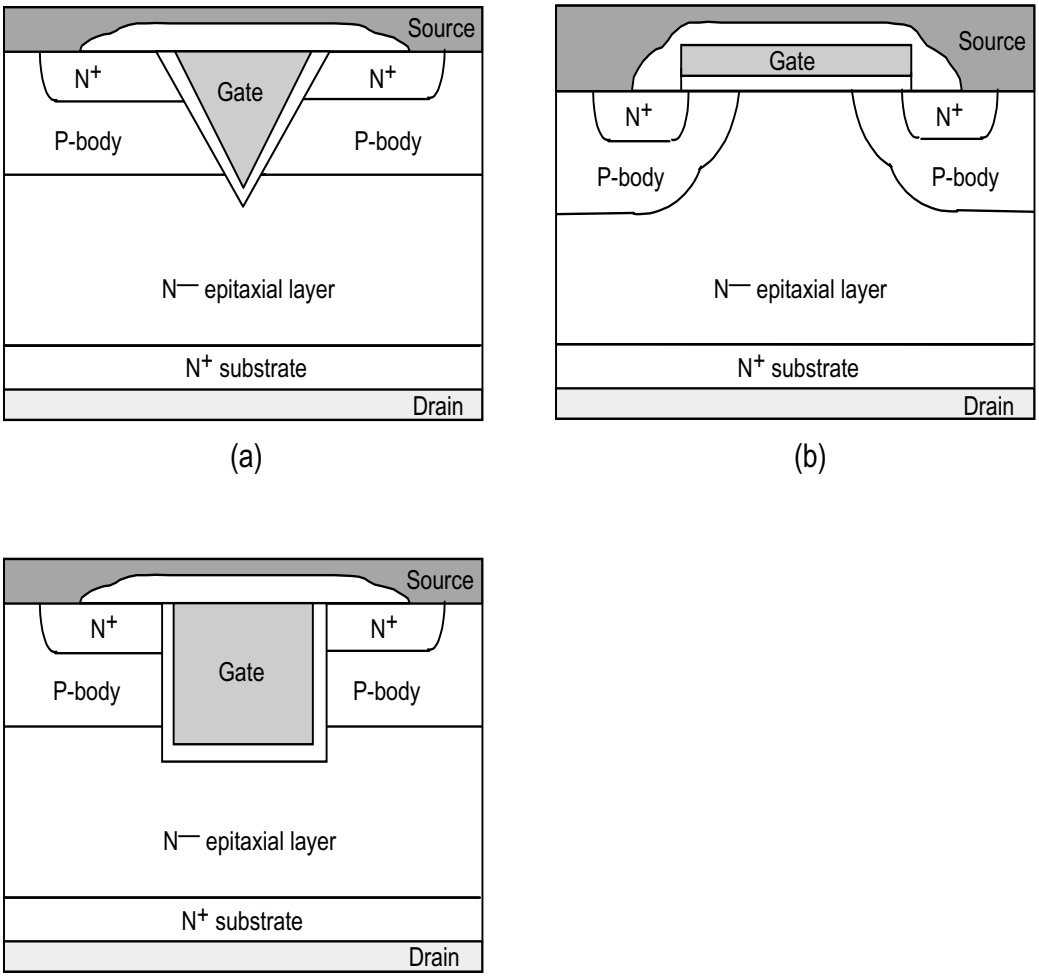

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Figure 4: Vertical Channel Structure

(a) The VMOSFET Structure
(b) The DMOSFET Structure
(c) The UMOSFET Structure

4. The Characteristics of a MOSFET

1) Advantages

1. High input impedance - voltage controlled device - easy to drive.

   To maintain the on-state, a base drive current which is 1/5th or 1/10th of collector current is required for the current controlled device (BJT). And also a larger reverse base drive current is needed for the high speed turn-off of the current controlled device (BJT). Due to these characteristics base drive circuit design becomes complicated and expensive. On the other hand, a voltage controlled MOSFET is a switching device which is driven by a channel at the semiconductor's surface due to the field effect produced by the voltage applied to the gate electrode, which is isolated from the semiconductor surface. As the required gate current during switching transient as well as the on and off states is small, the drive circuit design is simple and less expensive.

2. Unipolar device - majority carrier device - fast switching speed.

   As there are no delays due to storage and recombination of the minority carrier, as in the BJT, the switching speed is faster than the BJT by orders of magnitude. Hence, it has an advantage in a high frequency operation circuit where switching power loss is prevalent.

3. Wide SOA (safe operating area).

   It has a wider SOA than the BJT because high voltage and current can be applied simultaneously for a short duration. This eliminates destructive device failure due to second breakdown.

4. Forward voltage drop with positive temperature coefficient - easy to use in parallel.

   When the temperature increases, the forward voltage drop also increases. This causes the current to flow equally through each device when they are in parallel. Hence, the MOSFET is easier to use in parallel than the BJT, which has a forward voltage drop with negative temperature coefficient.

2) Disadvantage

In high breakdown voltage devices over 200V, the conduction loss of a MOSFET is larger than that of a BJT, which has the same voltage and current rating due to the on-state voltage drop.

3) Basic Characteristics

1. Vertically oriented four-layer structure (n^+ p n^- n^+)

2. Parasitic BJT exists between the source and the drain.

   The p-type body region becomes base, the n^+ source region becomes an emitter, and the n-type drain region becomes the collector (refer to Figure 5). The breakdown voltage decreases from BV_{CBO} to BV_{CEO}, which is 50 ~ 60 [%] of BV_{CBO} when the parasitic BJT is turned on. At this state, if a drain voltage higher than BV_{CEO} is supplied, the device falls into an avalanche breakdown state. If the drain current is not limited externally, it will be destroyed by the second breakdown. So the n^+ source region and the p-type body region must be shorted by metallization in order to prevent the parasitic BJT from turning on.

But if the V_{DS} rate of increase is large in the high speed turn–off state, there is a voltage drop between the base and the emitter, which causes the BJT to turn–on. This is prevented by increasing the doping density of the p - body region, which is at the bottom of the n^+ source region, and by lowering the MOSFETs switching speed by designing the circuit so that the gate resistance is large. Due to the source region being short, another parasitic component, the diode is formed. This is used in half-bridge and full-bridge converters.

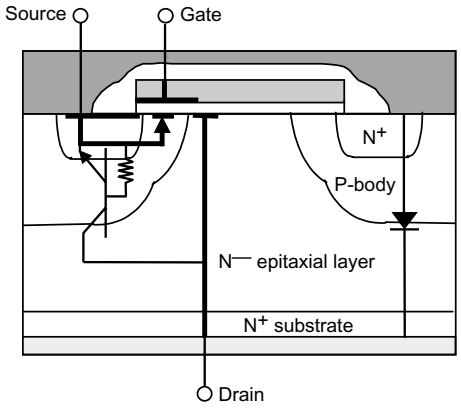


Figure 5: The MOSFET Vertical Structure Showing the Parasitic BJT and Diode

3. Output characteristics

   i_D characteristics due to V_{DS} in many V_{GS} conditions. (Refer to Figure 6)

   → It is divided into the ohmic region, the saturation (=active) region, and the cut-off region.

   - Ohmic region: A constant resistance region. If the drain-to-source voltage is zero, the drain current also becomes zero regardless of gate–to-source voltage. This region is at the left side of the $V_{GS} – V_{GS(th)} = V_{DS}$ boundary line ($V_{GS} – V_{GS(th)} > V_{DS} > 0$). Even if the drain current is very large, in this region the power dissipation is maintained by minimizing $V_{DS(on)}$.
   - Saturation region: A constant current region. It is at the right side of the $V_{GS} – V_{GS(th)} = V_{DS}$ boundary line. Here, the drain current differs by the gate–to-source voltage, and not by the drain-to-source voltage. Hence, the drain current is called saturated.
   - Cut-off region: It is called the cut-off region, because the gate-to-source voltage is lower than the $V_{GS(th)}$ (threshold voltage).

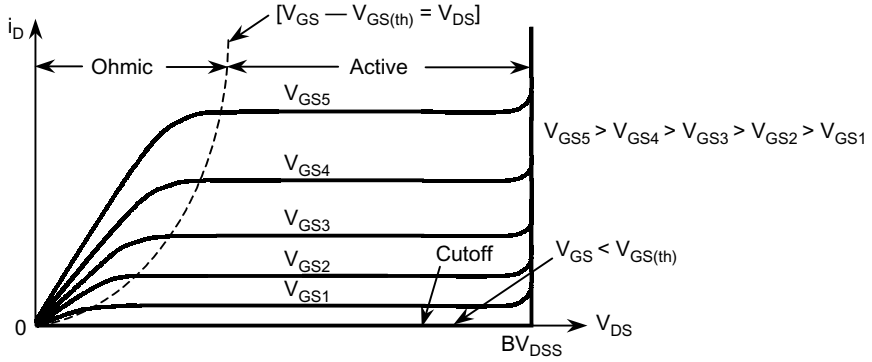


Figure 6: Output Characteristics

4. Transfer characteristics

   i_D characteristics due to V_{GS} in the active region. (Refer to Fig. 7)

   - i_D equation due to V_{GS}

$$i_D = K(V_{GS} - V_{GS(th)})^2$$

$$K = \mu_n C_{OX} \frac{W}{2L}$$

where μ_n: carrier mobility

C_{OX}: gate oxide capacitance per unit area

$$C_{OX} = \varepsilon_{OX}/t_{OX}$$

ε_{OX}: dielectric constant of the silicon dioxide

t_{OX}: thickness of the gate oxide

W: channel width

L: channel length

A parabolic transfer curve exists in a logic-level device according to the above equation. In a power MOSFET this is true only in the low i_D of the transfer curve, and the other areas show linearity. This is because the mobility of the carrier is not constant, but decreases due to the

increase of the electric field along with the increase of i_D at the inverse layer.

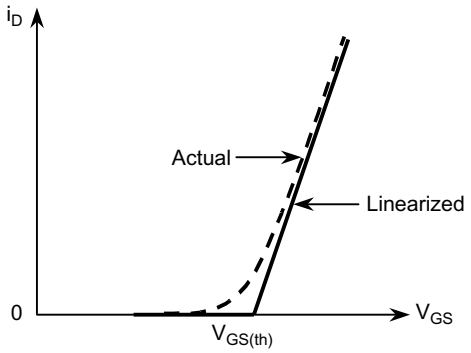


Figure 7: Transfer Curve

5. Characteristics of MOSFET's in ON and OFF States.

1) Off State

(1) BV_{DSS}: This is the maximum drain-to-source voltage where the MOSFET can endure without the avalanche breakdown of the body-drain pn junction in off state (where the gate and source are shorted). The measurement conditions are V_{GS} = 0 [V], I_D = 250 [μA], and the drift region's (N^- epitaxy) length is determined by the BV_{DSS}. Avalanche, reach-through, punch-through, zener, and dielectric breakdowns are the 5 factors which drive breakdown. Three of these factors are described below:

1. Avalanche breakdown

   It is the mobile carriers' sudden avalanche breakdown caused by the increasing electric field in the depletion region of the body-drain pn junction up to a critical value. It is the main factor among others that drives breakdown.

2. Reach-through breakdown

   It is a special case of avalanche breakdown occurring when the depletion region of the N^- epitaxy contacts the N^+ substrate.

3. Punch-through breakdown

   This is an avalanche breakdown occurring when the depletion region of the body-drain junction contacts the N^+ source region.

(2) I_{DSS}: The drain-to-source leakage current when it is an off state where the gate is being shorted with the source. The increase in I_{DSS}, which is sensitive to temperature, is large with the increase in temperature, while the increase in BV_{DSS} is very little.

2) Turn-on Transient

The Process of Channel Formation

1. The formation of the depletion region:
   When a small positive gate – to – source voltage is supplied to the gate electrode (refer to Figure 8 (a)):

   A positive charge induced in the gate electrode, inducts the same amount of negative charge at the oxide – silicon interface (P^--body region, which is underneath the gate oxide). The holes here are pushed into the semiconductor bulk by an electric field, and the depletion region is formed by the acceptors with a negative charge.

2 The formation of the inversion layer:
   As the positive gate – to – source voltage increases (refer to Figure 8 (b), (c)):

   The depletion region becomes wider towards the body, and begins to drag the free electrons to the interface. These free electrons are created by thermal ionization. The free holes, created with free electrons, are pushed into the semiconductor bulk. The holes that have not been pushed into the bulk are neutralized by the electrons that have been dragged by the positive charge of the holes from the n^+ source. If the supplied voltage keeps increasing, the density of the free holes of the body, and the free electrons of the interface becomes equal. At this point, the free electron layer is called an inversion layer. This inversion layer enables the current flow as it becomes the conductive pass(=channel) of the MOSFETs drain and source.

   Threshold voltage: The gate-to-source voltage, which forms the inverse layer, is called $V_{GS(th)}$ (=threshold voltage).

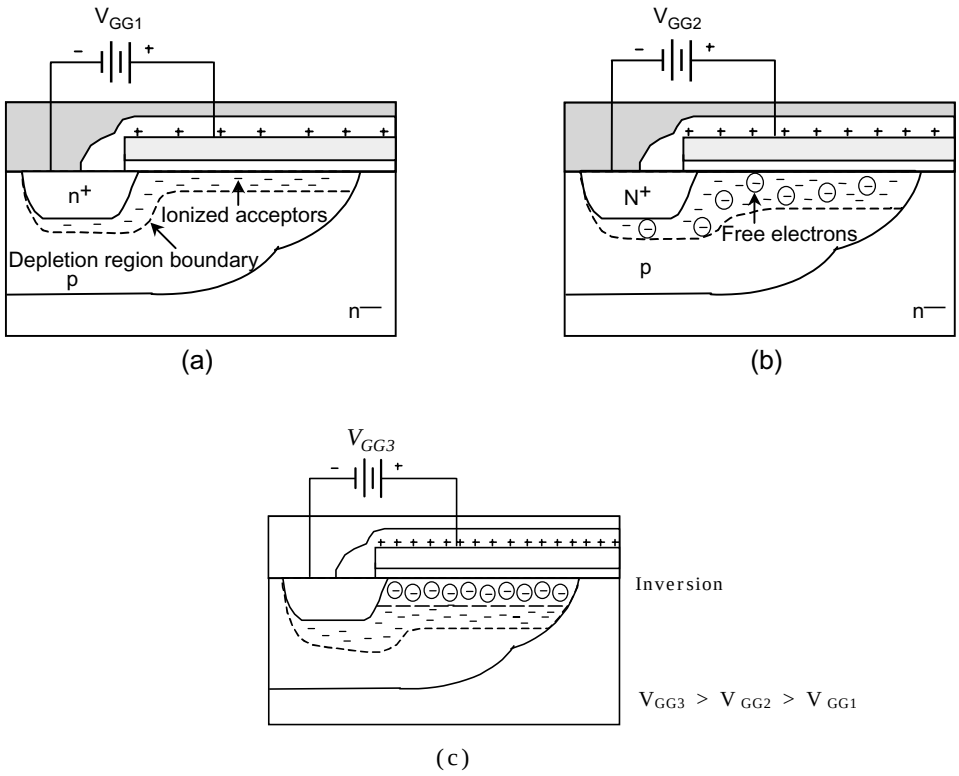


Figure 8: The Process of Channel Formation
(a) Formation of the Depletion Region
(b), (c) Formation of the Inversion Layer

3) On state

Drain current (I_D) changes due to the increase in drain-to-source voltage (V_{DD}) (V_{GS} is constant). I_D starts to flow when the channel has formed and V_{DD} is supplied. When the V_{GS} is a constant value, and the V_{DD} is increased, the I_D also increases linearly, But as shown in the MOSFET output characteristics graph, when the real V_{DD} goes over a certain level, the rate of increase I_D decreases slowly. And eventually, it becomes a constant value independent of V_{DD}, and becomes dependent on V_{GS}.

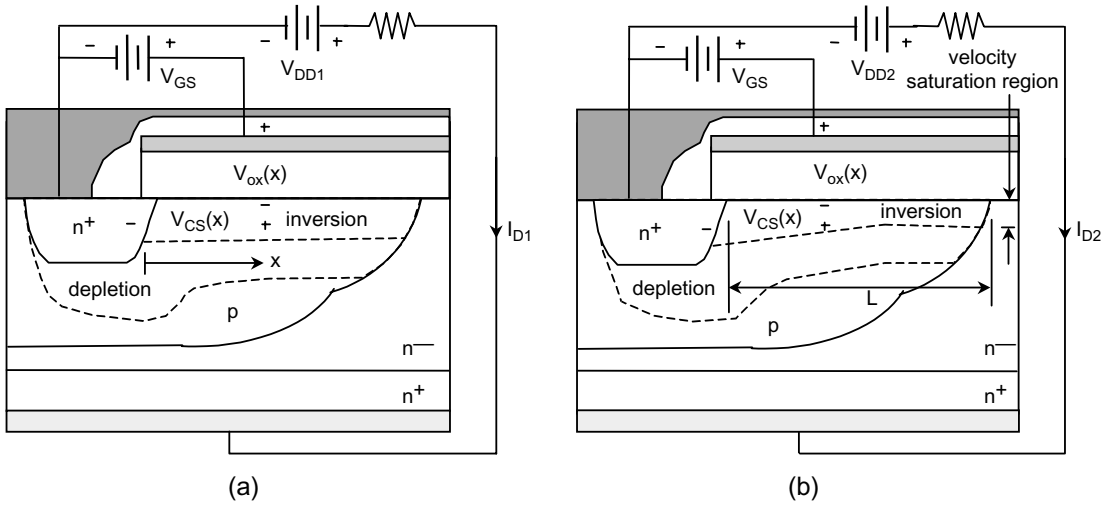


Figure 9: Inversion Layer Thickness Changes due to the Increase of the Drain-to-Source Voltage (V_{DD}). Where, $V_{DD1} < V_{GS} - V_{GS(th)}$, $V_{DD2} > V_{GS} - V_{GS(th)}$, I_{D2} (saturation current) > I_{D1}

(a) spatially uniform
(b) spatially nonuniform

To understand the characteristics, shown in Figure 9, note the voltage drop at $V_{CS}(x)$ due to ohmic resistance when I_D is flowing at the inverse layer. $V_{CS}(x)$ is the channel-to-source voltage from the source at a distance of x. This voltage is equal to the $V_{GS}–V_{ox}(x)$ at all x points. $V_{ox}(x)$ is the gate-to-body voltage crossing the gate oxide from the source at a distance of x, and it has the maximum value at V_{DS} at x=L (the drain end of the channel). As shown in Figure 9 (a), when low voltage $V_{DD}=V_{DD1}$ is supplied, low $I_D(=I_{D1})$ which has almost no voltage drop of $V_{CS}(x)$ flows. As $V_{ox}(0)\sim V_{ox}(L)$ is constant, the thickness of the inversion layer remains uniform. And as higher V_{DD} is supplied, I_D increases,the voltage drop of $V_{CS}(x)$ occurs, and the value of $V_{ox}(x)$ decreases. These reduce the thickness of the inversion layer starting from x=L. Because of this, the resistance increases, and the graph of I_D starts to become flat, as opposed to increasing with the increment of V_{DD}. When $V_{ox}(L)=V_{GS}–V_{DS}=V_{GS(th)}$, as I_D increases, the inversion layer at x=L doesn't disappear due to the high electric field ($J=\sigma E$) formed by the reduction in thickness, and maintains the minimum thickness. The high electric field not only maintains the minimum thickness of the inversion layer, it also saturates the velocity of the charge carrier at $V_{ox}(L)=V_{GS}–V_{DS}=V_{GS(th)}$.

The velocity of the charge carrier increases with the increase in the electric field initially, and at a certain point, it is saturated. Silicon starts saturating when the electric field reaches 1.5×10^4 [V/cm], and the drift velocity of the electron is 8×10^6 [cm/s]. At this point, the device goes into the active region. When a higher V_{DD} is supplied, as shown in Figure 9 (b), the electric field at x=L increases more, and the channel region which maintained the minimum thickness expands towards the source. V_{DS} becomes $V_{DS} > V_{GS} - V_{GS(th)}$ due to the increase of V_{DD}, and I_D is kept constant.

4) Turn-off Transient

The reverse process of the turn-on transient is turn-off transient.

6. User's Manual

1) Characteristics of Capacitance

The three types of parasitic capacitance described in the data book are shown below.

- Input capacitance $C_{iss} = C_{gd} + C_{gs}$
- Output capacitance $C_{oss} = C_{gd} + C_{ds}$
- Reverse transfer capacitance $C_{rss} = C_{gd}$

The following figure shows the parasitic capacitance described above.

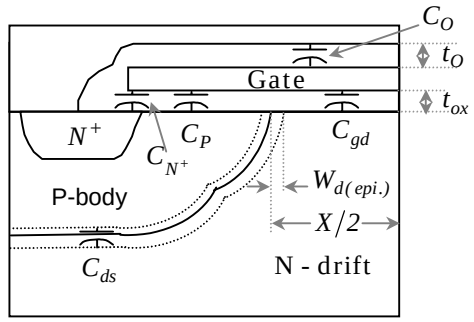


Figure 10: Vertical Structure Showing Parasitic Capacitance

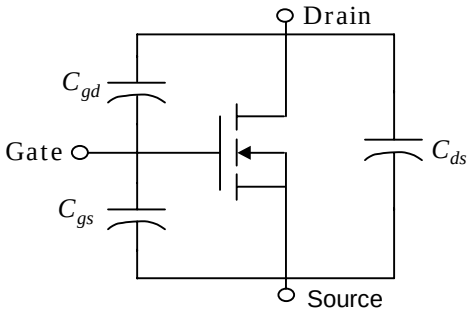


Figure 11: Equivalent Circuit Showing Parasitic Capacitance

(1): C_{GS}: The Capacitance between the Gate and Source

$$C_{gs} = C_O + C_{N^+} + C_P$$

1. C_O: The capacitance between the gate and source metal

$$C_O = \frac{\varepsilon_I A_O}{t_O}$$

where ε_I: the dielectric constant of the intervening insulator

t_O: the thickness of the intervening insulator

A_O: the area of the overlap between the source and gate electrode

2. C_{N^+}: The capacitance between the gate and the n^+ source diffusion region

$$C_{N^+} = \frac{\varepsilon_{ox} A_{N^+O}}{t_{ox}} = C_{ox} A_{N^+O}$$

where ε_{ox}: the dielectric constant of the gate oxide

t_{ox}: the gate oxide thickness

C_{ox}: gate-oxide capacitance per unit area

A_{N^+O}: the area of overlap of the gate electrode over the N^+ emitter

3. C_P: The capacitance between the gate and p-body. It is affected by the gate, the drain voltage and the channel length. The C_P is the only component that is influenced by the change of the drain voltage (V_{DS}) among other C_{gs} components. When V_{DS} increases, the depletion region expands to the p-body, and decreases the value of C_P. But even if the V_{DS} increases up to breakdown voltage, there is almost no change in the value of C_P, as the depletion region doesn't exceed 10% of the p-body. Hence, the change of C_{gs} due to V_{DS} is very small.

(2) C_{gd}: The Capacitance between the Gate and Drain.

This is influenced by the voltage of the gate and the drain. When there are variations in V_{DS}, the area under C_{gd} (n^--drift region meeting with the gate oxide) is changed, and the value of the capacitance is affected. And as shown in the following equation, when $V_{DS} >> \phi_B$, the capacitance decreases as V_{DS} increases with the relation of $C_{gd} \propto (1 - k\sqrt{V_{DS}})$.

$$C_{gd(\text{per unit area})} = C_{ox}\left(1 - \frac{2W_{d(epi.)}}{X}\right)$$

where X: the length between adjoining cells

$W_{d(epi.)}$: the width of the depletion region in the epitaxial layer(= N- drift region)

$$W_{d(epi.)} = \sqrt{\frac{2k_s\varepsilon_o(V_{DS} + \phi_B)}{qC_B}}$$

As C_{gd} increases ($1+g_{fs}R_L$(load resistance)) times due to the Miller effect, it prominently decreases the frequency characteristics.

Frequency response of the power MOSFET

The frequency response of the power MOSFET is limited by the charging and discharging of the input capacitance. If the C_{gs} and C_{gd} which determine the input capacitance become smaller, it is possible to work in high frequency. As the input capacitance is unrelated to the temperature, the MOSFET's switching speed is also unrelated to the temperature.

(3):C_{ds}: The Capacitance between the Drain and Source.

The capacitance varies due to the variation of the C_{ds}'s thickness, which is the junction thickness of the p-body and the n^-- drift region, with the change of V_{DS}.

$$C_{ds(\text{per unit area})} = \sqrt{\frac{qk_s\varepsilon_o C_B}{2(V_{DS} + \phi_B)}}$$

where q: the elementary electronic charge ($1.9\text{x}10^{-19}$ [C])

k_s: silicon dielectric constant

ε_o: the permeability of free space (8.86×10^{-14} [F/cm])

C_B: epitaxial layer background concentration [atoms/cm^3]

V_{DS}: drain-to-source voltage

ϕ_B: diode potential

As shown in the equation above, when $V_{DS} >> \phi_B$, C_{ds} decreases as V_{DS} increases with the relationship of $C_{gd} \propto (1/\sqrt{V_{DS}})$.

2) Characteristics of the Gate Charge

It is the amount of charge that is required during the MOSFET's turn-on or turn-off transient.

The following types of charges are mentioned In the data book.

Total Gate Charge …… Q_g (The amount of charge during $t_0 \sim t_4$)

Gate-Source Charge …… Q_{gs} (The amount of charge during $t_0 \sim t_2$)

Gate-Drain ("Miller") Charge …..... Q_{gd} (The amount of charge during $t_2 \sim t_3$)

Figure 12 shows the gate-source voltage, gate-source current, drain-source voltage, and drain-source current during turn-on. They are divided into four sections to show the equivalent circuits at the diode-clamped inductive load circuit.

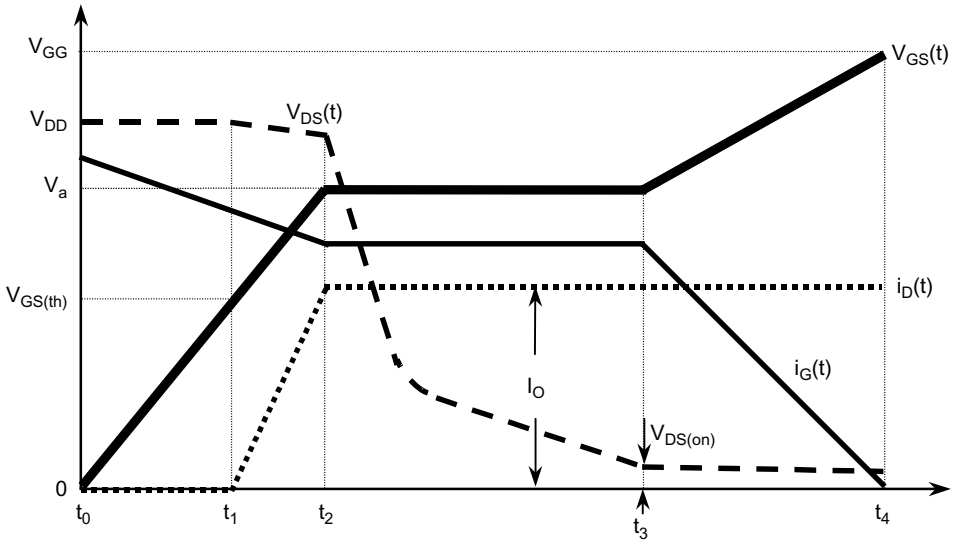


Figure 12: The Graph of $V_{GS}(t)$, $i_G(t)$, $V_{DS}(t)$, $i_D(t)$ when it is turned on

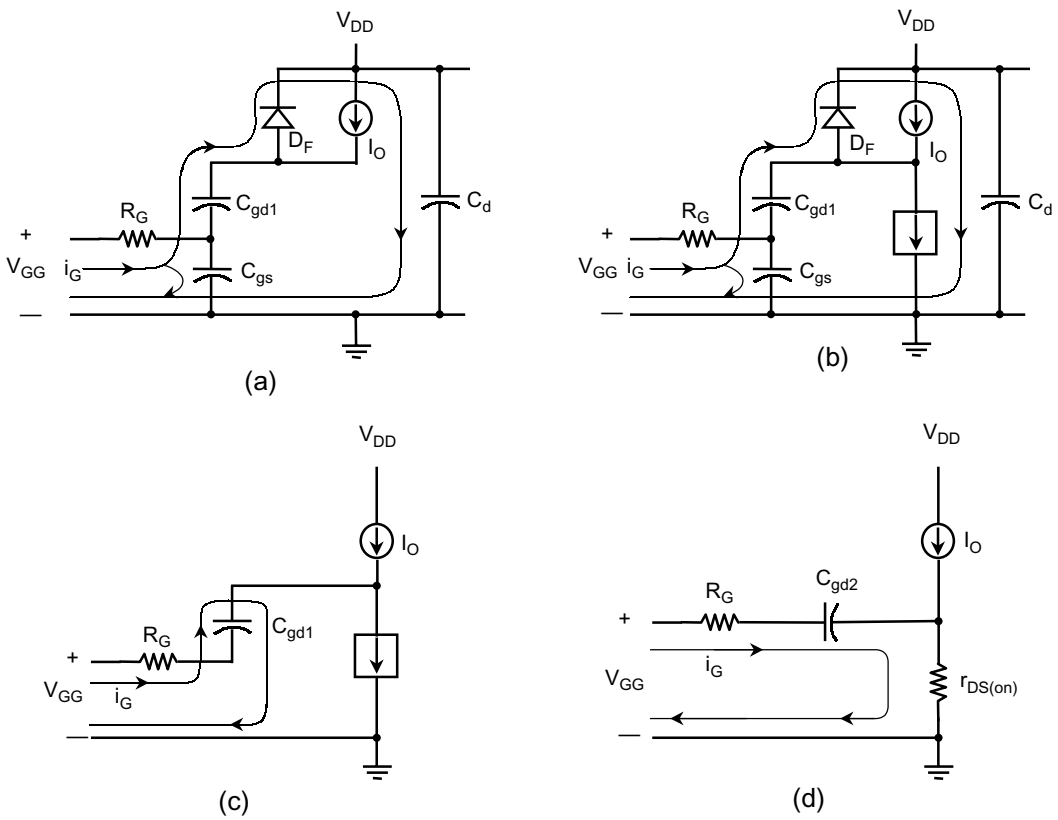


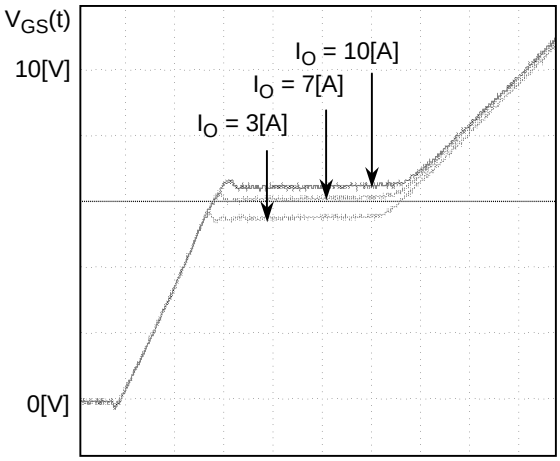
Figure 13: Equivalent Circuits of the MOSFET with Turn-on Divided into 4 Periods at the Diode-clamped Inductive Load Circuit.

(a) equivalent circuit of period $t_0 \sim t_1$
(b) equivalent circuit of period $t_1 \sim t_2$
(c), (d) equivalent circuit of period $t_2 \sim t_3$
(d) equivalent circuit of period t_3

1. $t_0 \sim t_1$: As i_G charges C_{gs} and C_{gd}, V_{GS} increases from 0[V] up to $V_{GS(th)}$. The graph of increasing $V_{GS}(t)$ seems to be increasing linearly, but it is in fact an exponential curve having a time constant of $\tau_1 = R_G(C_{gs} + C_{gd1})$. As shown in Figure 13 (a), V_{DS} is still equal to V_{DD}, and i_D is zero. The MOSFET is still in the turn off state.

2. $t_1 \sim t_2$: V_{GS} increases exponentially passing $V_{GS(th)}$, and as V_{GS} continues to increase, i_D begins to increase and reaches full load current (I_O). So (V_a) varies to I_O condition in t_2. When i_D is smaller than I_O, and when it is in a state where the D_F is being conducted, V_{DS} maintains the V_{DD}, but the graph shows the voltage which is a little less than V_{DD}. This is caused by the voltage drop due to the existing inductance in the line of the circuit.

The following graph shows the $V_{GS}(t)$ measuring the V_a variation in accordance with i_D conditions in turn-on state.



Device: FQP10N20

Test Condition: V_{DS} = 160[V]
V_{GS} = 10[V]

Division: $V_{GS}(t)$: 2[V]/div
t: 1[µsec]/div

3. $t_2 \sim t_3$: V_{GS} is a constant value in accordance with the transfer characteristics as it is in an active region where i_D is the full load current (I_O). So, i_G can only flow through C_{gd}, and is obtained by the following equation.

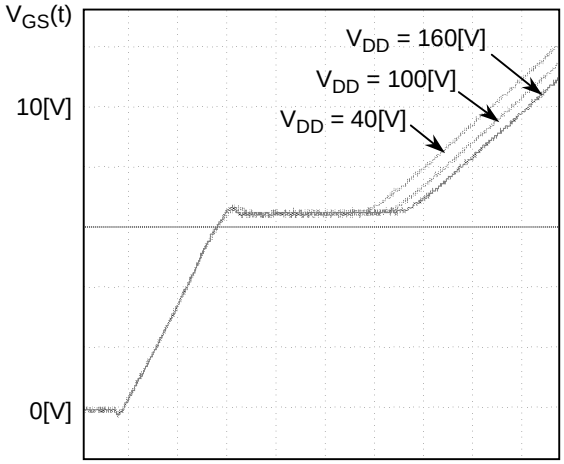
$$i_G = \frac{V_{GG} - V_a}{R_G}$$

So, the V_{DS} can be configured as the following ratios.

$$\frac{dv_{DG}}{dt} = \frac{dv_{DS}}{dt} = \frac{i_G}{C_{gd}} = \frac{V_{GG} - V_a}{R_G C_{gd}}$$

This is the region where the MOSFET is still operating in the active region, and as the V_{DS} decreases, it gets closer to the ohmic region. When V_{DD} increases, $t_2 \sim t_3$ (flat region of V_{GS}) also increase.

The following figure graphs $V_{GS}(t)$ and shows the variation of $t_2 \sim t_3$ (flat region of V_{GS}) in accordance with the V_{DD} condition.



Device: FQP10N20

Test Condition: I_O = 10[A]
V_{GS} = 10[V]

Division: $V_{GS}(t)$: 2[V]/div
t: 1[μsec]/div

At t_3 V_{DS} becomes $V_{DS(on)}=I_O \bullet r_{DS(on)}$, and the transient is completed. And the MOSFET is placed at the boundary of entering the ohmic region from the active region.

4. $t_3 \sim t_4$: It is the period where it operates in an ohmic region. The V_{GS} increases up to V_{GG} with a time constant of $\tau_2 = R_G(C_{gs} + C_{gd2})$

3) Drain-source On Resistance ($R_{DS(on)}$)

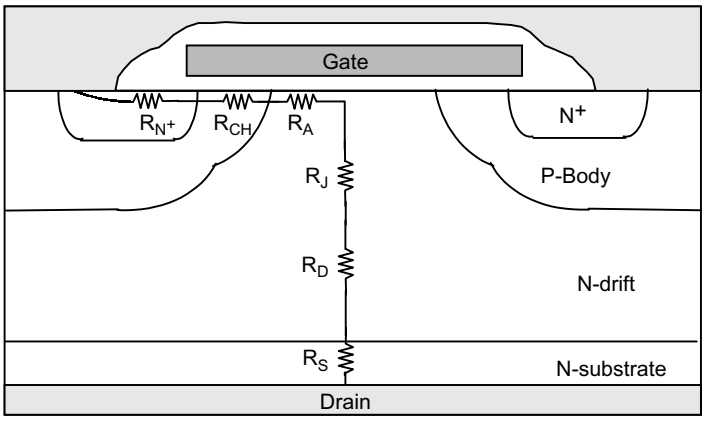


Figure 14: The Vertical Structure of a MOSFET Showing Internal Resistance

In a MOSFET $R_{DS(on)}$ is the total resistance between the source and the drain during the on state, and it is an important parameter determining maximum current rating and loss. To reduce $R_{DS(on)}$, the integrity of the chip and trench technique are used. This can be stated as shown in the following equation:

$$R_{DS(on)} = R_{N^+} + R_{CH} + R_A + R_j + R_D + R_S$$

where R_{N^+}: This is the resistance of the source region with N^+ diffusion, and it only uses a small portion of resistance compared to other components that form $R_{DS(on)}$. It can be ignored in high voltage power MOSFETs.

R_{CH}: This is the resistance of the channel region where it is the most dominant factor of $R_{DS(on)}$ in low voltage MOSFETs. This resistance can be varied by the ratio of the channel's width to the length, the thickness of the gate oxide, and the gate drive voltage.

R_A: As the gate drive voltage is supplied, charges start to accumulate in N^- epi. surface (the plate under C_{gd}), and forms a current path between the channel and the JFET region. The resistance of this accumulation region is R_A. The resistance varies by the charge in the accumulation layer, and the mobility of the free carriers at the surface. And if the gate electrode is reduced, its effect is the same as reducing the length of the accumulation layer, so the value of R_A is reduced while R_J increases.

R_J: The N^- epi. region between the P-bodies is called the JFET region, because the P-body region acts like the gate region of a JFET. The resistance of this region is R_J.

R_D: The resistance occurring from right below the P-body to the top of the substrate is called R_D, and is the most important factor in high voltage MOSFETs

R_S: This is the resistance of the substrate region. It can be ignored in high voltage MOSFETs. But in low voltage MOSFETs, where the breakdown voltage is below 50[V], it can have a large effect on $R_{DS(on)}$.

Additional resistances can arise from a non-ideal contact between the source/drain metal and the N^+ semiconductor regions, as well as from the leads used to connect the device to the package.

$R_{DS(on)}$ increases with the temperature. (positive temperature coefficient)
This is because the mobility of the hole and electron decreases as the temperature rises. The $R_{DS(on)}$, at a given temperature of a p / n- channel power MOSFET, can be estimated with the following equation.

$$R_{DS(on)}(T) = R_{DS(on)}(25°C)\left(\frac{T}{300}\right)^{2.3}$$

where T: absolute temperature

This is an important characteristic of device stability and paralleling. It doesn't need any external circuit's assistance to have good current sharing when $R_{DS(on)}$ increases with the temperature, and is connected in parallel.

4) Threshold Voltage ($V_{GS(th)}$)

This is the minimum gate bias which enables the formation of the channel between the source and the drain. The drain current increases in proportion to $(V_{GS}–V_{GS(th)})^2$ in the saturation region.

1. High $V_{GS(th)}$
   It is difficult to design gate drive circuitry for the power MOSFET because a high gate bias voltage is needed to turn it on.

2. Low $V_{GS(th)}$
   When the $V_{GS(th)}$ of the n-channel power MOSFET becomes negative due to the existence of charges in the gate oxide, it shows the characteristics of a normally on state, where the conductive channel exists even in a zero gate bias voltage. Even if $V_{GS(th)}$ is positive, and the value is very small, there could be a turn-on either by the noise signal of the gate terminal, or by the increasing gate voltage during high speed switching.

   The $V_{GS(th)}$ can be controlled by the gate oxide thickness. Normally the gate oxide is kept thick in a high voltage device so that the $V_{GS(th)}$ is set at 2~4[V], and the gate oxide is kept thin in a low voltage device (logic level) so that $V_{GS(th)}$ is 1 ~ 2 [V]. Additionally, $V_{GS(th)}$ can be controlled by back ground doping (the density of P-body for the n-channel power MOSFET). It increases in proportion to the square root of the background doping.

   Temperature characteristic

   $V_{GS(th)}$ decreases as the temperature increases, and the rate of decrease can be varied by the gate oxide thickness and background doping level. In other words, the decrease rate increases when the gate oxide becomes thicker and the background doping level increases.

5) Transconductance (g_{fs})

This is the gain in the MOSFET. It can be expressed as the following equation and represents the amount of change in drain current by the amount of change in the gate-source bias voltage.

$$g_{fs} = \left[\frac{\Delta I_{DS}}{\Delta V_{GS}}\right]_{V_{DS}}$$

V_{DS} should be set so that the device can be activated in the saturation region. V_{GS} should be supplied so that the I_{DS} becomes 1/2 of the maximum current rating. g_{fs} varies depending on the channel width/length, and the gate oxide thickness. As shown in Figure 15, after $V_{GS(th)}$ is applied, g_{fs} increases dramatically with the increase in the drain current, and it becomes a constant after the drain current reaches a certain point (at higher values of drain current). If g_{fs} is high enough, high current handling capability can be gained from the low gate drive voltage. A high frequency response is also possible.

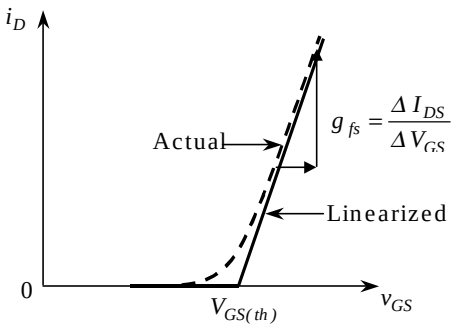


Figure 15: Transfer Curve & g_{fs}

Temperature characteristic

g_{fs} decreases as the temperature increases due to the reduction of mobility. From the following equation which is similar to the $R_{DS(on)}$ and temperature relationship, it is possible to know the g_{fs} changes by the changes in temperature.

$$g_{fs}(T) = g_{fs}(25°C)\left(\frac{T}{300}\right)^{-2.3}$$

where T: absolute temperature

6) Drain-Source Breakdown Voltage (BV_{DSS}), Breakdown Voltage Temperature Coefficient ($\Delta BV/\Delta T_J$)

BV_{DSS} is the maximum drain-to-source voltage where the MOSFET can endure without the avalanche breakdown of the body-drain pn junction in off state (where the gate and source are shorted). The measurement conditions are V_{GS}=0[V],I_D=250[μA], and the length of the drift region (N^- epitaxy) is determined by the BV_{DSS}. Avalanche, reach-through, punch-through, zener, and dielectric breakdowns are the 5 factors which drive breakdown.

Temperature characteristic

As junction temperature increases, it does so linearly, and whenever it goes up 100 [°C], 10[%] of BV_{DSS} at 25 [°C] increases (refer to the breakdown voltage temperature coefficient ($\Delta BV/\Delta T_J$) and Figure 7. breakdown voltage vs. temperature in the data book.)

7) Drain-to-Source Leakage Current (I_{DSS})

This can be measured by providing the maximum drain-to-source voltage and 80 [%] of the voltage (T_C=125[°C]) in the off state where the gate is shorted to the source. I_{DSS} is more sensitive to the temperature than BV_{DSS}, and it has a positive temperature coefficient.

8) Gate – to – Source Voltage (V_{GS})

This represents the maximum operating gate – to – source voltage. The negative voltage handling capability enables the enhancement of the turn – off speed by providing reverse bias to the gate and the source.

9) Gate – Source Leakage, Forward / Reverse (I_{GSS})

This is measured by providing the maximum operating gate – to – source voltage (V_{GS}) between the gate and the source. Forward or reverse direction is decided by the polarity of the V_{GS}. I_{GSS} is dependent on the quality of the gate oxide and device size.

10) Switching characteristics ($t_{d(on)}$, t_r, $t_{d(off)}$, t_f)

The power MOSFETs have good switching characteristics as there is no storage delay caused by the minority carrier, and no variation caused by the temperature. The following figure shows the switching sequence divided into sections.

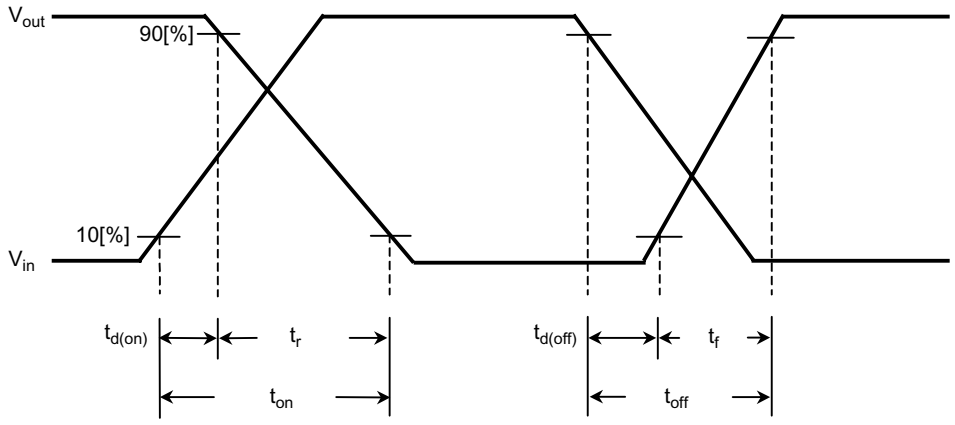


Figure 16: Resistive Switching Waveforms

$t_{d(on)}$(turn-on delay time): This is the time for the gate voltage V_{GS} to reach up to the threshold voltage $V_{GS(th)}$. The input capacitance during this period is C_{gs}+C_{gd}. This also means that this period is the charging period to bring up the capacitance to the threshold voltage.

t_r (rise time): It is the period after the V_{GS} reaches the $V_{GS(th)}$ to complete the transient. It can be divided into 2 regions. One is the period where the drain current starts from zero (increasing with the gate voltage in accordance with the transfer characteristics) and reaching up to the load current. The other region is when the drain voltage starts to drop and reaches the on-state voltage drop. As shown in the gate charge characteristics graph, the V_{GS} maintains a constant value as the drain current is constant in this region where the voltage decreases. During the rise time, as both the high voltage and the high current exist in the device, high power dissipation occurs. So the rise time should be reduced by reducing the gate series resistance and the drain-gate capacitance (C_{gd}). After this, the gate voltage continues to increase up to the supplied voltage level. But, as the drain voltage and the current are already in steady–state, they are not affected during this region.

$t_{d(off)}$(turn-off delay time): The gate voltage operates in the supplied voltage level during the on state, and when the turn-off transient starts, it starts to decrease. The $t_{d(off)}$ is the time for the gate voltage to reach the point where it is required to make the drain current become saturated at the value of load current. During this time there are no changes to the drain voltage and the current.

t_f (fall time): It is the time where the gate voltage reaches the threshold voltage after $t_{d(off)}$. It is divided into the region where the drain voltage reaches the supply voltage from on-state voltage, and the region where the drain current reaches zero from the load current. As there is a lot of power dissipation in the t_r region during turn-on state, the power dissipation occurs in the t_f region during turn-off state. Hence, t_f must be reduced as much as possible. After this, the gate voltage continues to decrease until it reaches zero. But as the drain voltage and the current are already in steady – state, they are not affected during this region.

11) Single – Pulsed Avalanche Energy; Unclamped Inductive Switching (E_{AS})

(1) Power MOSFET Turn-off (In inductive load circuit)

While in an on-state (supplying positive voltage exceeding the threshold voltage in n-channel device), the electrons flows into the drain from the source through the inversion layer (=channel) of the body surface, and forms a current flow from the drain to the source. If it is an inductive load, this current will increase linearly. To turn-off the MOSFET, the gate voltage must be removed or a reverse voltage applied so that it eliminates the inversion layer of the body surface. Once the charges at the inversion layer begins to dissipate and the channel current (drain current) begins to

reduce, the inductive load increases the drain voltage so that it maintains the drain current. When the drain voltage increases, the drain current is divided into the channel current and the displacement current. The displacement current is the current generated as the depletion region is developed at the drain-body diode, and it is proportional to dv_{DS}/dt (The ratio of drain voltage rise by the time). The dv_{DS}/dt is limited by how fast the gate is discharged and by how fast the drain-body depletion region is charged. Specially, the charge of the drain-body depletion region is determined by C_{ds} and the magnitude of the drain current. When the drain voltage increases, and cannot be clamped by an external circuit, the (UIS) drain-body diode starts to build the current carriers through avalanche multiplication, and the device falls into a sustaining mode. While in sustaining mode, all the drain current (avalanche current) goes through the drain-body diode, and is controlled by the (channel current equals to zero) inductor load. If the current (leakage current, displacement current (dv_{DS}/dt current), avalanche current) flowing at the body region underneath the source is large enough, the parasitic bipolar transistor becomes active, and can result in device failure.

Figure 17 shows the drain voltage and the current when a single pulse (width: t_P) is supplied at the unclamped inductive load circuit.

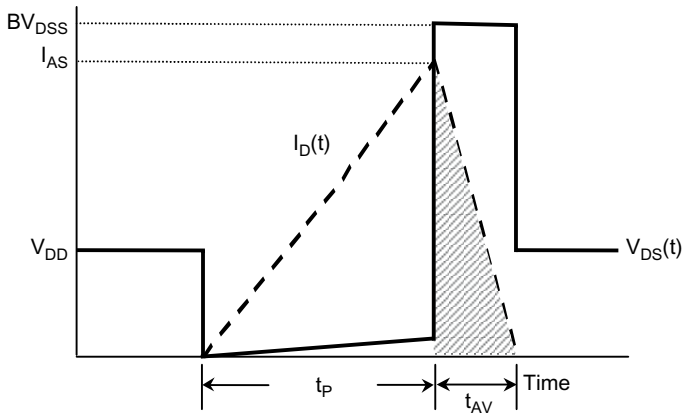


Figure 17: Unclamped Inductive Switching Waveforms.

$I_D(t)$ can be changed by the inductor load size, supply voltage (V_{DD}) and the gate pulse width (t_P). The shaded area of the avalanche region (t_{AV}) shows the dissipation energy (E_{AS}). E_{AS} and t_{AV} can be calculated with the following equation.

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

$$t_{AV} = \frac{L_L I_{AS}}{BV_{DSS}}$$

(2) A power MOSFET Failure has the following characteristics during an inductive turn-off.

1. It has the same electrical characteristics as the second breakdown of the bipolar transistor.

2. Independent from dv_{DS}/dt.
   By maintaining the gate turn-off voltage constantly, and changing the magnitude of the external gate resistance, the magnitude of the gate turn-off current changes. This changes the dV_{DS}/dt. If dV_{DS}/dt current causes a device failure, the voltage that can lead to a second breakdown should be decreased with an increase in dV_{DS}/dt. But when measuring the second breakdown voltage while changing the external gate resistance (changing dV_{DS}/dt), the highest voltage should be measured at the highest dV_{DS}/dt. ("TURN-OFF FAILURE OF POWER MOSFETS", David L. Blackburn)

3. The voltage at which failure occurs increases with the temperature.

4. Critical current reduces as temperature increases.
   Critical current represents the maximum value of the drain current that can safely turn-off the device in an unclamped mode. At currents exceeding this, a second breakdown occurs.

5. It is not related to the magnitude of the load inductance.
   $\rightarrow$The avalanche current from the drain-body diode activates the parasitic bipolar transistor. This causes the MOSFET to fail.

12) Repetitive Avalanche Rating (E_{AR}, I_{AR})

E_{AR}: It represents avalanche energy for each pulse under repetitive conditions.

I_{AR}: It represents the maximum avalanche current, and is the same as the I_D rating of the device.

13) Drain-to-Source dv/dt Ratings

When high dv/dt is supplied at the drain, there is a possibility of current conduction in the power MOSFET, and in some cases, this can destroy the device. Given below are some instances of device turn-on due to dv/dt.

(1) Static dv/dt

1. False turn-on

2. Parasitic transistor turn-on

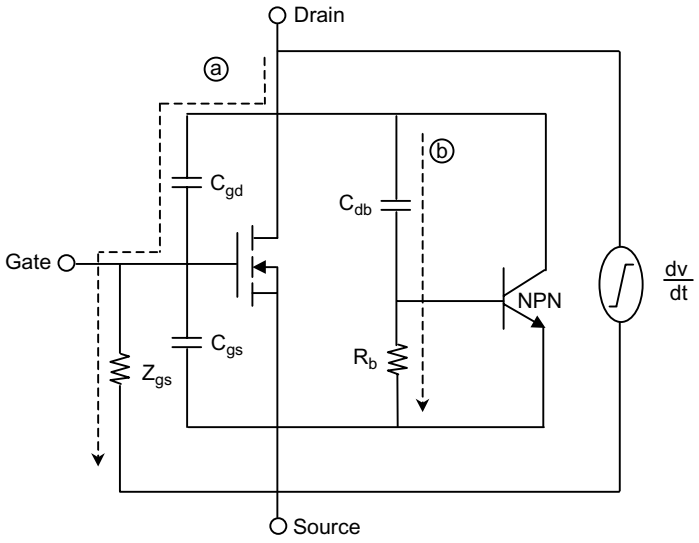


Figure 18: Equivalent Circuit of a N-channel MOSFET

1. In the off state, a sudden increase in drain voltage changes the voltage across the parasitic capacitance between the drain and the gate, and develops displacement current (a) of C*dv/dt. If voltage exceeding $V_{GS(th)}$ develops between the gate and source due to the displacement current and the gate-to-source impedance (Z_{gs}), it triggers a false turn-on of the MOSFET. Here the parasitic capacitance between the drain and gate can be C_{gd} or larger than C_{gd} in depending on the circuit layout. Z_{gs} is the impedance of the drive circuit, and can be presented as a series of R, L battery components. Due to the false turn-on, the device falls into a current conduction state, and in severe cases, high power dissipation develops in the device and results in destructive failure. The following equation shows the voltage drop V_{GS} across Z_{gs}, and dv/dt capability in this mode.

$$V_{GS} = Z_{gs} C_{gd} \left[\frac{dv}{dt}\right]$$

$$\left[\frac{dv}{dt}\right] = \frac{V_{GS(th)}}{Z_{gs} C_{gd}}$$

   To increase dv/dt capability, a gate drive circuit with very low impedance should be used, and $V_{GS(th)}$ must be increased. But in a drive circuit with low impedance, the cost is high and increasing the $V_{GS(th)}$ is associated to the rise of $R_{DS(on)}$. As $V_{GS(th)}$ has a negative temperature coefficient, the possibility of a false turn-on increases as the temperature rises. But typically, gate voltage doesn't go over the threshold voltage, and the high device resistance limits the device current. Hence device destruction due to false turn-on is rare.

2. In the off state, a sudden increase in drain voltage changes the voltage across C_{db}, and it develops current (b) flowing through R_b. And when the voltage across the R_b goes over V_{be} (emitter-base forward bias voltage where the parasitic bipolar transistor is turned on, approximately 0.7[V]), the parasitic bipolar transistor is turned on. When the parasitic bipolar

transistor is turned on, the breakdown voltage of the device is reduced from BV_{CBO} to BV_{CEO} which is 50 ~ 60 [%] of BV_{CBO}. If a drain voltage larger than BV_{CEO} is supplied, the device falls into an avalanche breakdown. If this drain current is not limited externally, the device can be destroyed by the second breakdown. The following equation shows the dv/dt capability in this mode.

$$\left[\frac{dv}{dt}\right] = \frac{V_{be}}{R_b C_{db}}$$

From the above equation, it is easy to see that the dv/dt capability is determined by the internal device structure. For high dv/dt capability, the R_b value must be small. This is done by increasing the doping level of the P-body region, and reducing the length of the N^+ emitter as much as possible. R_b is also affected by the drain voltage, and as the drain voltage increases, the depletion layer expands and enlarges the R_b value. When the temperature increases, as R_b is increased by the reduction of mobility and as the V_{be} decreases, the possibility of turn-on of the parasitic transistor increases. But as the base and the emitter is shorted by the source contact, the R_b value is very small. This occurs only if the dv/dt is enormously large.

→ In a false turn-on the dv/dt can be controlled externally, but in a parasitic transistor's turn-on, the dv/dt is determined by device design. This is the difference between these two modes.

(2) Dynamic dv/dt

If there is a sudden current interruption such as a clamped inductive turn-off in high speed switching, the device is destroyed by concurrent stresses caused by high drain current, high drain-source voltage, and displacement current at the parasitic capacitance.

(3) Diode Recovery dv/dt

This is the main cause of dv/dt failure in specific applications such as circuits using a body drain diode. The data book gives the maximum value for dv/dt. Exceeding this value will cause device failure due to excessive diode recovery dv/dt. Figure 19 shows a motor control circuit application which has a diode recovery dv/dt problem.

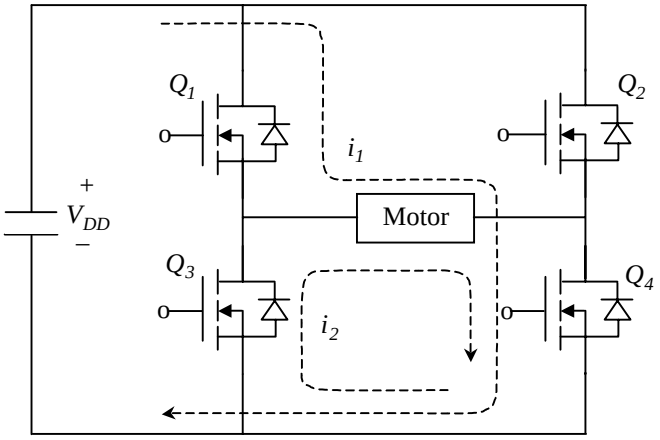


Figure 19: Motor Control Circuit

First Q_1 and Q_4 are conducted, and put in a state where current i_1 passes. If Q_1 is turned-off to control the speed of the motor then the current flows through the parasitic diode (freewheeling diode) of Q_3 as i_2. The parasitic diode of Q_3 falls into a forward bias state, and due to the characteristic of the diode, the minority charge begins to accumulate. When Q_1 is turned on, the current again becomes i_1, and the minority charge accumulated in the parasitic diode Q_3, is removed by the diode reverse recovery current (Figure 20 section a of I_S). Once the minority charge is removed to a certain level, the depletion region of the body drain diode expands and makes more reverse recovery current (Figure 20 section b of I_S). If this turns on the parasitic bipolar transistor, then Q_3 is destroyed. Figure 20 shows the diode recovery dv/dt test circuit & waveforms from our data book. And from this test, not only dv/dt but also V_{SD} (diode forward voltage), t_{rr} (reverse recovery time), and Q_{rr} (reverse recovery charge) data can be obtained. In the test, the V_{DD} value must be less or equal to the BV_{DSS}. Typically the V_{DD} is set at 80[%] of BV_{DSS}, and the pulse period of the driver V_{GS} must be controlled so that the I_S can become the continuous drain current I_D.

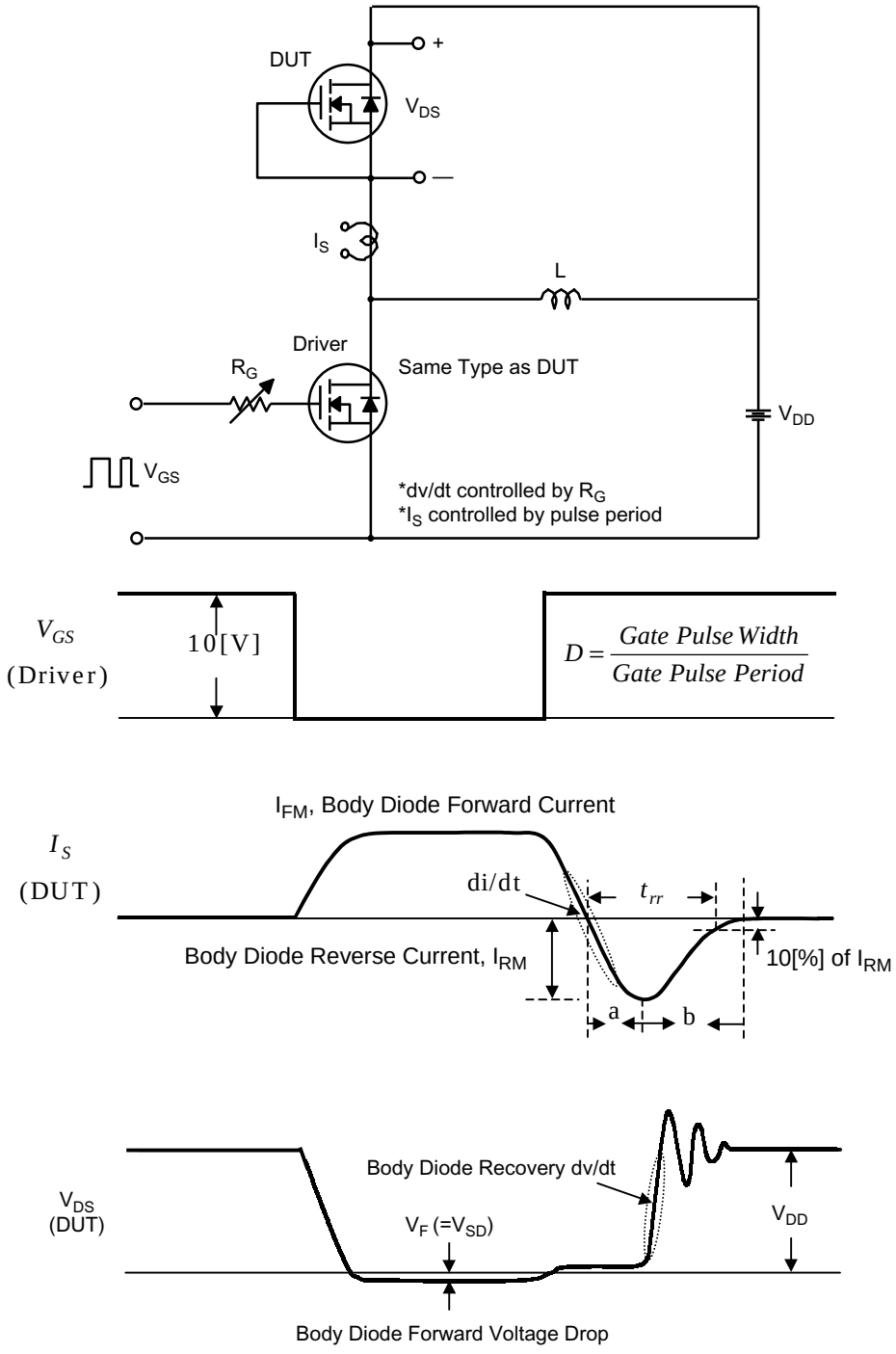


Figure 20: Diode Recovery dv/dt Test Circuit & Waveforms

Rev D, July 2000

The value of di/dt and dv/dt becomes larger as R_G is reduced. First t_{rr} can be obtained by measuring the part shown in the wave of I_S where the di/dt (It is measured from the point where it is 50[%] of I_{FM} above the ground to the point where it is 75[%] of I_{RM} below the ground) is 100[A/µs]. Q_{rr} can be calculated as (I_{RM} x t_{rr})/2. dv/dt can be measured from the point where it is between 10[%] ~ 90[%] of V_{DD} with the di/dt condition (It is measured from the point where it is 50[%] of I_{FM} above the ground to the point where it is 75[%] of I_{FM} below the ground) as stated in the data book. I_S (continuous source current) and I_{SM} (pulsed – source current) represents the current rating of the source – drain diode, and $I_S = I_D$ (continuous drain current), and $I_{SM} = I_{DM}$ (drain current – pulsed).

14)Thermal Characteristics (T_J, $R_{\theta JC}$, $R_{\theta SA}$, $Z_{\theta JC}(t)$)

The power loss of the device turns into heat and increases the junction temperature. This degrades device characteristics and reduces its life span. It is very important to lower the junction temperature by discharging heat from the chip junction. The thermal impedance ($Z_{\theta JC}(t)$) is used to monitor the above.

Thermal characteristics terminology is explained below:

T_J (Junction Temperature)

T_C (Case Temperature): Temperature at a point of the package which has the semiconductor chip inside.

T_S (Heat Sink Temperature)

T_A (Ambient Temperature): Ambient temperature of the environment of the operating device.

$R_{\theta JC}$ (Junction – to – Case Thermal Resistance)

$R_{\theta CS}$ (Case – to – Sink Thermal Resistance)

$R_{\theta SA}$ (Sink – to – Ambient Thermal Resistance)

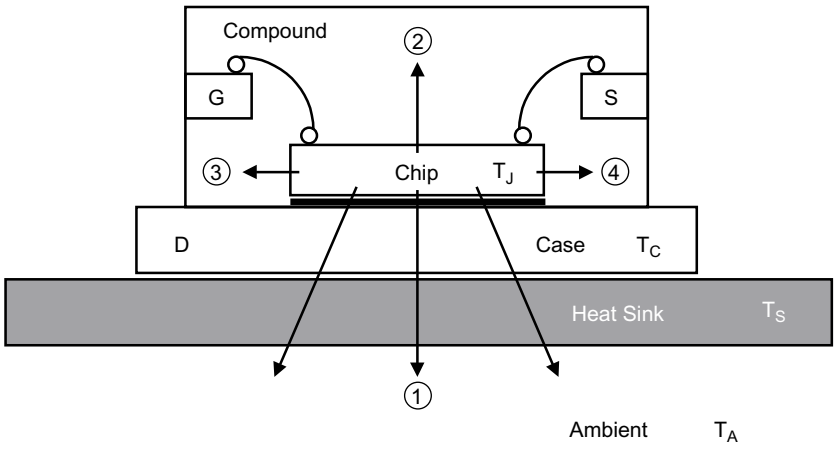


Figure 21: The Path of Thermal Discharge at the Chip Junction

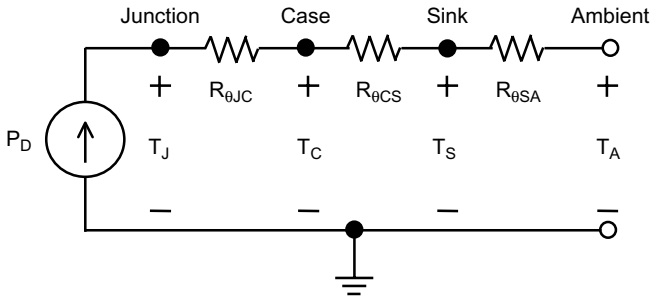


Figure 22: An Equivalent Circuit Based on Thermal Resistance

As shown in Figure 21, the heat produced at the chip junction normally discharges over 80[%] in the direction of ¨ and about 20[%] in the direction of ¦ Æ Ø. The path of the thermal discharge is the same as the movement of the current, and is represented in Figure 22 after considering thermal resistance. This is true only for DC operation. Most MOSFETs are used in switching operations with a fixed duty factor. Hence, thermal capacitance should be taken into consideration along with thermal resistance. The thermal resistance from the chip junction to the ambient is $R_{\theta JA}$ (junction – to – ambient thermal resistance), and the equivalent circuit can be expressed as the following equation.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA}$$

1. $R_{\theta JC}$ (Junction – to – Case Thermal Resistance)
   $R_{\theta JC}$ is the internal thermal resistance from the chip junction to the package case. Once the size of the die is decided, this thermal resistance of pure package is only determined by the package design, and lead frame material. $R_{\theta JC}$ can be measured under the condition of T_C = 25[°C] and can be written as the following equation.

$$R_{\theta JC} = \frac{T_J - T_C}{P_D}[°C/W]$$

   The condition T_C = 25[°C] means that the infinite heat sink is mounted.

   - Infinite heat sink: The case temperature of the package is equal to the environment temperature. It is the heat sink, which can realize $T_C = T_A$.

2. $R_{\theta CS}$ (Case – to – Sink Thermal Resistance)
   This is the thermal resistance from the package case to the heat sink. It can vary due to the package and the mounting method to the heat sink.

3. $R_{\theta SA}$ (Sink – to – Ambient Thermal Resistance)
   This is the thermal resistance from the heat sink to the ambient, and it is determined by heat-sink design.

Thermal Response Characteristics

In Figure 11 in the data book, the graph of the thermal response shows the change of $Z_{\theta JC}(t)$ (junction– to–case thermal impedance) due to the change of the square wave pulse duration with a few duty factor conditions. $Z_{\theta JC}(t)$ can decide the junction temperature rise with the equation of @ Notes: 3. $T_{JM}–T_C=P_{DM}*Z_{\theta JC}(t)$ (considering power dissipation to be a constant value (P_{DM}) during the conduction period as in Figure 11 of the data book), it becomes saturated to the maximum value of ($R_{\theta JC}$) as it reaches low frequency or DC operation where the duty factor D=1. Figure 23 shows the junction temperature rise with the increasing duty factor.

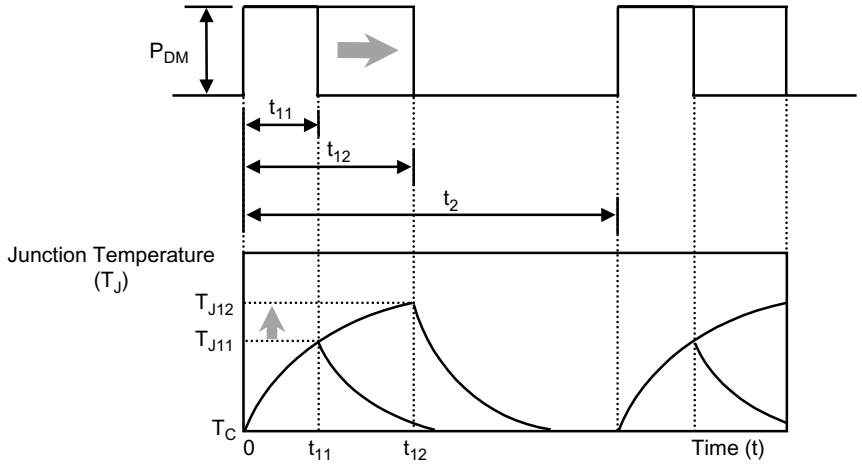


Figure 23: The Change in Junction Temperature due to Conduction Time

A single pulse curve determines the thermal resistance for repetitive power pulses having a constant duty factor (D) as shown in the following equation.

$$Z_{\theta JC}(t) = R_{\theta JC} \bullet D + (1–D) \bullet S_{\theta JC}(t)$$

where $Z_{\theta JC}(t)$: thermal impedance for repetitive power pulses with a duty factor of D.

$S_{\theta JC}(t)$: thermal impedance for a single pulse.

15) Continuous Drain Current (I_D), Drain Current - Pulsed (I_{DM})

(1) Continuous Drain Current (I_D)

As shown in the equation below, the I_D rating is determined by the heat removal ability of the device. In Figure 10. in the data book, the graph of max. drain current vs. case temperature shows the increasing permissible I_D as T_C decreases.

$$I_D(T_C) = \sqrt{\frac{T_{Jmax} - T_C}{R_{DS(on)}(T_{Jmax}) \bullet R_{\theta JC}}}$$

Where $R_{DS(on)}(T_{Jmax})$: the maximum value of on-resistance in an appropriate drain current condition ($\frac{1}{2} \bullet I_D$ in the data book) at T_{Jmax}. as maximum $R_{DS(on)}$ specified in the data book is at T_C = 25[°C] $R_{DS(on)}$ (T_{Jmax}) could easily be analogized by the Figure 8's graph of on-resistance vs. temperature in the data book.

$R_{\theta JC}$: maximum junction – to – case thermal resistance

T_C: case temperature

In real device applications where it is not feasible to maintain the temperature at T_C = 25[°C], the I_D(60 ~ 70 [%] of I_D at T_C = 25[°C]) at T_C = 100[°C] is a more usable specification.

(2) Drain Current - Pulsed (I_{DM})

The drain current over continuous drain current rating is that it should not go over the maximum junction temperature. The maximum upper limit is I_{DM}. I_{DM} which is about 4 times the value of I_D as shown in the following equation.

$$I_{DM} = I_D(T_C = 25[°C]) \times 4$$

Repetitive rating: Pulse width limited by maximum junction temperature

16) Total Power Dissipation (P_D), Linear Derating Factor

(1) $P_D(T_C) = I_D^2(T_C) \bullet R_{DS(on)}(T_{Jmax}) = \frac{T_{Jmax} - T_C}{R_{\theta JC}}$

(2) Linear derating factor = $\frac{1}{R_{\theta JC}}$

17) Safe Operating Areas (SOA)

(1) SOA (FBSOA):

It defines the maximum value of the drain – source voltage and drain current which guarantees safe operation when the device is at the forward bias.

(2) Boundaries

1. The right - hand boundary: maximum drain – source voltage rating
2. The horizontal line:
   DC: maximum rated continuous drain current at T_C = 25[°C].

   For MOSFETs, excluding package limitations, maximum rated continuous drain current can be determined by the $R_{DS(on)}(T_{Jmax})$ as in the equation below.

$$I_D(T_C) = \sqrt{\frac{T_{Jmax} - T_C}{R_{DS(on)}(T_{Jmax}) \bullet R_{\theta JC}}}$$

   Single pulse: Maximum rated drain current - pulsed

$$I_{DM} = I_D(T_C) \times 4$$

3. The upper limit with + slope: The boundary where the power can be limited by the drain – to – source on – resistance.
4. The upper limit with – slope: It is determined by the transient thermal impedance and the maximum junction temperature

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